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Title

SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

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TITLE OF THE INVENTION:

SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a semiconductor device having a circuit constituted by thin film transistors on the substrate thereof having an insulation surface, and to a method of fabricating such a semiconductor device. More specifically, this invention relates to an electro-optical device typified by a liquid crystal display device and a construction of an electronic appliance having the electro-optical device mounted thereto.

The term "semiconductor device" used in this specification represents devices in general that function by utilizing semiconductor characteristics, and includes the electro-optical device and the electronic appliance having the electro-optical device mounted thereto, that are described above.

2. Description of the Related Art

Development of semiconductor devices having a large area integrated circuit comprising thin film transistors (hereinafter called the "TFTs") has made a steady progress, and an active matrix liquid crystal device and an adhesion type image sensor are typical examples of such semiconductor devices.

The TFTs can be classified in accordance with their structures and their fabrication methods. The TFTs using a semiconductor film having a crystal structure as an active layer (crystalline TFTs), in particular, can form a variety of functional circuits because their field effect mobility is high.

The term "semiconductor film having the crystal structure" used in this specification represents a single crystal semiconductor, a polycrystalline semiconductor and a micro-crystal semiconductor. Furthermore, the term includes the semiconductors that are described in Japanese Patent Laid-Open Nos. Hei 7-130652(1995), Hei 8-78329(1996), Hei 10-135468(1998) and Hei 10-135469(1998).

In the active matrix liquid crystal display device, a pixel matrix circuit (also called a "pixel area") comprising n-channel TFTs and an integrated circuit comprising a CMOS circuit as a basic circuit such as a shift register circuit, a level shifter circuit, a buffer circuit, a sampling circuit, and so forth, are formed for each functional block on one substrate.

In the adhesion type image sensor, on the other hand, integrated circuits such as a sample-and-hold circuit, a shift register circuit, a multiplexer circuit, and so forth, are formed using the TFTs.

Because the operating conditions of these circuits are not always the same, performance required for each TFT naturally varies to certain extents.

The pixel unit, for example, employs the construction that includes switching devices comprising an n-channel TFT and an auxiliary signal storage capacitance, and drives the liquid crystal by applying a voltage. The liquid crystal must be driven by an alternating current, and a system called "frame inversion driving" has been employed. Therefore, the TFTs must sufficiently reduce a leakage current as one the requisites imposed on them.

Because a high driving voltage is applied to the buffer circuit, a withstand voltage must be high. It is also necessary to sufficiently secure an ON current in order to improve current driving capacity.

However, the crystalline TFT involves the problem that its OFF current is likely to become high. From the aspect of reliability, the crystalline TFT is believed yet unequal to MOS transistors (the transistors that are fabricated on a single crystal semiconductor substrate) used for LSIs. For instance, a deterioration phenomenon such as the drop of the ON current has often been observed in the crystalline TFT. This problem results from the hot carrier effect. In other words, the hot carriers generated by a high electric field in the proximity of a drain are believed to cause this deterioration.

A lightly doped drain (LDD) structure is known as a structure of the TFT. In this structure, a low concentration impurity region is disposed between a channel region and a source or drain region into which an impurity is doped in a high concentration, and this low concentration impurity region is referred to as the "LDD" region.

The LDD structure can be further classified into a GOLD (Gate-drain Overlapped LDD) structure in which the LDD region overlaps with the gate electrode and the LDD structure in which it does not, depending on the positional relationship with the gate electrode. The GOLD structure mitigates the high electric field in the proximity of the drain, prevents the hot carrier effect and thus improves reliability. According to Mutsuko Hatano, Hajime Akimoto and Takeshi Sakai, "IEDM97 Technical Digest", p523-526, 1997, a GOLD structure having side walls formed of silicon has been confirmed to have by far more excellent reliability than TFTs having other structures.

Nonetheless, the GOLD structure is not free from the problem that the OFF current becomes greater than the ordinary LDD structure, and it has not always been preferable to fabricate all the TFTs of a large area integrated circuit by this GOLD structure. If the OFF current increases in the n-channel TFTs constituting the pixel unit, for example, power consumption increases and abnormality is likely to appear in image display. For this reason, it is not preferable to apply as such the crystalline TFTs having the GOLD structure.

Another problem of the LDD structure is that the ON current drops with the increase of the series resistance. The ON current can be freely designed by means of the channel width of the TFT, and an offset TFT is not always necessary to be provided to the TFTs that constitute the buffer circuit, for example.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a TFT having an optimum structure by each functional circuit in a semiconductor device having a large area integrated circuit typified by an active matrix liquid crystal display device and an image sensor.

It is another object of the present invention to provide a method of fabricating such TFTs on the same substrate by the same fabrication process.

It is another object of the present invention to provide a technology for achieving the objects described above and to realize a crystalline TFT having reliability equivalent or superior to that of an MOS transistor.

It is still another object of the present invention to improve reliability of a semiconductor device having a large area integrated circuit including various functional circuits constituted by such crystalline TFTs.

In a TFT having an LDD structure, the objects described above can be accomplished by the construction in which a region where the LDD region overlaps with a gate electrode and a region where it does not are disposed in one TFT.

In order to realize TFTs having an optimum structure for each functional circuit in a semiconductor device having a large area integrated circuit typified by an active matrix liquid crystal display device and an image sensor, the present invention employs the construction in which a ratio of a region, where the LDD structure overlaps with a gate electrode, to a region where it does not is varied for each TFT.

To obtain the construction described above, the present invention employs a fabrication process that forms n-channel TFTs by a non-self-alignment process and p-channel TFTs, by a self-alignment process.

Therefore, in a semiconductor device including a semiconductor layer, a gate insulation film, a gate electrode and a gate wiring connected to the gate electrode on a substrate having an insulation surface, the present invention provides a semiconductor device having a construction wherein each of the gate electrode and the gate wiring comprises a first conductor layer, the semiconductor layer includes a channel formation region, a first impurity region of one conductivity type, a second impurity region of one conductivity type sandwiched between the channel formation region and the first impurity region of one conductivity type and keeping contact with the channel formation region, and wherein a part of the second impurity region of one conductivity type overlaps with the gate electrode through the gate insulation film.

The first conductor layer applied to the present invention uses one or a plurality of elements selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W) and molybdenum (Mo), or a compound using the element or elements as the principal component. The second conductor layer is made of a low resistance conductor material of one or a plurality of elements selected from the group consisting of aluminum (Al) and copper (Cu), or a compound using the element or elements as the principal components.

The present invention can be applied to a semiconductor device including a matrix circuit comprising n-channel thin film transistors, and a CMOS circuit comprising n-channel thin film transistors and p-channel thin film transistors.

However, the construction of the present invention is not always necessarily applied to the p-channel TFTs in the CMOS circuit described above.

A method of fabricating a semiconductor device according to the present invention comprises the steps of forming a semiconductor layer on a substrate having an insulation surface; removing a part of the semiconductor layer and forming at least first and second island semiconductor layers; forming a gate insulation film in such a fashion as to keep contact with the first and second island semiconductor layers; adding an impurity element of one conductivity type into a selected region of the first island semiconductor layer and forming a second impurity region; forming a first conductor layer in contact with the gate insulation film; forming a second gate electrode overlapping with the second island semiconductor layer from the first conductor layer; adding an impurity element of a conductivity type opposite to one conductivity type into a selected region of the second island semiconductor layer, thereby forming a third impurity region; forming a first gate electrode overlapping with the first island semiconductor layer from the first conductor layer; and adding an impurity element of one conductivity type into a selected region of the first island semiconductor layer and forming a first impurity region.

A method of fabricating a semiconductor device according to another embodiment of the present invention comprises the steps of forming a semiconductor layer on a substrate having an insulation surface; removing a part of the semiconductor layer and forming at least first and second island semiconductor layers; forming a gate insulation film in contact with the first and second island semiconductor layers; adding an impurity element of one conductivity type into a selected region of the first island semiconductor layer and forming a second impurity region; forming a first conductor layer in contact with the gate insulation film; forming a first gate electrode overlapping with the first island semiconductor layer and a second gate electrode overlapping with the second island semiconductor layer from the first conductor layer; adding an impurity element of one conductivity type into a selected region of the first island semiconductor layer and forming a first impurity region; and adding an impurity element of a conductivity type opposite to one conductivity type into a selected region of the second island semiconductor layer and forming a third impurity region.

A method of fabricating a semiconductor device according to still another embodiment of the present invention comprises the steps of: forming a semiconductor layer on a substrate having an insulation surface; removing a part of the semiconductor layer and forming at least first and second island semiconductor layers; forming a gate insulation film in contact with the first and second island semiconductor layers; adding an impurity element of a conductivity type opposite to one conductivity type into a selected region of the second island semiconductor layer and forming a third impurity region; adding an impurity element of one conductivity type into a selected region of the first island semiconductor layer and forming a second impurity region; forming a first conductor layer in contact with the gate insulation film; forming a first gate electrode overlapping with the first island semiconductor layer and a second gate electrode overlapping with the second island semiconductor layer from the first conductor layer; and adding an impurity element of one conductivity type into a selected region of the first island semiconductor layer and forming a first impurity region.

A method of fabricating a semiconductor device according to still another embodiment of the present invention comprises the steps of: forming a semiconductor layer on a substrate having an insulation surface; removing a part of the semiconductor layer and forming at least first and second island semiconductor layers; forming a gate insulation film in contact with the first and second island semiconductor layers; adding an impurity element of a conductivity type opposite to one conductivity type into a selected region of the second island semiconductor layer and forming a third impurity region; adding an impurity element of one conductivity type into a selected region of the first island semiconductor layer and forming a first impurity region; adding an impurity element of one conductivity type into a selected region of the first island semiconductor layer and forming a second impurity region; forming a first conductor layer in such a fashion as to keep contact with the gate insulation film; and forming a first gate electrode overlapping with the first island semiconductor layer and a second gate electrode overlapping with the second island semiconductor layer from the first conductor layer.

A method of fabricating a semiconductor device according to still another embodiment of the present invention comprises the steps of: forming a semiconductor layer on a substrate having an insulation surface; removing a part of the semiconductor layer and forming at least first and second island semiconductor layers; forming a gate insulation film in contact with first and second island semiconductor layers; adding an impurity element of one conductivity type into a selected region of the first island semiconductor layer and forming a first impurity region; adding an impurity element of one conductivity type into a selected region of the first island semiconductor layer and forming a second impurity region; forming a first conductor layer in such a fashion as to keep contact with the gate insulation film; forming a second gate electrode overlapping with the second island semiconductor layer from the first conductor layer; adding an impurity element of a conductivity type opposite to one conductivity type into a selected region of the second island semiconductor layer and forming a third impurity region; and forming a first gate electrode overlapping with the first island semiconductor layer from the first conductor layer.

A method of fabricating a semiconductor device according to still another embodiment of the present invention comprises the steps of: forming a semiconductor layer on a substrate having an insulation surface; removing a part of the semiconductor layer and forming at least first and second island semiconductor layers; forming a gate insulation film in contact with the first and second island semiconductor layers; adding an impurity element of one conductivity type into a selected region of the first island semiconductor layer and forming a first impurity region; adding an impurity element of a conductivity type opposite to one conductivity type into a selected region of the second island semiconductor layer and forming a third impurity region; adding an impurity element of one conductivity type into a selected region of the first island semiconductor layer and forming a second impurity region; forming a first conductor layer in contact with the gate insulation film; and forming a first gate electrode overlapping with the first island semiconductor layer and a second gate electrode overlapping with the second island semiconductor layer from the first conductor layer.

In the construction of the present invention described above, the first conductor layer is preferably comprised of one or a plurality of elements selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W) and molybdenum (Mo), or a compound comprising at least one of these elements as the principal component.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view showing a fabrication process of a TFT;

Fig. 2 is a sectional view showing a fabrication process of a TFT and a plan view of a CMOS circuit;

Fig. 3 is a sectional view showing a fabrication process of a TFT;

Fig. 4 is a sectional view showing a fabrication process of a TFT and a plan view of a CMOS circuit;

Fig. 5 is a sectional view showing a fabrication process of a TFT;

Fig. 6 is a sectional view showing a fabrication process of a TFT;

Fig. 7 is a sectional view showing a fabrication process of a TFT;

Fig. 8 is a sectional view showing a fabrication process of a TFT;

Fig. 9 is a sectional view showing a fabrication process of a TFT;

Fig. 10 is a sectional view showing a fabrication process of a TFT;

Fig. 11 is a sectional view showing a fabrication process of an active matrix substrate;

Fig. 12 is a sectional view showing a fabrication process of an active matrix substrate;

Fig. 13 is a sectional view showing a fabrication process of an active matrix substrate;

Fig. 14 is a sectional view showing a fabrication process of a liquid crystal display device;

Fig. 15 is a sectional view of a liquid crystal display device;

Fig. 16 is a perspective view of an active matrix substrate;

Fig. 17 is a top view of an active matrix circuit;

Fig. 18 shows a fabrication process of a crystalline silicon film;

Fig. 19 shows a fabrication process of the crystalline silicon film;

Fig. 20 shows a fabrication process of the crystalline silicon film;

Fig. 21 shows a fabrication process of the crystalline silicon film;

Fig. 22 is a sectional view showing a fabrication process of a TFT;

Fig. 23 is a block circuit diagram of an active matrix liquid crystal display device according to one embodiment of the present invention;

Fig. 24 is a sectional view showing the

construction of the TFT according to the present invention;

Fig. 25 is a perspective view showing examples of a semiconductor device;

Fig. 26 is an explanatory view useful for explaining the relation between a gate electrode and an LDD region in the present invention;

Fig. 27 is a top view and a sectional view each showing the construction of an EL display device;

Fig. 28 is a sectional view of a pixel area of the EL display device;

Fig. 29 is a top view and a circuit diagram of the pixel area of the EL display device;

Fig. 30 is a sectional view of the pixel area of the EL display device;

Fig. 31 is a circuit diagram of the pixel area of the EL display device;

Fig. 32 is a graph showing an example of light transmission characteristics of an anti-ferromagnetic mixed liquid crystal;

Fig. 33 is a perspective view showing examples of a semiconductor device;

Fig. 34 is a perspective view showing examples of a semiconductor device;

Fig. 35 is a graph showing gate voltage (Vg)-v·-drain current (Id) characteristics; and

Fig. 36 is a graph showing the result of a DC bias stress test.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[Embodiment 1]

The first embodiment of the present invention will be explained with reference to Figs. 1 and 2. This embodiment represents the case where n-channel TFTs and p-channel TFTs are fabricated on the same substrate and an inverter circuit as the basic construction of a CMOS circuit is constituted.

The substrate 101 can use a glass substrate, a plastic substrate, a ceramic substrate, and so forth. A silicon substrate and a metal substrate typified by a stainless steel substrate having an insulation film such as a silicon oxide film, or a silicon nitride film, formed on the surface thereof can also be used. Needless to say, a quartz substrate can be used, too.

An underlying film 102 comprising a silicon nitride film and an underlying film 103 comprising a silicon oxide film are formed on the main plane of the substrate 101 on which the TFTs are to be formed. These underlying films are formed by plasma CVD or sputtering, and are disposed in order to prevent detrimental impurities from diffusing into the TFTs from the substrate 101. Therefore, an underlying film 102 comprising a silicon nitride film is formed into a thickness of 20 to 100 nm, typically 50 nm, and another underlying film 103 comprising the silicon oxide film is formed into a thickness of 50 to 500 nm, typically 150 to 200 nm.

Needless to say, the underlying film may comprise only either one of the underlying film 102 of the silicon nitride film and the underlying film 103 of the silicon oxide film, but a two-layered structure is most preferable in view of reliability of the resulting TFTs.

A semiconductor layer, that is so formed in contact with the underlying film 103, preferably uses a crystalline semiconductor that is obtained by first forming an amorphous semiconductor by a film formation method such as plasma CVD, vacuum CVD or sputtering, and then crystallizing it by laser annealing or a solid phase growing method by heat-treatment. A micro-crystal semiconductor formed by the film formation method described above can also be used. The semiconductor material that can be used in this case includes silicon (Si), germanium (Ge), a silicon germanium alloy, silicon carbide, and compound semiconductor materials such as gallium arsenic.

Alternatively, the semiconductor layer to be formed on the substrate 101 may be an SOI (Silicon-On-Insulator) substrate having a single crystal silicon layer formed thereon. Several kinds of the structures of the SOI substrate, and the method of fabricating the same, are known. Typically, SIMOX (Separation by Implanted Oxygen), ELTRAN

(Epitaxial Layer Transfer: a registered trade name of Canon Co.) substrate, Smart-Cut (a registered trade name of SOITEC Co.) can be used. Other SOI substrates can be used naturally.

The semiconductor layer is formed into a thickness of 10 to 100 nm, typically 50 nm. The amorphous semiconductor film formed by plasma CVD contains about 10 to about 40 atom% of hydrogen in the film. It is therefore preferable to conduct heat-treatment at 400 to 500° C prior to the crystallization process so that hydrogen can dissociate from the film and the hydrogen content is not more than 5 atom%. Though the amorphous silicon film may be formed by other formation methods such as sputtering or vacuum deposition, impurity elements contained in the film such as oxygen and nitrogen are preferably reduced sufficiently.

Because the underlying films and the amorphous semiconductor film can be formed by the same film formation method, it is advisable to continuously form the underlying film 102, the underlying film 103 and the semiconductor layer. Because its surface is not exposed to the atmosphere after each of these films is formed, surface contamination can be prevented. As a result, one of the factors that cause variation of TFT performance can be obviated.

A known laser annealing technology or a known heat annealing technology may be employed in order to crystallize the amorphous semiconductor film. The crystalline semiconductor film can be used when the heat annealing technology using a catalytic element is employed. Furthermore, excellent TFT performance can be obtained by applying gettering and removing the catalytic element, after forming crystalline semiconductor film by the heat annealing technology using the catalytic element.

The crystalline semiconductor film so formed is patterned by a known patterning process using a first photo-mask to form a resist mask, and a second island semiconductor layer 104 and a first island semiconductor layer 105 are formed by dry etching.

Next, a gate insulation film 106 consisting of silicon oxide or silicon nitride as a principal component is formed on the surface of the second island semiconductor layer 104 and on the surface of the first island semiconductor layer 105. This gate insulation film 106 is formed by plasma CVD or sputtering to a thickness of 10 to 200 nm, preferably 50 to 150 nm (see Fig. 1(A)).

Resist masks 107 and 108 to cover the channel formation regions of the second and first island semiconductor layers 104 and 105 are formed with a second photo-mask. At this time, a resist mask 109 may be formed in a region in which wiring is to be made.

A process step for forming a second impurity region is carried out by adding an impurity element for imparting the n type. Phosphorus (P), arsenic (As) and antimony (Sb) are known as the impurity elements that impart the n type conductivity to the crystalline semiconductor material, but phosphorus is used here and added by ion doping using phosphine (PH_3). In this process step, an acceleration voltage is set to a rather high level of 80 keV in order to add phosphorus into the semiconductor layer below the gate insulation film 106 through this film 106. The concentration of P doped into the semiconductor layer is preferably within the range of 1×10^{16} to 1×10^{19} atoms/cm^3, and is 1×10^{18} atoms/cm^3 in this case. In this way, regions 110 and 111 in which P is doped into the semiconductor layer are formed. A part of the second impurity region formed in this process functions as the LDD region (Fig. 1(B)).

An alkaline peeling solution that is commercially available may be used in order to remove the resist mask, but the resist mask can be effectively removed by ashing. Ashing is the method in which plasma is generated in an oxidizing atmosphere, and exposes and removes the cured resist. It can be carried out effectively when steam is added to the atmosphere besides oxygen.

The first conductor layer 112 is formed on the surface of the gate insulation film 106. This first conductor layer 112 is formed from a conductive material selected from the group consisting of Ta, Ti, Mo and W as the principal component. The first conductor layer 107 is formed preferably to a thickness of 10 to 100 nm, more preferably 150 to 400 nm (Fig. 1(C)).

Compounds such as WMo, TaN, MoTa or WSi_x ($x = 2.4 < x < 2.7$), for example, can be used.

The conductive materials such as Ta, Ti, Mo and W have higher resistivity than Al and Cu. However, they can be used without any problem up to about 100 cm^2 in connection with the area of the circuit to be fabricated.

Next, resist masks 113, 114, 115 and 116 are formed using a third photo-mask. The resist mask 113 is for forming the gate electrode of a p-channel TFT, and the resist masks 115 and 116 are for forming gate wiring and gate bus line. The resist mask 114 is so formed as to cover the entire surface of the first island semiconductor layer, and functions as a mask for preventing impurities from being added in the next process step.

Unnecessary portions of the first conductor layer are etched away by drying etching, giving a second gate electrode 117, a gate wiring 119 and a gate bus line 120. Here, ashing is preferably carried out if any etching residues remain.

Next, a process step for forming a third impurity region is carried out by adding an impurity element for imparting the p type to a part of the second island semiconductor layer 104, in which the p-channel TFT is to be formed, while the resist masks 113, 114, 115 and 116 are left as such. Boron (B), aluminum (Al) and gallium (Ga) are known as the impurity element for imparting the p type. This embodiment selects boron (B) and adds it by ion doping that uses diborane (B_2H_6). The acceleration voltage is also 80 keV and boron is doped in a dose of 2×10^{20} atoms/cm^3. In this way, third impurity regions 121 and 122 doped with boron in a high concentration are formed as shown in Fig. 1(D).

After the resist mask formed in Fig. 1(D) is removed, resist masks 123, 124 and 125 are formed using a fourth photo-mask. The fourth photo-mask is for forming the gate electrode of the n-channel TFT, and the first gate electrode 126 is formed by dry etching. At this time, the first gate electrode 126 is formed in such a fashion as to overlap with a part of the second impurity regions 110 and 111 through the gate insulation film (Fig. 1(E)).

After the resist masks 123, 124 and 125 are removed completely, resist masks 129, 130 and 131 are formed using a fifth photo-mask. The resist mask 130 is formed in such a fashion as to cover the first gate electrode 126 and to overlap with a part of the second impurity regions 110 and 111. The resist mask 130 decides the offset quantity of the LDD region.

The surface of the semiconductor layer where the first impurity region is formed may be exposed by removing a part of the gate insulation film by using this resist mask 130. This arrangement makes it possible to effectively conduct the process step of adding the impurity element for imparting the n conductivity type to be executed in the next step.

The process step of forming the first impurity region by adding the impurity element for imparting the n conductivity type is then carried out. There are formed a first impurity region 132 to serve as the source region and a first impurity region 133 to serve as the drain region. Ion doping using phosphine (PH_3) is used in this case. In this process step, too, the acceleration voltage is set to a rather high level of 80 keV in order to dope phosphorus into the semiconductor layer below the gate insulation film 106 through this film 106. In comparison with the process step of adding the first impurity element for imparting the n conductivity type, the P concentration of this region is higher, and is preferably from 1×10^{19} to 1×10^{21} atoms/cm^3. The concentration of 1×10^{20} atoms/cm^3 is used in this embodiment (Fig. 2(A)).

First inter-layer insulation films 134 and 135 are then formed on the surface of each of the gate insulation film 106, the first and second gate electrodes 126 and 117, the gate wiring 127 and the gate bus line 128. The first inter-layer insulation film 134 is a silicon nitride film and is formed to a thickness of 50 nm. The first inter-layer insulation film 135 is a silicon oxide film and is formed to a thickness of

950 nm.

The first inter-layer insulation film 134 comprising silicon nitride film formed here is necessary for conducting the heat-treatment in the next process step. This is effective for preventing the surface of each of the first and second gate electrodes 126 and 117, the gate wiring 127 and the gate bus line 128 from being oxidized.

The heat-treatment step is necessary for activating the impurity elements doped in the respective concentrations to impart the n and p type conductivities. This step may use heat annealing using an electric heating furnace, laser annealing using the excimer laser described above, or rapid thermal annealing (RTA) using a halogen lamp. Though laser annealing can execute activation at a low substrate heating temperature, the method cannot easily activate the regions hidden beneath the gate electrode. Therefore, this embodiment uses heat annealing for activation. The heat-treatment is carried out at 300 to 700° C, preferably 350 to 550° C, in a nitrogen atmosphere. In this embodiment, it is carried out at 450° C for 2 hours.

In this heat-treatment step, 3 to 90% of hydrogen may be added to the nitrogen atmosphere. It is advisable to carry out a hydrogenation treatment in a 3 to 100% hydrogen atmosphere at 150 to 500° C, preferably 300 to 450° C, for 2 to 12 hours. A hydrogen plasma treatment at a substrate temperature of 150 to 500° C, preferably 200 to 450° C, may be carried out, as well. In any case, hydrogen compensates for defect remaining in the semiconductor layer and on its interface, and can improve TFT performance.

After a predetermined resist mask is formed using a sixth photo-mask, the first inter-layer insulation films 134 and 135 are etched to form contact holes reaching the source and drain regions of the respective TFTs. The second conductor layer is formed, and then the source electrodes 136 and 137 and the drain electrode 138 are formed by patterning with a seventh photo-mask. This embodiment uses, as the second conductor layer of this electrode, the electrode having a three-layered structure comprising a Ti film of 100 nm, a Ti-containing Al film of 300 nm and a Ti film of 150 nm that are formed continuously by sputtering.

As a result of the process steps described above, the p-channel TFTs are formed in the self-alignment configuration, whereas the n-channel TFTs are formed in the non-self-alignment configuration.

A channel formation region 142, first impurity regions 145 and 146 and second impurity regions 143 and 144 are formed in the n-channel TFTs of the CMOS circuit. Here, a second impurity region includes a region (GOLD region) 143a, 144a that overlaps with the gate electrode and a region (LDD region) 143b, 144b that does not. The first impurity region

145 functions as the source region and the first impurity region 146, as the drain region.

On the other hand, a channel formation region 139 and third impurity regions 140 and 141 are formed in the p-channel TFTs. The third impurity region 140 functions as the source region and the third impurity region 141, as the drain region (Fig. 2(B)).

Fig. 2(C) is a top view of an inverter circuit. In the drawing, the sectional structure taken along a line A - A' of the TFT portion, the B - B' sectional structure of the gate wiring portion and the C - C' sectional structure of the gate bus line portion correspond to those of Fig. 2(B), respectively. In the present invention, the gate electrode, the gate wiring and the gate bus line comprise the first conductor layer.

Figs. 1 and 2 typically show the CMOS circuit formed by complementarily combining the n-channel TFTs and the p-channel TFTs by way of example. However, the present invention can be applied to an NMOS circuit using the n-channel TFTs or to the pixel area of the liquid display device.

[Embodiment 2]

Another embodiment will be explained with reference to Figs. 3 and 4. This embodiment represents the formation of an inverter circuit as the basic construction of a CMOS circuit by forming the n-channel TFTs and the p-channel

TFTs on the same substrate.

An underlying film 302 comprising a silicon nitride film, and then an underlying film 303 comprising a silicon oxide film, a first island semiconductor layer 305, a second island semiconductor layer 304 and a gate insulation film 306 are formed first on a substrate 301 in the same way as in the first embodiment (Fig. 3(A)).

Resist masks 307 and 308 that cover the channel formation regions of the second and first island semiconductor layers 304 and 305, are formed using a second photo-mask. At this time, a resist mask 309 may be formed in the wiring formation region, too.

A process step of forming a second impurity region is carried out by adding an impurity element for imparting the n type conductivity. This embodiment employs ion doping of phosphorus using phosphine (PH_3). The P concentration doped into the first island semiconductor layer 305 is preferably within the range of 1×10^{16} to 1×10^{19} atoms/cm^3, and this embodiment uses the P concentration of 1×10^{18} atoms/cm^3. P-doped regions 310 and 311 are thus formed in the semiconductor layer. A part of the resulting second impurity region is to function as the LDD region (Fig. 3(B)).

Next, a first conductor layer 312 is formed on the surface of the gate insulation film 306. The first conductor layer 312 uses a conductive material selected from the group consisting of Ta, Ti, Mo and W as the principal component. The thickness of this first conductor layer 312 is 100 to 1,000 nm, preferably 150 to 400 nm (Fig. 3(C)).

Resist masks 313, 314, 315 and 316 are then formed using a third photo-mask. A part of the first conductor layer 312 is etched away by dry etching using the resist masks, forming thereby a first gate electrode 318, a second gate electrode 317, a gate wiring 319 and a gate bus line 320 (Fig. 3(D)).

After the resist masks 313, 314, 315 and 316 are completely removed, resist masks 321, 322 and 323 are formed using a fourth photo-mask. The resist mask 322 is formed in such a fashion as to cover the first gate electrode 318 and to overlap with a part of the second impurity regions 310 and 311. The resist mask 322 decides the offset quantity of the LDD region.

A process step of forming the first impurity region is carried out by adding an impurity element for imparting the n type conductivity. There are thus formed the first impurity region 325 to function as the source region and the first impurity region 324 to function as the drain region. This embodiment employs ion doping of P using phosphine (PH_3). In this process step, too, the acceleration voltage is set to a rather high level of 80 keV in order to dope phosphorus into the semiconductor layer beneath the gate insulation film 106 through this film 106. The P concentration of this region is preferably 1 x 10^{19} to 1 x 10^{21} atoms/cm^3. This embodiment uses the P concentration of 1 x 10^{20} atoms/cm^3 (Fig. 3(E)).

Next, resist masks 326, 327 and 328 are formed using a fifth photo-mask. A process step of forming a third impurity region is carried out by adding an impurity element for imparting the p type conductivity to a part of a second island semiconductor layer 304 in which p-channel TFTs are formed. This embodiment uses boron as the impurity element and conducts ion doping using diborane (B_2H_6). The acceleration voltage is set to 80 keV, too, in order to dope boron in a concentration of 2 x 10^{20} atoms/cm^3. There are thus formed third impurity regions 329 and 330 doped with boron in a high concentration as shown in Fig. 4(A).

First inter-layer insulation films 329 and 330 are formed over the surface of the gate insulation film 306, the first and second gate electrodes 318 and 317, the gate wiring 319 and the gate bus line 320. The first inter-layer insulation film 329 is a silicon nitride film and is formed to a thickness of 50 nm. The first inter-layer insulation film 330 is a silicon oxide film and is formed to a thickness of 950 nm.

Subsequently, the heat-treatment step is carried out in the same way as in the Embodiment 1 to form source electrodes 331 and 332 and the drain electrode 333, and a channel formation region 337, first impurity regions 340 and

341 and second impurity regions 338 and 339 are formed in n-channel TFTs of a CMOS circuit. Here, regions (GOLD regions) 338a and 339a overlapping with the gate electrode and regions (LDD regions) 338b and 339b not overlapping the gate electrode are formed in the second impurity region. The first impurity region 340 functions as the source region and the first impurity region 341 functions as the drain region.

On the other hand, a channel formation region 334, a third impurity region 335 to function as the source region and a third impurity region 336 to function as the drain region are formed in the p-channel TFT (Fig. 4(B)).

Fig. 4(C) is a top view of an inverter circuit. The A - A′ sectional structure of the TFT portion, the B - B′ sectional structure of the gate wiring portion and the C - C′ sectional structure of the gate bus line portion correspond to those shown in Fig. 4(B), respectively. In the present invention, the gate electrode, the gate wiring and the gate bus line are comprised of the first conductor layer.

Figs. 3 and 4 show a CMOS circuit comprising a complementary combination of n-channel TFTs and p-channel TFTs by way of example, but the present invention can be applied also to an NMOS circuit using the n-channel TFTs and to a pixel area of a liquid crystal display device.

[Embodiment 3]

The construction of the TFTs according to the present invention will be explained in further detail with reference to Fig. 26. Each reference numeral in Fig. 26 corresponds to the one used in Figs. 1 and 2. The second impurity region as the LDD region can be divided into the second impurity region 143a overlapping with the first gate electrode 126 and the second impurity region 143b not overlapping with the gate electrode 126. In other words, there are formed the LDD region (Lov) overlapping with the gate electrode and the LDD region (Loff) not overlapping with the gate electrode.

The lengths of Lov and Loff in the LDD regions can be easily determined by using three photo-masks as represented in Embodiment 1. In the process step of Embodiment 1, the resist mask is formed using the second photo-mask and the second impurity region is formed by the doping step that imparts the n-type conductivity. A part of this region functions as the LDD region. The first gate electrode is formed using the fourth photo-mask, and the overlapping region (Lov) of the LDD is formed at this time. Furthermore, the LDD region (Loff) is formed using the resist mask that is formed using the fifth photo-mask.

The three photo-masks described are directed to form the resist masks in the doping step and in addition, they are the masks for patterning the gate electrode. They have both of these functions.

Therefore, design freedom can be given to the lengths of Lov and Loff, and the lengths can be set arbitrarily in conjunction with the size of the TFTs to be fabricated. This method has been extremely advantageous when TFTs having mutually different driving voltages are fabricated for respective functional circuits in the large area integrated circuit. Fig. 26 shows an example of design values of the TFTs used in the logic circuit portion, the buffer circuit portion, the analog switch portion and the pixel area of the active matrix liquid crystal display device, by way of example. At this time, not only the channel length but also the length of each of the second impurity region 143a overlapping the gate electrode and the second impurity region 143b not overlapping with the gate electrode can be set appropriately in consideration of the driving voltages of the respective TFTs.

The ON characteristics of the TFTs of the shift register circuit of the driver circuit of the liquid crystal display device and of the TFTs of the buffer circuit are basically of importance. Therefore, the second impurity region 143b not overlapping with the gate electrode is not always necessary to be disposed so long as only the so-called "GOLD structure" is disposed. When it is disposed, however, the Loff value may be set to the range of 0.5 to 3 μm in consideration of the driving voltages. When the withstand voltage is taken into consideration, the value of the second impurity region 143b not overlapping with the gate electrode is preferably greater as the driving voltage becomes higher.

In order to prevent the increase of the OFF current of the TFTs disposed in the sample circuit or in the pixel unit, the length of the second impurity region 143a may be set to 1.5 μm and the length of the second impurity region 143b not overlapping with the gate electrode, to 1.5 μm, when the channel length is 3 μm. Needless to say, the present invention is not specifically limited to these design values but may select appropriate design values.

On the other hand, only the channel formation region, the source region and the drain region may be formed in the p-channel TFT. Though the structure similar to that of the n-channel TFT may be used, it is more preferred to secure the ON current and to keep the balance of performance with the n-channel TFT because the p-channel TFT has high reliability from the outset. When the present invention is applied to the CMOS circuit as shown in Fig. 1, this balance of performance is of utmost importance. However, no problem develops when the construction of the present invention is applied to the p-channel TFT.

[Embodiment 4]

The fourth embodiment of the present invention will be explained with reference to Fig. 5. The explanation is given on the embodiment in which the n-channel TFTs and the p-channel TFTs are fabricated on the same substrate to form the inverter circuit as the basic construction of the CMOS circuit.

To begin with, the substrate under the state shown in Fig. 1(A) is formed in the same way as in Embodiment 1. Resist masks 501, 502 and 503 are formed using the second photo-mask.

The process step for forming the third impurity region is conducted by adding an impurity element that imparts the p type conductivity. Here, boron is the impurity element, and ion doping is carried out using diborane (B_2H_6). The acceleration voltage is 80 keV, too, and boron is doped in a dose of 2 x 10^{20} atoms/cm^3. There are thus formed the third impurity regions 504 and 505 doped with boron in a high concentration.

Resist masks 506, 507 and 508 are formed using the third photo-mask, and the process step for forming the second impurity region is conducted by doping an impurity element for imparting the n type conductivity to a selected region of the first island semiconductor layer. Here, phosphorus is used as the impurity element, and ion doping is conducted using phosphine (PH_3). The concentration of phosphorus added here is preferably within the range of 1 x 10^{16} to 1 x 10^{19} atoms/cm^3, and a dose of 1 x 10^{18} atoms/cm^3 is employed. There are thus formed phosphorus-doped regions 509 and 510 in the semiconductor layer. A part of the resulting second impurity region functions as the LDD region (Fig. 5(B)).

The first conductor layer 511 is formed on the surface of the gate insulation film 106 using a conductive material consisting of the element selected from Ta, Ti, Mo and W as the principal component. The first conductor layer 511 is formed to a thickness of 100 to 1,000 nm, preferably 150 to 400 nm (Fig. 5(C)).

Next, resist masks 512, 513, 514 and 515 are formed using the fourth photo-mask. A part of the first conductor layer 511 is etched away by dry etching using the resist masks, thereby forming the first gate electrode 517, the second gate electrode 516, the gate wiring 518 and the gate bus line 519 (Fig. 5(D)).

Resist masks 520, 521 and 522 are formed using the fifth photo-mask. The resist mask 521 is formed in such a fashion as to cover the first gate electrode 517 and to partially overlap with the second impurity regions 509 and 510. The resist mask 521 determines the offset amount of the LDD region.

The process step for forming the first impurity region by adding an n-type imparting impurity element is conducted. There are thus formed the first impurity region 524 to function as the source region and the first impurity region 523 to function as the drain region. Here, ion doping using phosphine (PH_3) is employed. The P concentration in this region is preferably within the range of 1 x 10^{19} to 1 x 10^{21} atoms/cm^3, and is 1 x 10^{20} atoms/cm^3 (Fig. 5(E)) in this case.

Subsequently, the heat-treatment step is conducted in the same way as in Embodiment 1, and the source electrodes 527 and 528 and the drain electrode 529 are formed. The channel formation region 533, the first impurity regions 536 and 537 and the second impurity regions 534 and 535 are formed in the n-channel TFTs of the CMOS circuit. Here, the regions (GOLD region) 534a and 535a overlapping the gate electrode and the regions (LDD region) 534b and 535b not overlapping with the gate electrode are formed in the second impurity region. The first impurity region 536 functions as the source region and the first impurity region 537, as the drain region. On the other hand, the channel formation region 530, the third impurity region 531 to function as the source region and the third impurity region 532 to function as the drain region are formed in the p-channel TFT (Fig. 5(F)).

[Embodiment 5]

The fifth embodiment of the present invention will be explained with reference to Fig. 6. The explanation is given on the embodiment in which the n-channel TFTs and the p-channel TFTs are fabricated on the same substrate to form the inverter circuit as the basic construction of the CMOS circuit.

To begin with, the substrate under the state shown in Fig. 1(A) is formed in the same way as in Embodiment 1.

Resist masks 601, 602 and 603 are formed using the second photo-mask.

The process step for forming the third impurity region by adding a p type conductivity imparting impurity element is conducted. Here, boron is the impurity element, and ion doping is conducted using diborane (B_2H_6). The acceleration voltage is 80 keV and boron is doped in a dose of 2×10^{20} atoms/cm^3. There are thus formed the third impurity regions 604 and 605 doped with boron in a high concentration as shown in Fig. 6(A).

Resist masks 606, 607 and 608 are formed using the third photo-mask. The process step for forming the first impurity region by adding the n type conductivity imparting impurity element is conducted into the first island semiconductor layer 105. There are thus formed the first impurity region 610 to function as the source region and the first impurity region 609 to function as the drain region. Here, ion doping using phosphine (PH_3) is conducted. The phosphorus concentration in this region is preferably within the range of 1×10^{19} to 1×10^{21} atoms/cm^3, and it is 1×10^{20} atoms/cm^3 in this case (Fig. 6(B)).

Next, resist masks 611, 612 and 613 are formed using the fourth photo-mask, and the process step for forming the second impurity region by adding the n type imparting impurity element to a selected region of the first island semiconductor layer 105 is conducted. Here, phosphorus is used as the impurity element and ion doping is conducted using phosphine (PH_3). The P concentration added here is preferably within the range of 1×10^{16} to 1×10^{19} atoms/cm^3, and it is 1×10^{18} atoms/cm^3 in this case. There are thus formed phosphorus-doped regions 614 and 615 in the semiconductor layer. A part of the second impurity region formed here functions as the LDD region (Fig. 6(C)).

The first conductor layer 616 is formed on the surface of the gate insulation film 106 using a conductive material containing the element selected from Ta, Ti, Mo and W as the principal component. The first conductor layer 616 may be formed to a thickness of 100 to 1,000 nm, preferably 150 to 400 nm (Fig. 6(D)).

Next, resist masks 617, 618, 619 and 620 are formed using the fifth photo-mask. A part of the first conductor layer 616 is etched away by dry etching, forming the first gate electrode 622, the second gate electrode 621, the gate wiring 623 and the gate bus line 624 (Fig. 6(E)).

Subsequently, the heat-treatment step is conducted in the same way as in Embodiment 1, and the source electrodes 627 and 628 and the drain electrode 629 are formed. The channel formation region 633, the first impurity regions 636 and 637 and the second impurity regions 634 and 635 are formed in the n-channel TFTs of the CMOS circuit. The regions

(GOLD region) 634a and 635a overlapping with the gate electrode and the regions (LDD region) 634b and 635b not overlapping with the gate electrode are formed in the second impurity region. The first impurity region 636 functions as the source region and the first impurity region 637 functions as the drain region. On the other hand, the channel formation region 630, the third impurity region 631 to function as the source region and the third impurity region 632 to function as the drain region are formed in the p-channel TFT (Fig. 6(F)).

[Embodiment 6]

The sixth embodiment will be explained with reference to Fig. 7. Here, the explanation is given on the embodiment in which the n-channel TFTs and the p-channel TFTs are fabricated on the same substrate to form the inverter circuit as the basic construction of the CMOS circuit.

To begin with, the substrate under the state shown in Fig. 1(A) is formed in the same way as in Embodiment 1. Resist masks 701, 702 and 703 are formed using the second photo-mask.

First, the n type imparting impurity element is selectively added to the first island semiconductor layer 105 to form the first impurity region. Ion doping using phosphine (PH_3) is conducted in this case. The P concentration of this region is preferably 1×10^{19} to 1×10^{21} atoms/cm^3, and it is 1×10^{20} atoms/cm^3 in this case. There are thus formed the regions 704 and 705 doped with P into the semiconductor layer (Fig. 7(A)).

Next, resist masks 706, 707 and 708 are formed using the third photo-mask. The process step for forming the second impurity region by adding the n type imparting impurity element to the selected region of the first island semiconductor layer is conducted. Here, the concentration of phosphorus is preferably within the range of 1 x 10^{16} to 1 x 10^{19} atoms/cm^3, and typically 1 x 10^{18} atoms/cm^3. There are thus formed the regions 709 and 710 containing phosphorus doped into the semiconductor layer. A part of the second impurity region formed hereby functions as the LDD region (Fig. 7(B)).

The first conductor layer 711 is formed on the surface of the gate insulation film 106 using the element selected from Ta, Ti, Mo and W as the principal component. The thickness of the first conductor layer 711 is 100 to 1,000 nm, preferably 150 to 400 nm (Fig. 7(C)).

Next, the resist masks 712, 713 and 714 are formed using the fourth photo-mask. The resist mask 712 is to form the second gate electrode. The resist mask 713 is formed in such a fashion as to cover the entire surface of the first island semiconductor layer and to function as the mask for preventing the addition of the impurity in the following step.

The unnecessary portions of the first conductor layer are etched away by dry etching, forming the second gate electrode 715. The process step for forming the third impurity region by adding the p-type imparting impurity element to a part of the second island semiconductor layer 104 for forming the p-channel TFT is conducted. The p-type imparting impurity element is boron, and is added in a dose of 2×10^{20} atoms/cm^3. There are thus formed the third impurity regions 718 and 719 containing boron in a high concentration as shown in Fig. 7(D).

Next, the resist masks 718, 719, 720 and 721 are formed using the fifth photo-mask. A part of the first conductor layer 716 and 717 is etched away by dry etching, forming the first gate electrode 722, the gate wiring 723 and the gate bus line 721 (Fig. 7(E)).

Subsequently, in the same way as in Embodiment 1, the heat-treatment step is conducted and the source electrodes 727 and 728 and the drain electrode 729 are formed. The channel formation region 733, the first impurity region 736 and 737 and the second impurity regions 734 and 735 are formed in the n-channel TFT of the CMOS circuit. Here, the regions (GOLD region) 734a and 735a overlapping with the gate electrode and the regions (LDD region) 734b and 735b not overlapping with the gate electrode are formed in the second impurity regions, respectively. The first impurity region 736 functions as the source region and the first impurity region 737 functions as the drain region. On the other hand, the channel formation region 730, the third impurity region 731 to function as the source region and the third impurity region 732 to function as the drain region are formed in the p-channel TFT (Fig. 7(F)).

[Embodiment 7]

To begin with, the substrate under the state shown in Fig. 1(A) is formed in the same way as in Embodiment 1. Resist masks 801, 802 and 803 are formed using the second photo-mask.

The first impurity region is first formed by selectively adding the n-type imparting impurity element to the first island semiconductor layer 105. Here, ion doping using phosphine (PH_3) is employed. The P concentration in this region is preferably 1×10^{19} to 1×10^{21} atoms/cm^3, and it is 1×10^{20} atoms/cm^3 in this case. There are thus formed regions doped with phosphorus 804 and 805 in the semiconductor layer (Fig. 8(A)).

Next, the resist masks 806, 807 and 808 are formed using the third photo-mask, and the process step for forming the third impurity region by adding the p-type imparting impurity element is conducted. Here, boron is the impurity element, and ion doping is conducted using diborane (B_2H_6). The acceleration voltage is 80 keV in this case, too, and boron is added in a dose of 2×10^{20} atoms/cm^3. There are thus formed the third impurity regions 809 and 810 doped with boron in a high concentration as shown in Fig. 8(B).

Next, the resist masks 811, 812 and 813 are formed using the third photo-mask. The process step for forming the second impurity region is conducted by adding the n-type imparting impurity element into a selected region of the first island semiconductor layer. Here, phosphorus is used, and ion doping using phosphine (PH_3) is conducted. The dose of phosphorus in this case is preferably within the range of 1×10^{16} to 1×10^{19} atoms/cm^3, and it is 1×10^{18} atoms/cm^3. There are thus formed the regions 814 and 815 containing phosphorus in the semiconductor layer. A part of the resulting second impurity regions functions as the LDD region (Fig. 8(C)).

The first conductor layer 816 is formed on the surface of the gate insulation film 106 using a conductive material containing the element selected from Ta, Ti, Mo and W as the principal component. The first conductor layer 816 may be formed to a thickness of 100 to 1,000 nm, preferably 150 to 400 nm (Fig. 8(C)).

Next, the resist masks 817, 818, 819 and 820 are formed using the fourth photo-mask. A part of the first conductor layer 816 is etched away by dry etchin using the resist masks, forming the first gate electrode 822, the second gate electrode 821, the gate wiring 823 and the gate bus line 824 (Fig. 8(E)).

Subsequently, in the same way as in Embodiment 1, the heat-treatment step is conducted and the source electrodes 827 and 828 and the drain electrode 829 are formed. The channel formation region 833, the first impurity regions 836 and 837 and the second impurity regions 834 and 835 are formed in the n-channel TFT of the CMOS circuit. Here, the regions (GOLD region) 834a and 835a overlapping with the gate electrode and the regions (LDD regions) 834b and 835b not overlapping with the gate electrode are formed in the second impurity regions, respectively. The first impurity region 836 functions as the source region and the first impurity region 837, as the drain region. On the other hand, the channel formation region 830, the third impurity region 831 to function as the source region and the third impurity region 832 to function as the drain region are formed in the p-channel TFT (Fig. 8(F)).

[Embodiment 8]

To begin with, the state shown in Fig. 1(E) is obtained in the same way as in Embodiment 1. Next, the resist masks 901, 902 and 903 are formed as shown in Fig. 9(A). The resist mask 902 is formed in such a fashion as to cover the first gate electrode 126 of the n-channel TFT and a part of the second impurity region, and is used for forming the LDD. Here, the resist mask 902 is formed only on the drain side of the n-channel TFT. The LDD prevents the increase of the leakage current, and a sufficient effect can be obtained by disposing it only on the drain side (Fig. 9(A)).

The subsequent process steps are conducted in the same way as in Embodiment 1, forming the CMOS circuit shown in Fig. 9(B). The channel formation region 914, the first impurity regions 917 and 918 and the second impurity regions 915 and 916 are formed in the n-channel TFT. Here, the region (GOLD region) 916 overlapping with the first gate electrode and the region (LDD region) 916b not overlapping with the first gate electrode are formed in the second impurity region 916. The first impurity region 917 functions as the source region and the first impurity region 918, as the drain region.

[Embodiment 9]

This embodiment will be explained with reference to Fig. 10. To begin with, the state shown in Fig. 5(C) is obtained in the same way as in Embodiment 1.

The resist masks 1012, 1013, 1014 and 1015 are formed using a photo-mask, and a part of the first conductor layer 511 is etched away by dry etching. Thereafter, by using this resist mask, the second doping process for imparting the n-type is conducted to form the regions 1010, 1011, 1020 and 1021 containing phosphorus doped into the semiconductor layers 104 and 105 (Fig. 10(A)).

Here, the resist masks are completely removed by ashing and an alkaline peeling solution. A photo-resist film is formed again, and the patterning process is conducted by the exposure from the back. In this case, the patterns of the gate electrode, the gate wiring and the gate bus line exhibit the same function as that of the photo-mask, and the resist masks 1022, 1023, 1024 and 1025 are formed on the respective patterns. The exposure from the back is effected by using direct light and scattered light, and the resist masks can be formed inside and on the gate electrode as shown in Fig. 10(B) when the exposure condition such as the light intensity, the exposure time, and so forth, is adjusted.

The first gate electrode 1002, the second gate electrode 1001, the gate wiring 1003 and the gate bus line 1004 are formed by etching away a part of the gate electrode, the gate wiring and the gate bus line by dry etching.

Subsequently, the process steps are conducted in the same way as in Embodiment 5, forming the CMOS circuit shown in Fig. 10(C). The channel formation region 1034, the first impurity regions 1037 and 1038 and the second impurity regions 1035 and 1036 are formed in the n-channel TFT. Here, the regions (GOLD regions) 1035a and 1036a overlapping with the first gate electrode and the regions (LDD regions) 1035b and 1036b not overlapping with the first gate electrode are formed in the second impurity regions. The first impurity region 1037 functions as the source region and the first impurity region 1038, as the drain region.

[Examples]

[Example 1]

In this example, the construction of the present invention and the method of simultaneously fabricating the pixel area and the CMOS circuit, which is the basic form of the driving circuit to be disposed round the pixel area, will be explained with reference to Figs. 11 to 13.

In Fig. 11, an alkali-free glass substrate typified by "Corning 1737 glass" substrate is used for a substrate 1101. An underlying layer 1102 is formed on the surface of the substrate 1101, on which TFTs are to be formed, by plasma CVD or sputtering. A silicon nitride film and a silicon oxide film are formed to a thickness of 50 nm (generally 25 to 100 nm) and 150 nm (generally 50 to 300 nm), respectively, as the underlying layer 1102, though the films are not shown in the drawing. The underlying layer 1102 may use only the silicon nitride film or the silicon nitride oxide film.

Besides the materials described above, the underlying layer 1102 may have a two-layered structure in which a first silicon oxide nitride film is formed from SiH_4, NH_3 and N_2O to a thickness of 10 to 100 nm, and a second silicon oxide nitride film is formed from SiH_4 and N_2O on the former to a thickness of 100 to 200 nm.

The first silicon oxide nitride film is formed by parallel flat sheet type plasma CVD. This silicon oxide nitride film is formed by the steps of introducing SiH_4 at 10 sccm, NH_3 at 100 sccm and N_2O at 20 sccm into a reaction chamber, and setting a substrate temperature to 325° C, a reaction pressure to 40 Pa, a discharge power density to 0.41 W/cm^2 and a discharge frequency to 60 MHz. On the other hand, the second silicon oxide nitride film is formed by the steps of introducing SiH_4 at 4 sccm and N_2O at 400 sccm into the reaction chamber, and setting the substrate temperature to 400° C, the reaction pressure to 40 Pa, the discharge power density to 0.41 W/cm^2 and the discharge frequency to 60 MHz. These films can be formed continuously only by changing the substrate temperature and switching the reaction gas. The first silicon oxide nitride film is formed so that the internal stress functions as the tensile stress as the substrate is considered as the center. The second silicon oxide nitride film is also provided with the internal stress in the same direction. However, the stress of the second silicon oxide nitride film may be formed so that the absolute value of its internal stress is smaller than that of the first silicon oxide nitride film.

Next, a 50 nm-thick amorphous silicon film is formed by plasma CVD on the underlying layer 1102. Though depending on the hydrogen content, a dehydrogenation heat-treatment is conducted preferably at 400 to 550° C for several hours. It is preferred to carry out crystallization after the hydrogen content is decreased to 5 atom% or below in this way, a crystallization step is carried out. Though the amorphous silicon film may be formed by other fabrication methods such as sputtering or vacuum deposition, impurity elements contained in the film such as oxygen and nitrogen are preferably lowered sufficiently.

Here, both the underlying layer and the amorphous silicon film are formed here by plasma CVD, and they may be formed continuously in this case in vacuum. If the process step that inhibits the exposure of the underlying film to the atmospheric air after it is formed is employed, surface contamination can be prevented, and variance of performance of the resulting TFTs can be decreased.

The crystallization step of the amorphous silicon film may use known laser annealing or thermal annealing. In this example, a crystalline silicon film is formed by condensing a pulse oscillation type KrF excimer laser beam into a linear shape and radiating it to the amorphous silicon film.

Incidentally, though this example forms the crystalline silicon film from the amorphous silicon film, a micro-crystalline silicon film may be used, or a crystalline silicon film may be formed directly.

The crystalline silicon film so formed is patterned using a first photo-mask, giving island semiconductor layers 1103, 1104 and 1105.

Next, a gate insulation film 1106 consisting of silicon oxide or silicon nitride as the principal component is formed in such a fashion as to cover the island semiconductor layers 1103, 1104 and 1105. A silicon nitride oxide film using N_2O and SiH_4 as the starting materials may be formed by plasma

CVD to a thickness of 10 to 200 nm, preferably 50 to 150 nm, as the gate insulation film 1106. The thickness is 100 nm in this example (Fig. 11(A)).

Resist masks 1107, 1108, 1109, 1110 and 1111 are formed using the second photo-mask in such a fashion as to cover the semiconductor layers 1103, and channel formation regions of island semiconductor layers 1104 and 1105. A resist mask 1109 may be formed also on the region in which wiring is to be formed.

A process step for forming the second impurity region is conducted by adding an n-type imparting impurity element. Here, phosphorus is used, and ion doping is conducted with phosphine (PH_3). In this process step, the acceleration voltage is set to 65 keV in order to add phosphorus into a semiconductor layer beneath the gate insulation film 1106 through this film. The P concentration added to the semiconductor layer is preferably 1×10^{16} to 1×10^{19} atoms/cm^3, and it is 1×10^{18} atoms/cm^3 in this case. Regions 1112, 1113, 1114, 1115 and 1116 in which phosphorus is doped are thus formed. A part of the phosphorus-doped regions is to become the second impurity regions that function as the LDD regions (Fig. 11(B)).

Next, the resist mask is removed, and a first conductor layer 1117 is formed on the entire surface. This first conductor layer 1117 uses a conductive material containing the element selected from Ta, Ti, Mo and W as the principal component. The thickness of the first conductor layer 1117 is 100 to 1,000 nm, preferably 150 to 400 nm. Here, the first conductor layer 1117 is formed by sputtering of Ta (Fig. 11(C)).

When the Ta film is used for the first conductor layer, sputtering can be employed. To form the Ta film, Ar is used as the sputtering gas. If a suitable amount of Xe or Kr is added to the sputtering gas, it becomes possible to mitigate the internal stress of the resulting film and to prevent the film from peeling. Resitivity of the α phase Ta film is about 20 μΩcm, and the film can be used for the gate electrode. However, resistivity of the β phase Ta film is about 180 μΩ and the film is not suitable for the gate electrode. Because the TaN film has a crystal structure approximate to the α phase, the α phase Ta film can be easily obtained when the Ta film is formed on the TaN film. Therefore, the TaN film may be formed to a thickness of 10 to 50 nm beneath the first conductor film, though it is not shown in the drawing. Similarly, a phosphorus-doped silicon film can be formed effectively to a thickness of about 2 to about 20 nm beneath the first conductor film, though this silicon film is not shown, either. In this way, it becomes possible to improve adhesion power of the conductor film, to prevent its oxidation and to prevent the diffusion of the alkali metal elements contained in trace amounts in the first or second conductor film into the gate insulation film 1106. In any way, the first conductor film has preferably a resistivity of 10 to 50 μΩcm.

It is further possible to use a W film. In such a case, the W film is formed to a thickness of 200 nm by sputtering that uses W as the target and introduces an argon (Ar) gas and a nitrogen (N_2) gas. The W film can be formed by thermal CVD using tungsten hexafluoride (WF_6). In order to use it as the gate electrode, its resistance must be lowered. Therefore, the resistivity of the W film is preferably not greater than 20 μΩcm. The resistivity of the W film can be lowered by increasing its crystal grain size. However if large amounts of impurities such as oxygen are contained in the W film, crystallization is impeded and the resistivity becomes high. Therefore, when sputtering is employed, the W film must be formed by using a W target having a purity of 99.9999% while sufficient caution is taken so as not to allow mixing of the impurities from the gaseous phase. A resistivity of 9 to 20 μΩcm can be realized in this way.

Next, the resist masks 1118, 1119, 1120, 1121, 1122 and 1123 are formed using the third photo-mask. The fourth photo-mask is used for forming the gate electrode of the p-channel TFTs, the gate wiring of the CMOS circuit and the pixel area and the gate bus lines. Because the gate electrode of the n-channel TFT is formed in the later process step, the resist masks 1119 and 1123 are formed in such a fashion that the first conductor layer 1117 remains on the entire surface of the semiconductor layer 1104.

The unnecessary portions of the first conductor layer are etched away by drying etching. Etching of Ta is effected using a mixed gas of CF_4 and O_2. There are thus formed the gate electrode 1124, the gate wirings 1126 and 1128 and the gate bus line 1127.

A process step for adding a p-type imparting impurity element is conducted into a part of the semiconductor layer 1103 where the p-channel TFT is formed, while the resist masks 1118, 1119, 1120, 1121, 1122 and 1123 are left as such. Here, boron is used as the impurity element, and ion doping is conducted using diborane (B_2H_6). The acceleration voltage is also 80 keV· in this case, and boron is doped in a dose of 2×10^{20} atoms/cm^3. There are thus formed the third impurity regions 1130 and 1131 doped with boron in a high concentration as shown in Fig. 12(A).

After the resist mask disposed in the step shown in Fig. 12(A) is removed, resist masks 1124, 1125, 1126, 1127, 1128, 1129 and 1130 are formed afresh using the fourth photo-mask. The fourth photo-mask is for forming the gate electrode of the n-channel TFT, and the gate electrodes 1131, 1132 and 1133 are formed by dry etching. At this time, the gate electrodes 1131, 1132 and 1133 are so formed as to overlap partially with the second impurity regions 1112, 1113, 1114, 1115 and 1116 (Fig. 12(B)).

After the resist mask is completely removed, new resist masks 1135, 1136, 1137, 1138, 1139, 1140 and 1141 are formed. The resist masks 1136, 1139 and 1140 are so formed as to cover the gate electrodes 1131, 1132 and 1133 of the n-channel TFTs and partially the second impurity region. Here, the resist masks 1136, 1139 and 1140 determine the offset amount of the LDD region.

A process step for forming the first impurity region is conducted by adding an n-type imparting impurity element. There are thus formed the first impurity regions 1143 and 1144 to function as the source region and the first impurity regions 1142, 1145 and 1146 to function as the drain region. Here, ion doping is conducted using phosphine (PH_3). In order to add phosphorus into the semiconductor layer below the gate insulation film 1106 through this film 1106, the acceleration voltage in this step is set to 80 keV, too. The P concentration in this step is higher than the concentration of the step for adding the n-type imparting first impurity element and is preferably 1×10^{19} to 1×10^{21} atoms/cm^3. In this example, it is 1×10^{20}atoms/cm^3 (Fig. 12(C)).

After the process steps up to Fig. 12(C) are completed, a process step for forming the first inter-layer insulation films 1147 and 1148 are conducted. First, a silicon nitride film 1147 is formed to a thickness of 50 nm. This silicon nitride film 1147 is formed by plasma CVD. SiH_4, NH_3 and N_2 are introduced at 5 sccm, 40 sccm and 100 sccm, respectively, at a pressure of 0.7 Torr and radio frequency power of 300 W. Subsequently, a silicon oxide film as the first inter-layer insulation film 1148 is formed to a thickness of 950 nm by introducing TEOS at 500 sccm and O_2 at 50 sccm, at a pressure of 1 Torr and radio frequency power of 200 W (Fig. 13).

The heat-treatment is then conducted. This heat-treatment is necessary for activating the n- or p-type imparting impurity element added in each concentration. This step may be carried out by thermal annealing using an electric heating furnace, laser annealing using the excimer laser described above, a rapid thermal annealing using a halogen lamp (RTA), and so forth. In this example, the activation step is carried out by thermal annealing. The heat-treatment is done at 300 to 700° C, preferably 350 to 550° C, and at 450° C in this example, for 2 hours in a nitrogen atmosphere.

The first inter-layer insulation films 1147 and 1148 are thereafter patterned and contact holes reaching the source region and the drain region of each TFT are formed. The source electrodes 1149, 1150 and 1151 and the drain electrodes 1152 and 1153 are formed. This example uses the electrodes each having a three-layered structure comprising a Ti film having a thickness of 100 nm, a Ti-containing Al film having a thickness of 300 nm and a Ti film having a thickness of 150 nm that are formed continuously by sputtering.

As a result of the process steps described above, the channel formation region 1157, the first impurity regions 1160 and 1161 and the second impurity regions 1158 and 1159 are formed in the n-channel TFTs of the CMOS circuit. Here, regions (GOLD regions) 1158a and 1159a overlapping with the gate electrode and regions (LDD regions) 1158b and 1159b not overlapping the gate electrode are formed in the second impurity regions, respectively. The first impurity region 1160 functions as the source region and the first impurity region 1161, as the drain region.

The channel formation region 1154 and the third impurity regions 1155 and 1156 are formed in the p-channel TFTs. The third impurity region 1155 functions as the source region and the third impurity region 1156, as the drain region.

The n-channel TFT of the pixel area has a multi-gate structure, and there are formed the channel formation regions 1162 and 1163, the first impurity regions 1168, 1169 and 1145 and the second impurity regions 1164, 1165, 1166 and 1167. The regions 1164a, 1165a, 1166a and 1167a overlapping with the gate electrode and the regions 1164b, 1165b, 1166b and 1167b not overlapping with the gate electrode are formed in the second impurity regions.

In this way, the active matrix substrate having the CMOS circuit and the pixel area formed on the substrate 1101 is formed as shown in Fig. 13. A low concentration impurity region 1170, to which the n-type imparting impurity element is added in the same concentration as the second impurity region, a gate insulation film 1106 and a holding capacitance electrode 1171 are formed on the drain side of the n-channel TFT of the pixel unit. A holding capacitance to be disposed in the pixel unit is formed simultaneously.

[Example 2]

This example represents the case where the crystalline semiconductor film used as the semiconductor layer in Example 1 is formed by thermal annealing by use of a catalytic element. When the catalytic element is used, the technology described in Japanese Patent Laid-Open Nos. Hei 7-130652(1995) and Hei 8-78329(1996) is preferably employed.

Fig. 18 shows the case where the technology described in Japanese Patent Laid-Open No. Hei 7-130652(1995) is applied to the present invention. First, a silicon oxide film 1802 is deposited to a substrate 1801, and an amorphous silicon film 1803 is formed on this silicon oxide film 1802. Furthermore, a nickel-containing layer 1804 is formed by applying a nickel acetate solution containing 10 ppm of nickel calculated by weight (Fig. 18(A)).

After a dehydrogenation step is carried out at 500° C for 1 hour, heat-treatment is conducted at 500 to 650° C for 4 to 12 hours, or at 550° C for 8 hours, for example, to form a crystalline silicon film 1805. The crystalline silicon film 1805 obtained in this way has extremely excellent crystallinity (Fig. 18(B)).

The technology described in Japanese Patent Laid-Open No. Hei 8-78329(1996) makes it possible to selectively crystallize the amorphous semiconductor film by selectively adding the catalytic element. The application of this technology to the present invention will be explained with reference to Fig. 19.

First, a silicon oxide film 1902 is disposed on a glass substrate 1901, and an amorphous silicon film 1903 and a silicon oxide film 1904 are continuously formed on the silicon oxide film 1902. The thickness of this silicon oxide film 1904 is 150 nm at this time.

Next, the silicon oxide film 1904 is patterned to form selectively each hole portion 1905, and a nickel acetate solution containing 10 ppm of nickel, calculated by weight, is applied. In this way, a nickel-containing layer 1906 is formed. This nickel-containing layer 1906 is brought into contact with the amorphous silicon film 1902 only at the bottom of the hole portion 1905 (Fig. 19(A)).

Heat-treatment is then conducted at 500 to 650° C for 4 to 24 hours, for example, at 570° C for 14 hours, to form a crystalline silicon film 1907. During this crystallization process, the portion of the amorphous silicon film keeping contact with nickel is first crystallized, and crystallization proceeds from thence in the lateral direction. The crystalline silicon film 1907 thus formed comprises the aggregate of rod- or needle-like crystals, and each crystal grows with certain specific directivity when watched macroscopically. Therefore, the crystalline silicon film 1907 has the advantage that its crystallinity is uniform (Fig. 19(B)).

The catalytic element that can be used in the two technologies described above includes germanium (Ge), iron (Fe), palladium (Pd), tin (Sn), lead (Pb), cobalt (Co), platinum (Pt), copper (Cu) and gold (Ag) other than nickel (Ni).

The semiconductor layer of the crystalline TFT can be fabricated by first forming the crystalline semiconductor film (inclusive of the crystalline silicon film and the crystalline silicon germanium film) and then conducting patterning in accordance with these technologies. The TFT fabricated from the crystalline silicon film using the technology of this example provides excellent characteristics, and high reliability is required. However, when the TFT structure of the present invention is employed, the TFT making the most of the advantage of this example can now be fabricated.

[Example 3]

This example represents the case where the crystalline semiconductor film is formed as the initial film using the catalytic element described above to form the amorphous semiconductor film and then removing the catalytic element from the crystalline semiconductor film, as the method of forming the semiconductor layer used in Example 1. This example uses the technologies disclosed in Japanese Patent Laid-Open No. Hei 10-247735(1998), Hei 10-135468(1998) or Hei 10-135469(1998) for forming the semiconductor layer.

The technology described in each reference is the technology for removing the catalytic element used for crystallization of the amorphous semiconductor film by employing the P gettering function after crystallization. This technology makes it possible to reduce the concentration of the catalytic element in the amorphous semiconductor film to not higher than 1 x 10^{17} atoms/cm^3, preferably 1 x 10^{16} atoms/cm^3.

The construction of this example will be explained with reference to Fig. 20. An alkali-free glass substrate typified by a Corning 1737 substrate is used in this example. Fig. 20(A) shows the state where an underlying layer 2002 and a crystalline silicon film 2003 are formed by using the crystallization technology described in Example 3. A silicon oxide film 2004 for masking is formed to a thickness of 150 nm on the surface of the crystalline silicon film 2003. A region in which each hole portion is formed by patterning and the crystalline silicon film is exposed is formed. A process step for adding phosphorus is conducted to give a region 2005 where phosphorus is added to the crystalline silicon film.

When heat-treatment is carried out under this state at 550 to 800° C for 5 to 24 hours, for example, at 600° C for 12 hours, in a nitrogen atmosphere, the region 2005 in which P is doped into the crystalline silicon film functions as a gettering site. In consequence, the catalytic element remaining in the crystalline silicon film 2003 can be segregated into the phosphorus-doped region 2005.

The silicon oxide film 2004 for masking and the phosphorus doped region 2005 are etched away by etching. As a result, the crystalline silicon film, in which the concentration of the catalytic element used in the crystallization process is reduced to 1×10^{17} atoms/cm^3 or below, can be obtained. This crystalline silicon film can be used as such for the semiconductor layer of the TFT of the present invention illustrated in Example 1.

[Example 4]

In the fabrication process of the TFT according to the present invention illustrated in Example 1, this example represents another example for forming the semiconductor layer and the gate insulation film. The construction of this example will be explained with reference to Fig. 21.

A substrate having heat-resistance to at least 700 to 1,100° C is necessary in this example, and a quartz substrate 2101 is used. The crystalline semiconductor is formed using the technology shown in Examples 2 and 3. To obtain the semiconductor layers of the TFT, this semiconductor is patterned into the island shape, giving the semiconductor layers 2102 and 2103. The gate insulation film 2104 is formed in such a fashion as to cover the semiconductor layers 2102 and 2103 by the use of a film consisting of silicon oxide as the principal component. In this example, a silicon nitride oxide film is formed to a thickness of 70 nm by plasma CVD (Fig. 21(A)).

Heat-treatment is conducted in an atmosphere containing a halogen (typically, chlorine) and oxygen. In this example, it is conducted at 950° C for 30 minutes. Incidentally, the heat-treatment temperature may be selected from the range of 700 to 1,100° C, and the treatment time, from the range of 10 minutes to 8 hours (Fig. 21(B)).

As a result, the thermal oxide film is formed in the interface between the semiconductor layers 2102, 2103 and the gate insulation film 2104, and the gate insulation film 2107 is formed. In the oxidation process in the halogen atmosphere, a metal impurity element among the impurities contained in the gate insulation film 2104 and in the semiconductor layers 2102 and 2103 forms a compound with the halogen, and can be removed into the gaseous phase.

The gate insulation film 2107 formed in the process steps described above has a high dielectric withstand voltage, and the interface between the semiconductor layer 2105, 2106 and the gate insulation film 2107 is extremely excellent. The subsequent process steps for obtaining the TFT construction of the present invention are the same as those of Example 1.

[Example 5]

In the fabrication method for forming the crystalline semiconductor film by the method described in Example 2 and the active material substrate by the steps shown in Example 1, this example represents the example where the catalytic element used for the crystallization process is removed by gettering. First, in Example 1, the semiconductor layers 1103, 1104 and 1105 shown in Fig. 11(A) are the crystalline silicon films using the catalytic element. Since the catalytic element used for the crystallization process remains in the semiconductor layer at this time, the gettering process is preferably carried out.

Here, the process step shown in Fig. 12(B) is as such carried out. Then, new resist masks 2201, 1136, 1137, 1138, 1139 and 1140 are formed as shown in Fig. 22. Next, the formation step of the first impurity region is conducted by adding the n-type imparting impurity. There are thus formed the regions 2202, 2203, 1142, 1143, 1144, 1145 and 1146 in which phosphorus is added into the semiconductor layer (Fig. 22(A)).

Boron as the p-type imparting impurity element has been already added to these P-doped regions 2202 and 2203. The P concentration at this time is 1×10^{19} to 1×10^{21} atoms/cm^3 and is about 1/2 of the concentration of boron. Therefore, no influences are observed on the characteristics of the p-channel TFT.

Heat-treatment is carried out under this state at 400 to 800° C for 1 to 24 hours, for example, at 500° C for 12 hours, in a nitrogen atmosphere. This step can activate the n- and p-type imparting impurity elements. Furthermore, because the P-doped regions function as the gettering site, the catalytic elements remaining after the crystallization step can be segregated. As a result, the catalytic element can be removed from the channel formation region (Fig. 22(B)).

After the process step in Fig. 22(B) is completed, the subsequent steps are conducted in the same way as those in Example 1, and the active matrix substrate can be fabricated.

[Example 6]

In this example, the process step for fabricating an active matrix liquid crystal display device from the active matrix substrate fabricated in Example 1 will be explained with reference to Fig. 14.

A passivation film 1401 is formed over the active matrix substrate under the state shown in Fig. 13. The passivation film 1401 comprises a silicon nitride film having a thickness of 50 nm. A second inter-layer insulation film 1402 formed of an organic resin is further deposited to a thickness of about 1,000 nm. A polyimide resin, an acrylic resin or a polyimideamide resin can be used for the organic resin film. The organic resin film provides the advantages that the film formation method is simple and easy, the parasitic capacitance can be reduced because its specific dielectric constant is low, and it has high planarity. Organic resin films other than those described above can be used, too. This example uses polyimide of the type that is thermally polymerized after the application to the substrate, and the film is formed by baking at 300° C.

The third inter-layer insulation film is further formed. The third inter-layer insulation film 1404 is composed of an organic resin film such as polyimide. Contact holes reaching the drain electrode 1153 are formed in the third inter-layer insulation film 1404, the second inter-layer insulation film 1402 and the passivation film 1401, and then pixel electrode 1405 is formed. The pixel electrode 1405 uses a transparent conductive film for a transmission type liquid crystal display device, and a metallic film for a reflection type liquid crystal display device. Since this example deals with the transmission type liquid crystal display device, an indium oxide-tin (ITO) film is formed by sputtering to a thickness of 100 nm, giving the pixel electrode 1405.

Next, as shown in Fig. 15, an orientation film 1501 is formed on the surface of the third inter-layer insulation film 1404 and the pixel electrode 1405. Generally, the liquid crystal display device uses a polyimide resin for the orientation film in most cases. A transparent conductive film 1503 and an orientation film 1504 are formed on the substrate 1502 on the opposite side. After the orientation film is formed, it is subjected to rubbing treatment so that the liquid crystal molecules are oriented in parallel with a certain predetermined pre-tilt angle.

After the above-described process steps are completed, the pixel unit, the active matrix substrate on which the CMOS circuit has been formed and the opposing substrate are bonded through a sealant and spacers (both are not shown) by a known cell assembly step. Thereafter, a liquid crystal material 1505 is injected between both substrates and is completely sealed by a sealant (not shown). The active matrix type liquid crystal display device shown in Fig. 15 is thus completed.

Next, the construction of the active material liquid crystal display device of this example will be explained with reference to Figs. 16 and 17. Fig. 16 is a perspective view of the active matrix substrate of this example. The active matrix substrate comprises a pixel area 1601 formed on the glass substrate 1101, a scanning (gate) line driving circuit 1603 and a signal (source) line driving circuit 1604. Each pixel TFT 1600 of the pixel area is the n-channel TFT, and the driving circuit round the pixel TFTs basically comprises a CMOS circuit. The scanning (gate) line driving circuit 1603 and the signal (source) line driving circuit 1604 are connected to the pixel area 1601 through the gate wires 1703 and the source wires 1704.

Fig. 17 is a top view of the pixel area 1601, and is substantially a top view of one pixel. The n-channel TFTs are disposed in the pixel area. Each gate electrode 1702 that is formed continuously to the gate wire 1703 crosses the semiconductor layer 1701 therebelow through a gate insulation film, not shown. The source region, the drain region and the first impurity region are formed in the semiconductor layer, though they are not shown in the drawing. A holding capacitance 1707 is constituted by the semiconductor layer, the gate insulation film and the electrode made of the same material as that of the gate electrode, on the drain side of the pixel TFT. The sectional structures taken along a line A - A' and B - B' in Fig. 17 correspond to the sectional view of the pixel unit shown in Fig. 15.

The pixel TFT 1600 in this example has a double-gate structure, but it may be a single gate structure or a multi-gate structure made as triple gate. The structure of the active matrix substrate of this example is not particularly limited to the structure of this example. The feature of the construction of the present invention resides in the structure of the gate electrode, and in the structures of the source region of the semiconductor layer disposed through the gate insulation film, the drain region and other impurity regions. Therefore, constructions other than the construction of the present invention may be appropriately selected and determined.

[Example 7]

Fig. 23 shows an example of the circuit construction of the active matrix type liquid crystal display device shown in Example 6. The active matrix type liquid crystal display device of this example includes a source signal line side driving circuit 2301, a gate signal line side driving circuit (A) 2307, a gate signal line side driving circuit (B) 2311, a pre-charge circuit 2312 and a pixel area 2306.

The source signal line side driving circuit 2301 includes a shift register circuit 2302, a level shifter circuit 2303, a buffer circuit 2304 and a sampling circuit 2305.

The gate signal line side driving circuit (A) 2307 includes a shift register circuit 2308, a level shifter circuit 2309 and a buffer circuit 2310. The gate signal line side driving circuit (B) 2311 has a similar construction.

An example of the driving voltage of each of these circuits are such that the shift register circuits 2302 and 2308 have a voltage of 10 to 16 V. The driving voltage of each of the level shifter circuits 2303 and 2309, the buffer circuits 2304 and 2310, the sampling circuit 2305 and the pixel area 2306 is 14 to 16 V. The voltage of the sampling circuit 2305 and the pixel unit 2306 is the amplitude of the voltage, and the voltages the polarity of which is inverted are generally applied alternately.

It is easy according to the present invention to make the lengths of the second impurity regions functioning as the LDD region different in consideration of the driving voltage of the n-channel TFTs, and to fabricate the optimum shape for the TFTs constituting each TFT in the same process step.

Fig. 24(A) shows a structural example of the TFT of the shift register circuit. The n-channel TFT of the shift register circuit is of the single gate type, and the second impurity region to function as the LDD region is disposed only on the drain side. Here, the length of the LDD region (GOLD region) 206a overlapping with the gate electrode and the length of the LDD region 206b not overlapping with the gate electrode may be the length shown in Fig. 26, for example. They can be formed to a length of 2.0 μm for 206a and 1.0 μm for 206b, for example.

Fig. 24(B) shows a structural example of the TFTs of the level shifter circuit and the buffer circuit. The n-channel TFTs of these circuits are of the double-gate type, and the second impurity regions to function as the LDD regions are disposed on the drain side. The length of the LDD regions (GOLD regions) 205a and 205c overlapping with the gate electrode is 2.5 μm, for example, and the length of the LDD regions 205b and 205d not overlapping with the gate electrode is 2.5 μm, for example.

Fig. 24(C) shows a structural example of the TFTs of the sampling circuit. The n-channel TFTs of this circuit are of the single gate type. Because the polarity is inverted, however, the second impurity regions to function as the LDD regions are disposed on both sides of the source and drain sides. The lengths of the LDD regions (GOLD regions) 205a and 206a overlapping with the gate electrode are preferably equal to each other, and the lengths of the LDD regions 205b and 206b not overlapping with the gate electrode are preferably equal to each other. The length of the LDD regions (GOLD regions) 205a and 206a is 1.5 μm, for example, and the lengths of the LDD regions 205b and 206b not overlapping with the gate electrode are 1.0 μm, for example.

Fig. 24(D) shows a structural example of the pixel area. The n-channel TFT of this circuit is of the multi-gate type, and because the polarity is inverted, the second impurity regions to function as the LDD region are disposed on both of the source and drain sides. For example, the length of the LDD regions (GOLD regions) 205a, 205b, 206a and 206c overlapping with the gate electrode may have a length of 1.5 μm, and the length of the LDD regions 206b and 206d not overlapping with gate electrode is 1.5 μm.

[Example 8]

This example represents a semiconductor device incorporating the active matrix type liquid crystal display device using the TFT circuit according to the present invention. The explanation will be given with reference to Figs. 25, 33 and 34.

Examples of such a semiconductor device include mobile information terminals (electronic notebook, mobile computer, cellular telephone, etc.), video cameras, still cameras, personal computers, television sets, and so forth. Examples of such devices are shown in Figs. 25, 33 and 34.

Fig. 25(A) shows the cellular telephone, that comprises a main body 9001, a sound output unit 9002, a sound input unit 9003, a display device 9004, an operation switch 9005 and an antenna 9006. The present invention can be applied to the display device 9004 equipped with the sound output unit 9002, the sound input unit 9003 and the active matrix substrate.

Fig. 25(B) shows the video camera, that comprises a main body 9101, a display device 9102, a sound input unit 9103, an operation switch 9104, a battery 9105 and an image reception unit 9106. The present invention can be applied to the display device 9102 equipped with the active matrix substrate, the sound input unit 9103 and to the image reception unit 9106.

Fig. 25(C) shows the mobile computer, that comprises a main body 9201, a camera unit 9202, an image reception unit 9203, an operation switch 9204 and a display device 9205. The present invention can be applied to the display device 9205 equipped with the image reception unit 9203 and the active matrix substrate.

Fig. 25(D) shows a head-mount display, that comprises a main body 9301, a display device 9302 and an arm unit 9303. The present invention can be applied to the display device 9302. The present invention can be applied also to other signal control circuits, though not shown in the drawings.

Fig. 25(E) shows a portable book, that comprises a main body 9501,display devices 9502 and 9503, a storage medium 9504, an operation switch 9505 and an antenna 9506. This portable book displays the data stored in a mini-disk (MD) or a DVD and the data received through the antenna. The display devices 9502 and 9503 are direct view type display devices, and the present invention can be applied likewise to them.

Fig. 33(A) shows the personal computer, that comprises a main body 9601, an image input unit 9602, a display device 9603 and a keyboard 9604.

Fig. 33(B) shows a player using a recording medium recording a program thereon (hereinafter called the "recording medium"), that comprises a main body 9701, a display device 9702, a speaker unit 9703, a recording medium 9704 and an operation switch 9705. Incidentally, this device uses a DVD (Digital Versatile Disk), a CD, or the like, as the recording medium, and can enjoy listening to music, movies, games, etc., and can make an Internet communication.

Fig. 33(C) shows a digital camera, that comprises a main body 9801, a display device 9802, a viewing portion 9803, an operation switch 9804 and an image reception unit (not shown).

Fig. 34(A) shows a front type projector, that comprises a display device 3601 and a screen 3602. This invention can be applied to the display device and other signal control circuits.

Fig. 34(B) shows a rear type projector, that comprises a main body 3701, a display device 3702, a mirror 3703 and a screen 3704. The present invention can be applied to the display device and other signal control circuits.

Incidentally, Fig. 34(C) shows an example of the construction of the display devices 3601 and 3702 shown in Figs. 34(A) and 34(B). Each display device 3601, 3702 comprises a light source optical system 3801, mirrors 3802 and 3804 through 3806, a dichroic mirror 3803, a prism 3807, a liquid crystal display device 3808, a phase difference plate 3809 and a projection optical system 3810. It comprises an optical system including the projection optical system 3810 and a projection lens. Though this example represents an example of a three-plate system, the present invention is not particularly limited thereto. For example, a single plate type may also be used. Incidentally, an operator can appropriately insert an optical system such as an optical lens, a film having a polarization function, a film for adjusting the phase difference, an IR film, and so forth, into the optical path represented by arrows shown in Fig. 34(C).

Fig. 34(D) shows a structural example of the light source optical system 3810 in Fig. 34(C). In this example, the optical system 3810 comprises a reflector 3811, a light source 3812, lens arrays 3813 and 3814, a polarization conversion element 3815 and a condenser lens 3816. Incidentally, the light source optical system shown in Fig. 34(D) is merely illustrative but in no way restrictive. For example, the operator may appropriately insert an optical system such as an optical lens, a film having a polarization function, a film for adjusting the phase difference, an IR film, and so forth. Additionally, the present invention can be applied to image sensors and EL type display devices. As described above, the application range of the present invention is extremely broad, and the invention can be applied to electronic appliances of all fields.

[Example 9]

This example explains the example where EL (electro-luminescence) display panel (also called the "EL display device") is fabricated using the present invention.

Fig. 27(A) is a top view of the EL display panel using the present invention. In Fig. 27(A), reference numeral 10 denotes a substrate, 11 denotes a pixel area, 12 denotes a data line side driving circuit and 13 denotes a scanning side driving circuit. These driving circuits reach an FPC 17 through cables 14 to 16 and are connected to an external appliance.

In this instance, a seal material 19 is disposed in such a fashion as to encompass at least the pixel area, preferably the driving circuits and the pixel unit. These members are then sealed by an opposing plate 80. The opposing plate 80 may use a glass plate or a plastic plate. An adhesive 81 is disposed further outside the seal material 19, firmly bonds the substrate 10 to the opposing plate 80 and prevents the corrosion of the internal devices by the moisture entering from the bond end face. In this way, a sealed space is defined between the substrate 10 and the opposing plate 80. The EL device is completely sealed in the sealed space at this time and is completely cut off from the external air.

A seal resin 83 is further charged between the substrate 10 and the opposing plate 80. An organic resin material selected from a silicone type, an epoxy type, an acrylic type and a phenol type is used for the seal resin 83. Consequently, the organic resin material improves the effect of preventing degradation due to the moisture or the like of the EL device.

Fig. 27(B) shows the sectional structure of the EL display panel according to this example. Over the substrate 10 and the underlying film 21 are formed a driving circuit TFT 22 (a CMOS circuit comprising the combination of the n-channel TFT and the p-channel TFT is shown in this drawing) and a pixel area TFT 23 (only a TFT for controlling the current to the EL device is shown in this drawing). The n-channel TFT for the driving circuit or the p-channel TFT for the driving circuit shown in Example 1 may be used for the driving circuit TFT 22. The n-channel TFT or the p-channel TFT shown in Fig. 2 may be used for the pixel unit TFT 23.

After the driving circuit TFT 22 and the pixel unit TFT 23 are completed in accordance with the present invention, a pixel electrode 27 is formed on an inter-layer insulation film (planarization film) 26 made of a resin material. This pixel electrode 27 comprises a transparent conductor film to be electrically connected to the drain of the pixel unit TFT 23. A compound between indium oxide and tin oxide (called "ITO") or a compound between indium oxide and zinc oxide may be used for the transparent conductor film. After the pixel film 27 is formed, the insulation film 28 is formed and an opening is formed on the pixel electrode 27.

Next, an EL layer 29 is formed. The EL layer 29 may be constituted to a laminate structure or a single-layer structure by combining freely known EL materials (positive hole injection layer, positive hole transportation layer, light emitting layer, electron transportation layer or electron injection layer). Which structure is to be obtained may be determined by known technologies. The EL materials include low molecular weight materials and polymer materials. Vacuum deposition is employed when the low molecular weight materials are used, and a simple method such as spin coating, printing or ink jetting can be used when the polymer materials can be used.

In this example, the EL layer is formed by vacuum deposition using a shadow mask. Color display becomes feasible when the light emitting layers (red emitting layer, green emitting layer and blue emitting layer) capable of emitting the rays of light having a different color for each pixel are formed using the shadow mask. Additionally, either of a system comprising the combination of a color conversion layer (CCM) with color filters, a system comprising the combination of a white emitting layer with the color filters may be used as well. Needless to say, an EL display device of monochromatic emission can be constituted.

After the EL layer 29 is formed, a cathode 30 is formed on the EL layer 29. The moisture and oxygen that exist in the interface between the cathode 30 and the EL layer 29 are preferably eliminated as much as possible. Therefore, the EL layer 29 and the cathode 30 are continuously formed into the films in vacuum, or after the EL layer 29 is formed in an inert atmosphere, the cathode 30 is then formed without releasing the inert atmosphere. This example uses a film formation apparatus of a multi-chamber type (cluster tool system) and can conduct such film formation.

This example uses a laminate structure of a LiF (lithium fluoride) film and an Al (aluminum) film for the cathode 30. More concretely, a 1 nm-thick LiF (lithium fluoride) film is formed by vacuum deposition on the EL layer 29, and a 300 nm-thick aluminum film is formed on the LiF film. Needless to say, a MgAg electrode as a known cathode material may be used. The cathode 30 is connected to a cable 16 in a region represented by reference numeral 31. The cable 16 is a power supply line for applying a predetermined voltage to the cathode 30, and is connected to the FPC 17 through a conductive paste material 32.

In order to connect electrically the cathode 30 to the cable 16 in the region 31, contact holes must be formed in the inter-layer insulation film 26 and in the insulation film 28. The contact holes may be formed at the time of etching of the inter-layer insulation film 26 (at the time of the formation of the contact hole for the pixel electrode) and at the time of etching of the insulation film 28 (at the time of formation of the opening before the formation of the EL layer). When the insulation film 28 is etched, etching must be made collectively to the inter-layer insulation film 26. In this case, the shape of the contact holes becomes satisfactory if the inter-layer insulation film 26 and the insulation film 28 are made of the same resin material.

The cable 16 is electrically connected to the FPC 17 through the space between the seal 19 and the substrate 10 (which space is closed by the adhesive 81). Incidentally, though the explanation is given on the cable 16 here, other cables 14 and 15, too, are electrically connected likewise to the FPC 17 through and below the sealing material 18.

The present invention can be used for the EL display panel having the construction described above. Fig. 28 shows a further detailed sectional structure of the pixel unit and Fig. 29(A) shows its top structure. Fig. 29(B) shows its circuit diagram. Since common reference numerals are used in Figs. 28, 29(A) and 29(B), cross-reference is to be made among these drawings.

In Fig. 28, the switching TFT 2402 disposed over the substrate 2401 is fabricated using the n-channel TFT of the present invention (TFT shown in Fig. 2 in Embodiment 1, for example). Though it has the double-gate structure in this example, the explanation is omitted because great differences do not exist in the structure and the fabrication process. However, because the two TFTs are virtually connected in series on account of the double-gate structure, the OFF current value can be reduced advantageously. Though this example uses the double-gate structure, the single gate structure or the multi-gate structure having a greater number of gates may be used, too. Alternatively, the TFT may be fabricated using the p-channel TFT of the present invention.

The current control TFT 2403 is fabricated using the n-channel TFT of the present invention. At this time, the drain wiring 35 of the switching TFT 2402 is electrically connected by a cable 36 to the gate electrode 37 of the current control TFT. The wiring represented by reference numeral 38 denotes the gate wiring that connects the gate electrodes 39a and 39b of the switching TFT.

At this time, it is of utmost importance that the current control TFT 2403 has the structure of the present invention. Since the current control TFT is the device that controls the amount of the current flowing through the EL device, a large current flows through it, and the danger of its degradation due to heat and hot carrier is high. Therefore, the construction of the present invention, in which the LDD region is disposed on the drain side of the current control TFT in such a fashion as to overlap with the gate electrode through the gate insulation film, is extremely effective.

Though the current control TFT 2403 is shown as having the single gate structure in the drawing in this example, a multi-gate structure formed by connecting a plurality of TFTs in series may be used, too. Furthermore, it is possible to employ the construction in which a plurality of TFTs are connected in parallel so as to divide substantially the channel formation region into a plurality of regions and heat radiation is effected highly efficiently. Such a construction is effective as a counter measure for the degradation resulting from heat.

As shown in Fig. 29(A), the wiring to serve as the gate electrode 37 of the current control TFT 2403 overlaps with the drain wiring 40 of the current control TFT 2403 through the insulation film in the region represented by reference numeral 2404. At this time, a capacitor is formed in the region 2404. This capacitor 2404 functions as a capacitor for holding the voltage applied to the gate of the current control TFT 2403. Incidentally, the drain wiring 40 is connected to the current supply line (power source line) 2501, and a constant voltage is always applied to the capacitor.

A first passivation film 41 is disposed on the switching TFT 2402 and on the current control TFT 2403, and a planarization film 42 comprising a resin insulation film is formed on the passivation film 41. It is extremely important to planarize the altitude difference resulting from the TFTs by using the planarization film 42. Since the EL layer to be formed later is extremely thin, any altitude difference might invite an emission defect. Therefore, planarization is preferably carried out before the formation of the pixel electrodes so that the surface of the EL layer is as planar as possible.

Reference numeral 43 denotes the pixel electrode (cathode of the EL device) comprising a conductive film having a high reflecting property. It is electrically connected to the drain of the current control TFT 2403. A conductor film having a low resistance such as an aluminum alloy film, a copper alloy film or a silver alloy film, or their laminate film, is preferably used for the pixel electrode 43. A laminate structure with other conductor films may naturally be used, too.

A light emitting layer 44 is formed inside a trench (corresponding to the pixel) defined by banks 44a and 44b made of an insulation film (preferably, a resin). Though the drawing shows only one pixel, the light emitting layers may be formed dividedly in such a fashion as to correspond to R (red), G (green) and B (blue). A conjugate polymer material is used as the organic EL material to form the light emitting layer. Typical examples of the polymer materials include poly-paraphenylene vinylene (PPV), polyvinylcarbazole (PVK) and polyfluorene.

Various types are available for the PPV type organic EL materials, and it is possible to use the materials described in H. Shenk, H. Becker, O. Gelsen, E. Kluge, W. Kreuder and H. Spreitzer "Polymers for Light Emitting Diodes", Euro Display, Proceedings, 1999, p. 33-37, and in Japanese Patent Laid-Open No. Hei 10-92576(1998).

More concretely, it is possible to use cyano-polyphenylene vinylene for the red emitting layer, polyphenylene vinylene for the green emitting layer and polyphenylene vinylene or polyalkylphenylene for the blue emitting layer. The film thickness is 30 to 150 nm (preferably 40 to 100 nm).

However, the explanation given above represents an example of the organic EL material that can be used as the light emitting layer, and is not at all restrictive. In other words, the EL layer (layer for emitting light and for moving the carriers for light emission) may be formed by combining freely the light emitting layers, the charge transportation layer or the charge injection layer.

Though this example uses the polymer type materials for the light emitting layer, the low molecular weight organic EL materials may be used, too. Furthermore, inorganic materials such as silicon carbide can be used for the charge transportation layer and the charge injection layer.

Known materials can be used for these organic EL materials and the inorganic materials.

This example employs the EL layer of the laminate structure in which a positive hole injection layer 46 composed of PEDOT (polythiophene) or PAni (polyaniline) is disposed on the light emitting layer 45. An anode 47 comprising a transparent conductor film is disposed on the positive injection layer 46. In this example, the rays of light generated by the light emitting layer 45 is radiated towards the upper surface side (above the TFT). Therefore, the anode must be light transmissible. A compound between indium oxide and tin oxide or a compound between indium oxide and zinc oxide can be used for the transparent conductor film. However, because the transparent conductor film is formed after the light emitting layer having low heat resistance and the positive hole injection layer are formed, it is preferably the film that can be formed at a temperature as low as possible.

The EL device 2405 is completed at the point when the anode 47 is completed. Incidentally, the term "EL device 2405" used here represents the capacitor constituted by the pixel electrode (cathode) 43, the light emitting layer 45, the positive hole injection layer 46 and the anode 47. As shown in Fig. 29(A), the pixel electrode 43 has an area substantially corresponding to that of the pixel. Therefore, the pixel functions as the EL device as a whole. It has therefore extremely high utilization of light emission and can display a bright image.

Incidentally, the second passivation film 48 is disposed further on the anode 47. A silicon nitride film or a silicon nitride oxide film is preferred for the second passivation film 48. The second passivation film 48 is directed to cut off the EL device from outside. In other words, it prevents degradation of the organic EL material due to its oxidation and degassing from the organic EL material. Consequently, reliability of the EL display device can be improved.

As described above, the EL display panel according to the present invention includes the pixel unit comprising the pixels having the structure shown in Fig. 28, the switching TFTs having a sufficiently low OFF current value and the current control TFTs highly resistant to the hot carrier injection. Therefore, the present invention can obtain the EL display panel having high reliability and capable of displaying excellent images.

Incidentally, the construction of this example can be executed by combining it freely with the constructions of Embodiments 1 to 6 and Examples 1 to 6. In addition, the EL display panel of this example can be used effectively for the display unit of the electronic appliances of Example 10.

[Example 10]

In this example, the explanation will be given on the structure obtained by inverting the structure of the EL device 2405 in the pixel area shown in Example 9. This explanation will be made with reference to Fig. 30. Incidentally, since the difference of this construction from the construction shown in Fig. 29(A) resides only in the EL device portion and the current control TFT, the explanation of other portions will be omitted.

In Fig. 30, the current control TFT 2601 is fabricated using the p-channel TFT of the present invention. The fabrication process is the same as that of Example 1.

In this example, the pixel electrode (anode) 50 uses a transparent conductor film. More concretely, a conductor film composed of a compound between indium oxide and zinc oxide is used. Needless to say, a conductor film composed of indium oxide and tin oxide may be used, too.

After the banks 51a and 51b comprising the insulation film are formed, the light emitting layer 52 made of polyvinylcarbazole is formed by the application of a solution. The electron injection layer 53 composed of potassium acetylacetonate (hereinafter called "acacK") and the cathode 54 composed of an aluminum alloy are formed on the light emitting layer 52. In this case, the cathode 54 functions also as the passivation film. In this way, the EL device 2602 is formed.

In this example, the rays of light emitted from the light emitting layer 53 are radiated towards the substrate over which the TFTs are formed as indicated by an arrow. In the case of the construction of this example, the current control TFT 2601 comprises preferably the p-channel TFT.

The construction of this example can be executed by combining it freely with the constructions of Embodiments 1 to 6 and Examples 1 to 6. The EL display panel of this example can be applied effectively to the display unit of the electronic appliance of Example 18.

[Example 11]

As shown in Fig. 31, the pixel in this example has a different structure from the structure shown in the circuit diagram of Fig. 29(B). Reference numeral 2701 denotes the source wiring of the switching TFT 2702, reference numeral 2703 denotes the gate wiring of the switching TFT 2702, reference numeral 2704 denotes the current control TFT, reference numeral 2705 denotes the capacitor, reference numerals 2706 and 2708 denote the current supply lines and reference numeral 2707 denotes the EL device.

Fig. 31(A) shows an example where the current supply line 2706 is used in common between two pixels. In other words, this structure is characterized in that the two pixels have line symmetry with the current supply line 2706 as the center. In this case, since the number of the current supply lines can be decreased, the pixel unit can be constituted into a higher precision configuration.

Fig. 31(B) shows an example where the current supply line 2708 is disposed in parallel with the gate wiring 2703. Incidentally, the current supply line 2708 is shown disposed in such a manner as not to overlap with the gate wiring 2703 in Fig. 31(B), and they may be disposed in such a fashion as to overlap with each other through an insulation film if they are formed in different layers. In such a case, the current supply line 2708 and the gate wiring 2703 can share the exclusive occupying area. Therefore, the pixel unit can be constituted into a higher precision configuration.

The structure shown in Fig. 31(C) is characterized in that the current supply line 2708 is disposed in parallel with the gate wiring 2703 in the same way as in Fig. 31(B). Furthermore, the two pixels are disposed in such a fashion as to have line symmetry with the current supply line 2708 as the center. It is also effective to dispose the current supply line 2708 in such a fashion as to overlap with either one of the gate wirings 2703. In this case, since the number of the current supply lines can be decreased, the pixel unit can be constituted into a higher precision configuration.

The construction of this example can be executed by combining it freely with the construction of Example 11 or 12. The EL display panel having the pixel structure of this example can be applied effectively to the display unit of the electronic appliances of Example 10.

[Example 12]

Example 11 disposes a capacitor 2404 in order to hold the voltage applied to the gate of the current control TFT shown in Figs. 29(A) and 29(B). However, this capacitor 2404 can be omitted.

Since the n-channel TFT of the present invention shown in Fig. 28 is used as the current control TFT 2403 in Example 11, this structure includes the LDD region so disposed as to overlap with the gate electrode through the gate insulation film. The parasitic capacitance called the "gate capacitance" is generally formed in this overlapping region, and this example is characterized in that it utilizes positively the parasitic capacitance as the substitute for the capacitor 2404.

Since the capacitance of this parasitic capacitance varies with the overlapping area between the gate electrode and the LDD region, the capacitance can be determined by the length of the LDD region contained in the overlapping region.

The capacitor 2705 can be omitted from the structures shown in Figs. 31(A) to (C).

The construction of this example can be applied by combining it freely with the constructions of Embodiments

1 to 6 and Examples 1 to 6. The EL display panel having the pixel structure of this example can be applied effectively to the display unit of the electronic appliances shown in Example 10.

[Example 13]

Various liquid crystals can be used for the liquid crystal display device shown in Example 7 besides the nematic liquid crystal display device shown in Example 7. For example, it is possible to use the liquid crystals described in 1998, SID, "Characteristics and Driving Scheme of Polymer-Stabilized Mono-stable FLCD Exhibiting Fast Response Time and High Contrast Ratio with Gray-Scale Capability" by H. Furue et al., 1997 SID DIGEST, 841, "A Full-Color Thresholdless Antiferroelectric LCD Exhibiting Wide Viewing Angle with Fast Response Time" by T. Yoshida et al., 1996 J. Mater. Chem. 6(4), 671-673, "Thresholdless antiferroelectricity in liquid crystals and its application to displays" by S. Inui et al., and U.S. Patent Specification No. 5,594,569.

Fig. 32 shows the electro-optical characteristics of a mono-stable FLC when the phase transition of the cholesteric phase-chiral smectic phase C is generated using a ferroelectric liquid crystal (FLC) exhibiting an isotropic-cholesteric-chiral smectic phase transition series while a DC voltage is being applied, and a corn edge is brought substantially into conformity with a rubbing direction. The display mode by the ferroelectric liquid crystal shown in Fig. 32 is referred to as the "Half-V Shape Switching Mode". In the graph shown in Fig. 32, the ordinate represents transmissivity (arbitrary unit) and the abscissa does the impressed voltage. For the detail of the "Half-V Shape Switching Mode FLCD", refer to No. 46 Preceedings of Associated Conference of Society of Applied Physics, March, 1999, p. 1316 and Yoshihara et al., "Time Division Full-Color LCD using Ferroelectric Liquid Crystal", Liquid Crystal, Vol. 3, No. 3, p. 190.

It can be seen from Fig. 32 that when such a ferroelectric mixed liquid crystal is used, gradation display becomes feasible from low voltage driving. The liquid crystal display device according to the present invention can also use ferroelectric liquid crystal exhibiting such electro-optical characteristics.

Those liquid crystals which exhibit an antiferroelectric phase in a certain temperature zone are referred to as "antiferroelectric liquid crystal (AFLC)". Some of the mixed liquid crystals containing the antiferroelectric liquid crystal are called "thresholdless antiferroelectric mixed liquid crystals" exhibiting the electro-optical response characteristics the transmissivity of which changes continuously with respect to the electric field. The thresholdless antiferroelectrtic mixed liquid crystals exhibit so-called "V shape" type electro-optical response characteristics, and some have a driving voltage of about ±2.5 V (with cell thickness of 1 to 2 μm).

Generally, the thresholdless antiferroelectric mixed liquid crystal has great spontaneous polarization and has a high dielectric constant of the liquid crystal itself. Therefore, when the thresholdless antiferroelectric mixed liquid crystal is used for the liquid crystal display device, a relatively large holding capacitance is necessary for the pixel. Therefore, it is preferred to use the thresholdless antiferroelectric mixed liquid crystal having small spontaneous polarization.

Low voltage driving can be achieved by applying such a thresholdless antiferroelectric mixed liquid crystal to the liquid crystal display device of the present invention. In consequence, lower power consumption can be accomplished.

[Example 14]

Stability of the TFTs described in Embodiments 1 to 9 and Examples 1 to 5 is evaluated by a DC bias stress test. This test is conducted by setting the drain voltage (Vd) to a constant voltage of 1 V, and by applying a predetermined voltage for one minute to the gate. The changes of the drain currents before and after the test and field effect mobility are examined. The voltage applied to the gate is changed from 0 to 7 V. When the TFTs undergo degradation due to the hot carrier effect, the various characteristics such as the ON current and field effect mobility get deteriorated in this test. The TFTs used for the measurement have a channel length of 8 μm and a channel width of 8 μm. The LDD has the structure in which Lov is set to 2 μm and Loff is set to 1.5 μm.

Fig. 35 shows the gate voltage (Vg)-v·-drain current (Id) characteristics of the n-channel TFTs having the construction described above (Sample No. S665 - 14). The drain voltages represent the values measured at the impressed voltages of 1 V and 8 V. The characteristic values shown in Fig. 35 are typical values. As such characteristics, the TFTs according to the present invention have field effect mobility of 90 to 300 $cm^2/V{\cdot}sec$ and the drain current (current at application of Vd = 1 V and Vg = 1 V) of 1×10^{-5} to 1×10^{-3} A.

Fig. 36 shows the results of the DC bias stress test described above, and shows the change ratio of the drain current (at application of Vd = 1 V) to the gate bias and the change ratio of field effect mobility (maximum value) to the gate bias. Fig. 36(A) shows the result of the drain current. It can be seen that the drain current hardly changes. Fig. 36(B) shows the result of field effect mobility and shows its maximum value. The change ratio is not greater than 5%. In any way, the TFTs exhibit extremely high stability, and the graph shows that degradation due to the hot carrier effect does not exist.

As shown in Fig. 35, the drain current in the OFF region (OFF current) is not higher than 1 x 10^{-9} A when the voltage applied to the gate is within the range of 0 to -20 V, and such a low value can be attained only when Loff is provided.

As described above, it has been confirmed that when the LDD region (second impurity region) is constituted by the region overlapping with the gate electrode and the region not overlapping with the same in the TFT, degradation due to the hot carrier effect can be prevented, and the drain current of the OFF region can be reduced.

[Effect of the Invention]

The stable crystalline TFT operation can be obtained according to the present invention. As a result, the present invention can improve reliability of the semiconductor devices containing the CMOS circuit fabricated by the crystalline TFTs, or concretely speaking, the pixel unit of the liquid crystal display device and the driving circuit disposed round the pixel unit, and the liquid crystal display device capable of being used for an extended period of time can be obtained.

According to the present invention, it becomes easier to fabricate and adjust the length of the region (GOLD region) overlapping with the gate electrode and the region (LDD region) not overlapping with the gate electrode in the second impurity regions formed between the channel formation region of the n-channel TFT and the drain region. More concretely, it is also possible to decide the length of the region (GOLD region) overlapping with the gate electrode and the length of the region (LDD region) not overlapping with the gate electrode in the second impurity region in accordance with the driving voltage of the TFT. This makes it possible to fabricate the TFTs operating at the respective driving voltages by the same process steps when the TFTs are driven by different driving voltages inside the same substrate.

What is claimed is:

1. A semiconductor device comprising:

a substrate having an insulating surface;

a semiconductor layer formed over said substrate;

a gate insulating film formed in contact with said semiconductor layer;

a gate electrode formed in contact with said gate insulating film; and

a gate wiring connected to said gate electrode,

wherein said gate electrode and said gate wiring comprise a first conductor layer formed in contact with said gate insulation film,

wherein said semiconductor layer comprises

a channel formation region,

a first impurity region of one conductivity type and

a second impurity region of one conductivity type that is sandwiched between said channel formation region and said first impurity region, and is in contact with said channel formation region, and

wherein at least a part of said second impurity region overlaps with said gate electrode.

2. A semiconductor device having a matrix circuit comprising n-channel thin film transistors,

wherein a gate electrode of said n-channel thin film transistors and a gate wiring connected to said gate electrode comprise a first conductor formed in contact with a gate insulating film,

wherein a semiconductor layer of said n-channel thin film transistors comprises

a channel formation region,

a first impurity region of one conductivity type and

a second impurity region of said one conductive type that is sandwiched between said channel formation region and said first impurity region and is in contact with said channel formation region, and

wherein a part of said second impurity region of said one conductivity type overlaps with said gate electrode.

3. A semiconductor device having at least a CMOS circuit comprising n-channel thin film transistors and p-channel thin film transistors,

wherein a gate electrode of said n-channel thin film transistors and a gate wiring connected to said gate electrode comprise a first conductor layer formed in contact with a gate insulating film;

wherein a semiconductor layer of said n-channel thin film transistors comprises

a channel formation region,

a first impurity region of one conductivity type and

a second impurity region of one conductivity type that is sandwiched between said channel formation region and said first impurity region and is contact with said channel formation region, and

wherein a part of said second impurity region of said one conductivity type overlaps with said gate electrode.

4. A semiconductor device comprising

a matrix circuit comprising n-channel thin film transistors and

a CMOS circuit comprising n-channel thin film transistors and p-channel thin film transistors:

wherein a gate electrode of said n-channel thin film transistors and a gate wiring connected to said gate electrode comprise a first conductor layer formed in contact with a gate insulation film,

wherein a semiconductor layer of said n-channel thin film transistors comprises

a channel formation region,

a first impurity region of one conductivity type and

a second impurity region of said one conductivity type that is sandwiched between said channel formation region and said first impurity region and is in contact with said channel formation region, and

wherein a part of said second impurity region of said one conductivity type overlaps with said gate electrode.

5. A semiconductor device according to claim 3:

wherein a gate electrode of said p-channel thin film transistor and a gate wiring connected to said gate electrode comprise a first conductor layer formed in contact with a gate insulating film;

wherein a semiconductor layer of said p-channel thin film transistors comprises

a channel formation region and

a third impurity region having a conductivity type opposite to said one conductivity type, and

wherein a part of said third impurity region of said opposite conductivity type to said one conductivity type overlaps with said gate electrode.

6. A semiconductor device according to claim 4,

wherein a gate electrode of said p-channel thin film transistors and a gate wiring connected to said gate electrode comprise a first conductor layer formed in contact with a gate insulation film;

wherein a semiconductor layer of said p-channel thin film transistors comprises

a channel formation region and

a third impurity region having a conductivity type opposite to said one conductivity type, and

wherein a part of said third impurity region of said opposite conductivity type to said one conductivity type overlaps with said gate electrode.

7. A semiconductor device having a first n-channel thin film

transistor and a second n-channel thin film transistor in one pixel,

wherein a gate electrode of said first and second n-channel thin film transistors and a gate wiring connected to said gate electrode comprise a first conductor layer formed in contact with a gate insulating film;

wherein a semiconductor layer of said first n-channel thin film transistor comprises

a channel formation region,

a first impurity region of one conductivity type and

a second impurity region of said one conductivity type, that is sandwiched between said channel formation region and said first impurity region, and is in contact with said channel formation region,

wherein a part of said second impurity region of said one conductivity type overlaps with said gate electrode; and

wherein a semiconductor layer of said second n-channel thin film transistor comprises

a channel formation region,

a first impurity region of one conductivity type and

a second impurity region of said one conductivity type that is sandwiched between said channel formation region and said first impurity region and is in contact with said channel formation region,

wherein said second impurity region of said one conductivity type overlaps with said gate electrode.

8. A semiconductor device according to claim 7, wherein said first n-channel thin film transistor has a multi-gate structure.

9. A semiconductor device according to claim 7, wherein a device having a light emitting layer is connected to said second n-channel thin film transistor.

10. A semiconductor device including an n-channel thin film transistor and a p-channel thin film transistor in one pixel:

wherein a gate electrode of said n- and p-channel thin film transistors and a gate wiring connected to said gate electrode comprise a first conductor layer formed in contact with a gate insulating film;

wherein a semiconductor layer of said n-channel thin film transistor comprises

a channel formation region,

a first impurity region of one conductivity type and

a second impurity region of said one conductivity type that is sandwiched between said channel formation region and said first impurity region of said one conductivity type, and is in contact with said channel formation region;

wherein a part of said second impurity region of said one conductivity type overlaps with said gate electrode;

wherein a semiconductor layer of said p-channel thin film transistor comprises

a channel formation region,

a third impurity region of a conductivity type opposite to said one conductivity type,

wherein said third impurity region is disposed outside said gate electrode.

11. A semiconductor device including an n-channel thin film transistor and a p-channel thin film transistor in one pixel:

wherein a gate electrode of said n- and p-channel thin film transistors and a gate wiring connected to said gate electrode comprise a first conductor layer formed in contact with a gate insulating film;

wherein a semiconductor layer of said n-channel thin film transistor comprises

a channel formation region,

a first impurity region of one conductivity type and

a second impurity region of said one conductivity that is sandwiched between said channel formation region and said first impurity region of said one conductivity type, and is in contact with said channel formation region,

wherein a part of said second impurity region of said one conductivity type overlaps with said gate electrode;

wherein a semiconductor layer of said p-channel thin film transistor comprises

a channel formation region and

a third impurity region of a conductivity type opposite to said one conductivity type,

wherein a part of said third impurity region overlaps with said gate electrode.

12. A semiconductor layer according to claim 10, wherein said n-channel thin film transistor has a multi-gate structure.

13. A semiconductor layer according to claim 11, wherein said n-channel thin film transistor has a multi-gate structure.

14. A semiconductor device according to claim 10, wherein a device having a light emitting layer is connected to said p-channel thin film transistor.

15. A semiconductor device according to claim 11, wherein a device having a light emitting layer is connected to said p-channel thin film transistor.

16. A semiconductor device according to claim 3,

wherein said gate electrode of said p-channel thin film transistor and a gate wiring connected to said gate electrode of said p-channel thin film transistor comprise said first conductor layer formed contact with said gate insulating film;

wherein said semiconductor layer of a p-channel thin film transistor comprises

a channel formation region and

a third impurity region of a conductivity type opposite to said one conductivity type,

wherein a part of said third impurity region of the conductivity type opposite to said one conductivity type is disposed outside said gate electrode.

17. A semiconductor device according to claim 4,

wherein said gate electrode of said p-channel thin film transistor and a gate wiring connected to said gate electrode of said p-channel thin film transistor comprise said first conductor layer formed contact with said gate insulating film;

wherein said semiconductor layer of a p-channel thin film transistor comprises

a channel formation region and

a third impurity region of a conductivity type opposite to said one conductivity type,

wherein a part of said third impurity region of the conductivity type opposite to said one conductivity type is disposed outside said gate electrode.

18. A semiconductor device according to any of claims 1 through 12, wherein said first conductor layer is made of one, or a plurality, of elements selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W) and molybdenum (Mo), or compounds consisting of said element or elements as the principal component.

19. A semiconductor device according to any one of claims 1, 2, 3, 4, 7, 10 and 11, wherein said semiconductor device is a liquid crystal display.

20. A semiconductor device according to any of claims 1, 2,

3, 4, 7, 10 and 11, wherein said semiconductor device is an EL display device.

21. A semiconductor device according to any of claims 1, 2, 3, 4, 7, 10 and 11, wherein said semiconductor device is an image sensor.

22. A semiconductor device according to any of claims 1, 2, 3, 4, 7, 10 and 11, wherein said semiconductor device is a video camera.

23. A semiconductor device according to any of claims 1, 2, 3, 4, 7, 10 and 11, wherein said semiconductor device is a digital camera.

24. A semiconductor device according to any of claims 1, 2, 3, 4, 7, 10 and 11, wherein said semiconductor device is a projector.

25. A semiconductor device according to any of claims 1, 2, 3, 4, 7, 10 and 11, wherein said semiconductor device is a projection television.

26. A semiconductor device according to any of claims 1, 2, 3, 4, 7, 10 and 11, wherein said semiconductor device is a goggle type display.

27. A semiconductor device according to any of claims 1, 2, 3, 4, 7, 10 and 11, wherein said semiconductor device is a car navigation set.

28. A semiconductor device according to any of claims 1, 2, 3, 4, 7, 10 and 11, wherein said semiconductor device is a

personal computer.

29. A semiconductor device according to any of claims 1, 2, 3, 4, 7, 10 and 11, wherein said semiconductor device is a portable information processing terminal.

30. A semiconductor device according to any of claims 1, 2, 3, 4, 7, 10 and 11, wherein said semiconductor device is an electronic book.

31. A semiconductor device according to any of claims 1, 2, 3, 4, 7, 10 and 11, wherein said semiconductor device is a mobile computer.

32. A semiconductor device according to any of claims 1, 2, 3, 4, 7, 10 and 11, wherein said semiconductor device is a cellular phone.

33. A semiconductor device according to any of claims 1, 2, 3, 4, 7, 10 and 11, wherein said semiconductor device is a head-mount display.

34. A semiconductor device according to any of claims 1, 2, 3, 4, 7, 10 and 11, wherein said semiconductor device is a player.

35. A method of fabricating a semiconductor device comprising the steps of:

forming a semiconductor layer over a substrate having an insulation surface;

patterning said semiconductor layer to form at least a first and a second island semiconductor layers;

forming a gate insulation film in contact with said first and second island semiconductor layers;

adding an impurity element of one conductivity type into a selected region of said first island semiconductor layer, and forming a second impurity region;

forming a first conductor layer in contact with said gate insulation film;

forming a second gate electrode overlapping with said second island semiconductor layer by patterning said first conductor layer;

adding an impurity element of a conductivity type opposite to said one conductivity type into a selected region of said second island semiconductor layer, and forming a third impurity region;

forming a first gate electrode overlapping with said first island semiconductor layer by patterning said first conductor layer; and

adding an impurity element of said one conductivity type into a selected region of said first island semiconductor layer, and forming a first impurity region.

36. A method of fabricating a semiconductor device comprising the steps of:

forming a semiconductor layer over a substrate having an insulation surface;

patterning said semiconductor layer to form at least a first and a second island semiconductor layers;

forming a gate insulation film in contact with said first and second island semiconductor layers;

adding an impurity element of one conductivity type into a selected region of said first island semiconductor layer and forming a second impurity region;

forming a first conductor layer in contact with said gate insulation film;

forming a first gate electrode overlapping with said first island semiconductor layer and a second gate electrode overlapping with said second island semiconductor layer by patterning said first conductor layer;

adding an impurity element of said one conductivity type into a selected region of said first island semiconductor layer, and forming a first impurity region; and

adding an impurity element of a conductivity type opposite to said one conductivity type into a selected region of said second island semiconductor layer, and forming a third impurity region.

37. A method of fabricating a semiconductor device comprising the steps of:

forming a semiconductor layer over a substrate having an insulation surface;

patterning said semiconductor layer to form at least a first and a second island semiconductor layers;

forming a gate insulation film in contact with said first and second island semiconductor layers;

adding an impurity element of a conductivity type opposite to said one conductivity type into a selected region of said second island semiconductor layer, and forming a third impurity region;

adding an impurity element of said one conductivity type into a selected region of said first island semiconductor layer, and forming a second impurity region;

forming a first conductor layer in contact with said gate insulation film;

forming a first gate electrode overlapping with said first island semiconductor layer and a second gate electrode overlapping with said second island semiconductor layer from said first conductor layer; and

adding an impurity element of said one conductivity type into a selected region of said first island semiconductor layer, and forming a first impurity region.

38. A method of fabricating a semiconductor device comprising the steps of:

forming a semiconductor layer over a substrate having an insulation surface;

patterning said semiconductor layer to form at least a first and a second island semiconductor layers;

forming a gate insulation film in contact with said first and second island semiconductor layers;

adding an impurity element of a conductivity type opposite to said one conductivity type into a selected region of said second island semiconductor layer, and forming a third impurity region;

adding an impurity element of said one conductivity type into a selected region of said first island semiconductor layer, and forming a first impurity region;

adding an impurity element of said one conductivity type into a selected region of said first island semiconductor layer, and forming a second impurity region;

forming a first conductor layer in contact with said gate insulation film; and

forming a first gate electrode overlapping with said first island semiconductor layer and a second gate electrode overlapping with said second island semiconductor layer from said first conductor layer.

39. A method of fabricating a semiconductor device comprising the steps of:

forming a semiconductor layer over a substrate having an insulation surface;

patterning said semiconductor layer to form at least first and second island semiconductor layers;

forming a gate insulation film in contact with said first and second island semiconductor layers;

adding an impurity element of one conductivity type into a selected region of said first island semiconductor layer, and forming a first impurity region;

adding an impurity element of said one conductivity type into a selected region of said first island semiconductor layer, and forming a second impurity region;

forming a first conductor layer in contact with said gate insulation film;

forming a second gate electrode overlapping with said second island semiconductor layer from said first conductor layer;

adding an impurity element of a conductivity type opposite to said one conductivity type into a selected region of said second island semiconductor layer, and forming a third impurity region; and

forming a first gate electrode overlapping with said first island semiconductor layer from said first conductivity type.

40. A method of fabricating a semiconductor device comprising the steps of:

forming a semiconductor layer over a substrate having an insulation surface;

patterning said semiconductor layer to form at least first and second island semiconductor layers;

forming a gate insulation film in contact with said first and second island semiconductor layers;

adding an impurity element of one conductivity type into a selected region of said first island semiconductor layer, and forming a first impurity region;

adding an impurity element of a conductivity type opposite to said one conductivity type into a selected region of said second island semiconductor layer, and forming a third impurity region;

adding an impurity element of said one conductivity type into a selected region of said first island semiconductor layer, and forming a second impurity region;

forming a first conductor layer in contact with said gate insulation film; and

forming a first gate electrode overlapping with said first island semiconductor layer and a second gate electrode overlapping with said second island semiconductor layer from said first conductor layer.

41. A method of fabricating a semiconductor device according to any of claims 35 through 40, wherein said first conductor layer comprises an element selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W) and molybdenum (Mo), or compounds consisting of said element or elements as the principal component.

42. A method of fabricating a semiconductor device according to any of claims 35 through 40, wherein said semiconductor

device is a liquid crystal display device.

43. A method of fabricating a semiconductor device according to any of claims 35 through 40, wherein said semiconductor device is an EL display device.

44. A method of fabricating a semiconductor device according to any of claims 35 through 40, wherein said semiconductor device is an image sensor.

45. A method of fabricating a semiconductor device according to any of claims 35 through 40, wherein said semiconductor device is a video camera.

46. A method of fabricating a semiconductor device according to any of claims 35 through 40, wherein said semiconductor device is a digital camera.

47. A method of fabricating a semiconductor device according to any of claims 35 through 40, wherein said semiconductor device is a projector.

48. A method of fabricating a semiconductor device according to any of claims 35 through 40, wherein said semiconductor device is a projection television.

49. A method of fabricating a semiconductor device according to any of claims 35 through 40, wherein said semiconductor device is a goggle type display.

50. A method of fabricating a semiconductor device according to any of claims 35 through 40, wherein said semiconductor device is a car navigation.

51. A method of fabricating a semiconductor device according to any of claims 35 through 40, wherein said semiconductor device is a personal computer.

52. A method of fabricating a semiconductor device according to any of claims 35 through 40, wherein said semiconductor device is a portable information processing terminal.

53. A semiconductor device according to any of claims 35 through 40, wherein said semiconductor device is an electronic book.

54. A semiconductor device according to any of claims 35 through 40, wherein said semiconductor device is a mobile computer.

55. A semiconductor device according to any of claims 35 through 40, wherein said semiconductor device is a cellular phone.

56. A semiconductor device according to any of claims 35 through 40, wherein said semiconductor device is a head-mount display.

57. A semiconductor device according to any of claims 35 through 40, wherein said semiconductor device is a player.

ABSTRACT OF THE DISCLOSURE

Reliability of crystalline TFTs is improved in a large area integrated circuit typified by an active matrix type liquid crystal display device. In TFTs having an LDD structure, a region whose LDD region overlaps with a gate electrode and a region not overlapping with the gate electrode are fabricated inside one TFT. To accomplish this structure, n-channel TFTs are fabricated in non-self-alignment whereas p-channel TFTs are fabricated in self-alignment.

Fig. 1(A)

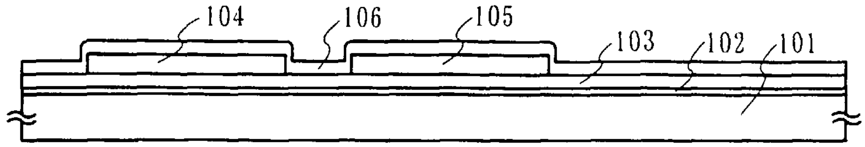


Fig. 1(B)

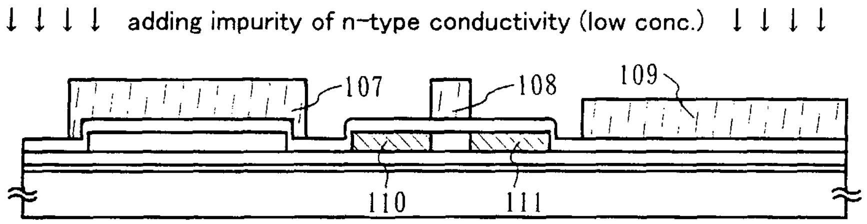


Fig. 1(C)

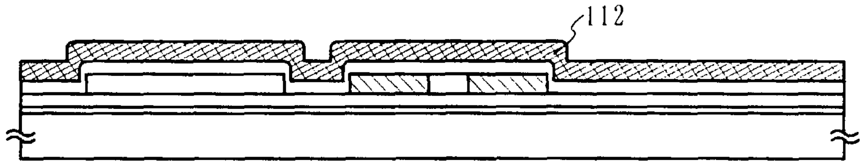


Fig. 1(D)

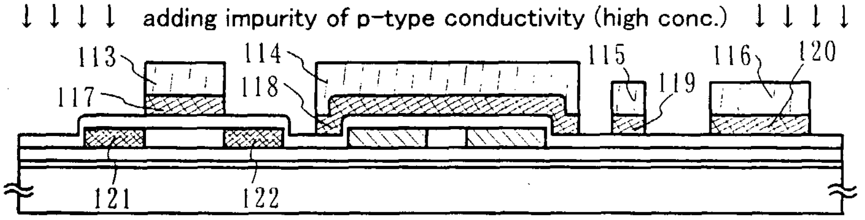


Fig. 1(E)

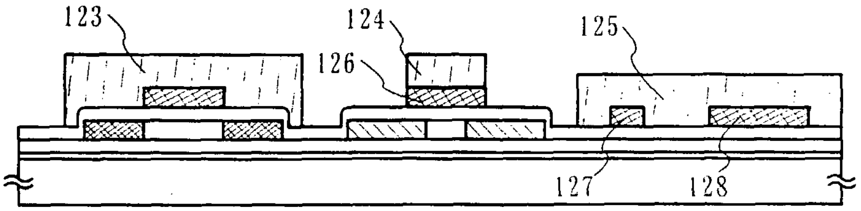
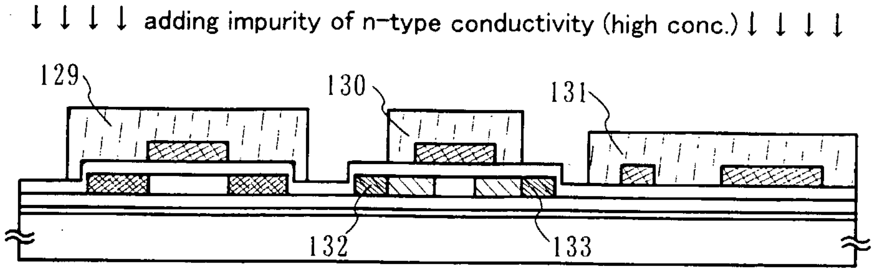
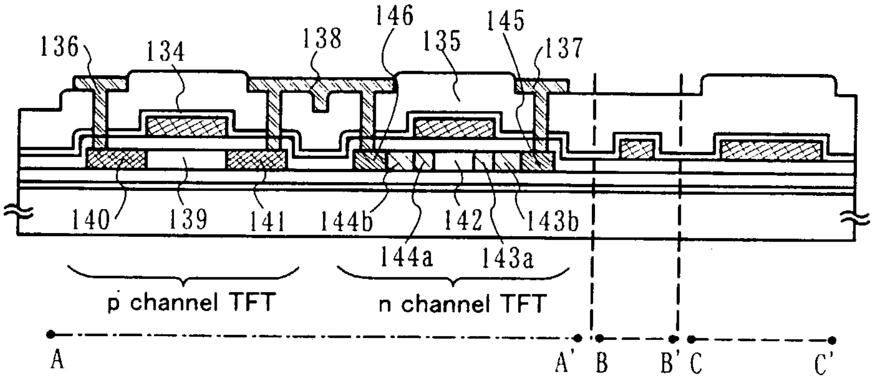


Fig. 2(A)



↓ ↓ ↓ ↓ adding impurity of n-type conductivity (high conc.) ↓ ↓ ↓ ↓
129
130
131
132
133

Fig. 2(B)



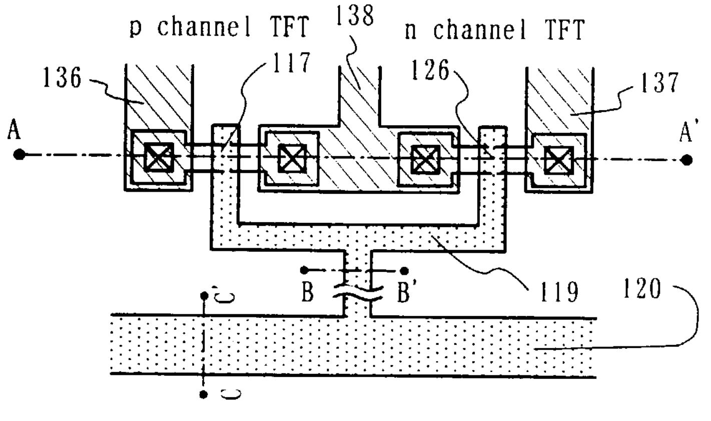


Fig. 2(C)A Top View of CMOS Circuit

Fig. 3(A)

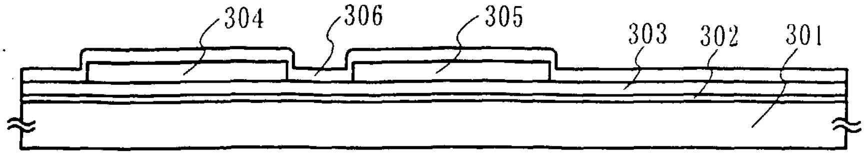


Fig. 3(B)

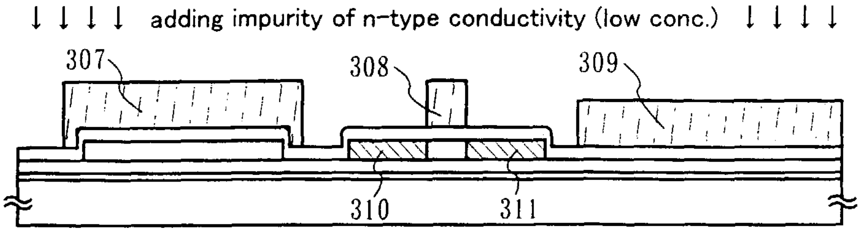

↓ ↓ ↓ ↓ adding impurity of n-type conductivity (low conc.) ↓ ↓ ↓ ↓
307
308
309
310
311

Fig. 3(C)

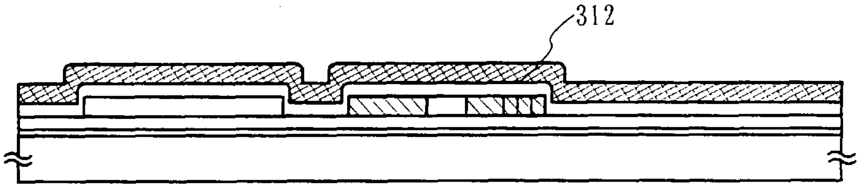


Fig. 3(D)

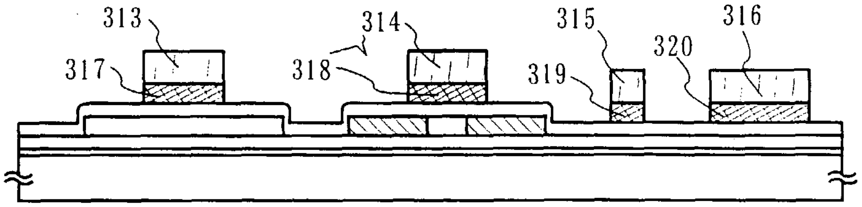
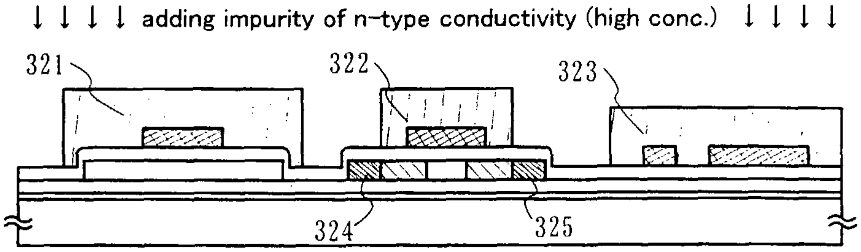


Fig. 3(E)


↓ ↓ ↓ ↓ adding impurity of n-type conductivity (high conc.) ↓ ↓ ↓ ↓
321
322
323
324
325

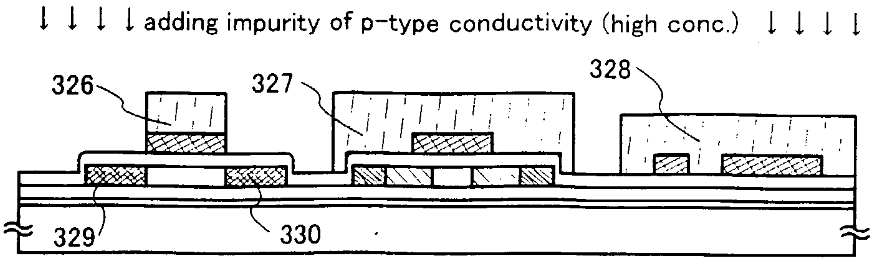


Fig. 4(A)

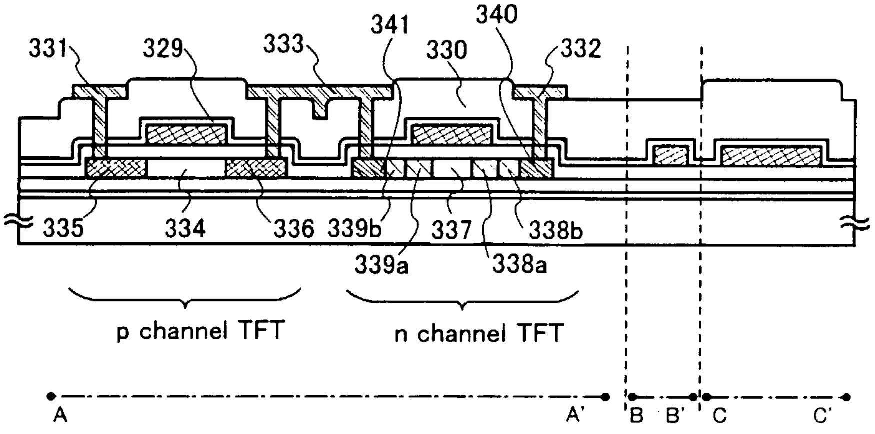


Fig. 4(B)

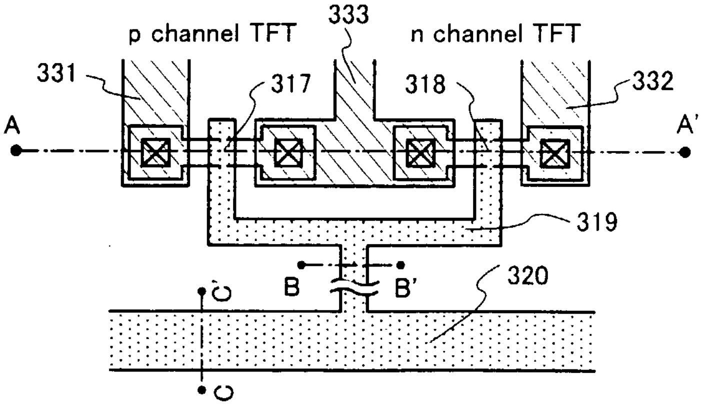


Fig. 4(C)

Fig. 5(A)

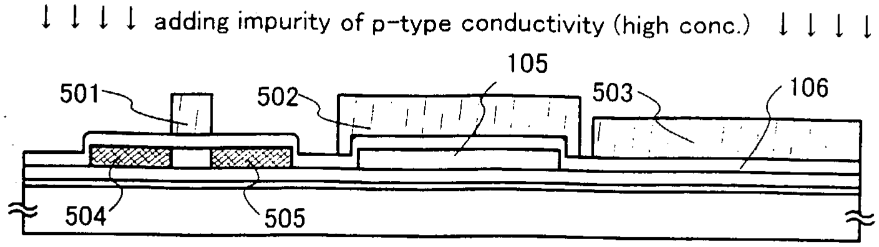

↓ ↓ ↓ ↓ adding impurity of p-type conductivity (high conc.) ↓ ↓ ↓ ↓
105
501
502
503
106
504
505

Fig. 5(B)

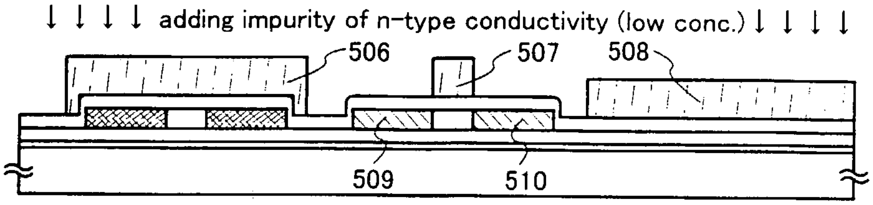

↓ ↓ ↓ ↓ adding impurity of n-type conductivity (low conc.) ↓ ↓ ↓ ↓
506
507
508
509
510

Fig. 5(C)

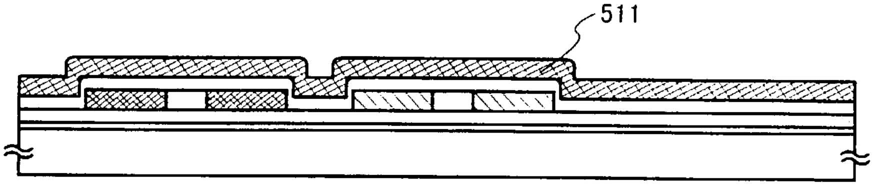


Fig. 5(D)

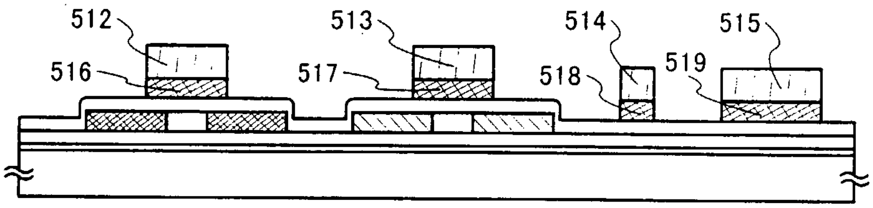


Fig. 5(E)

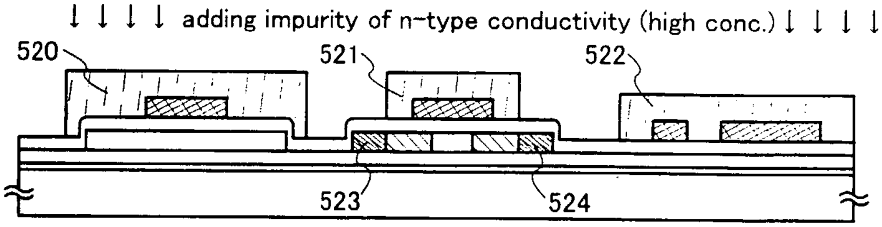
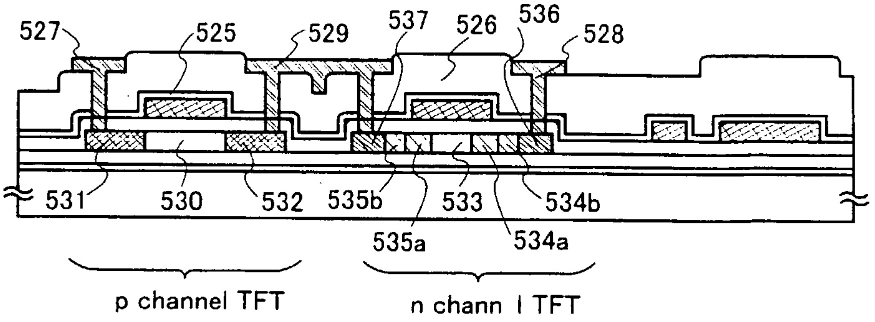

↓ ↓ ↓ ↓ adding impurity of n-type conductivity (high conc.) ↓ ↓ ↓ ↓
520
521
522
523
524

Fig. 5(F)



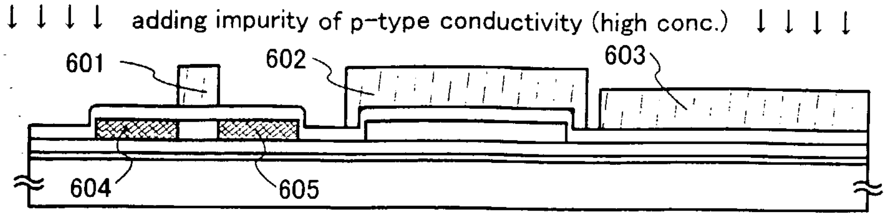
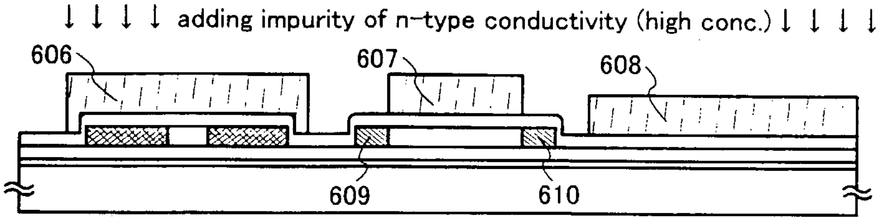


Fig. 6(A)


Fi.g 6(B)

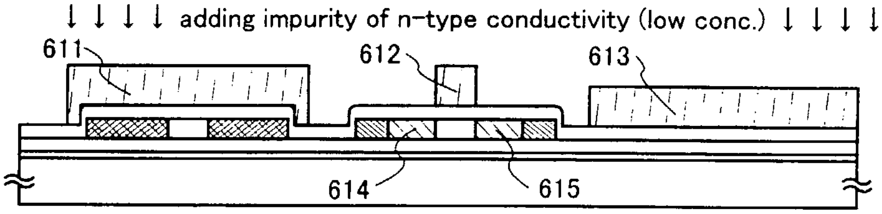
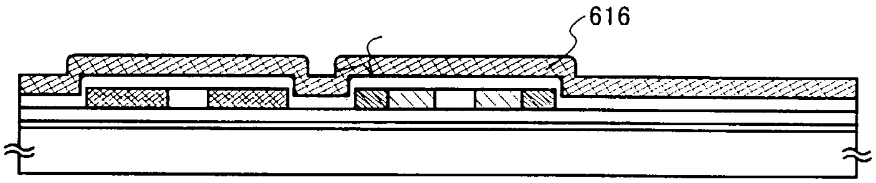


Fig. 6(C)


Fi.g 6(D)

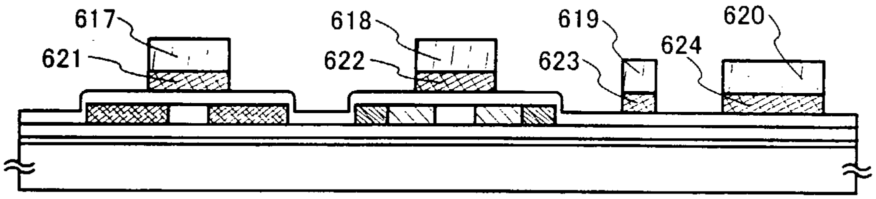


Fig. 6(E)

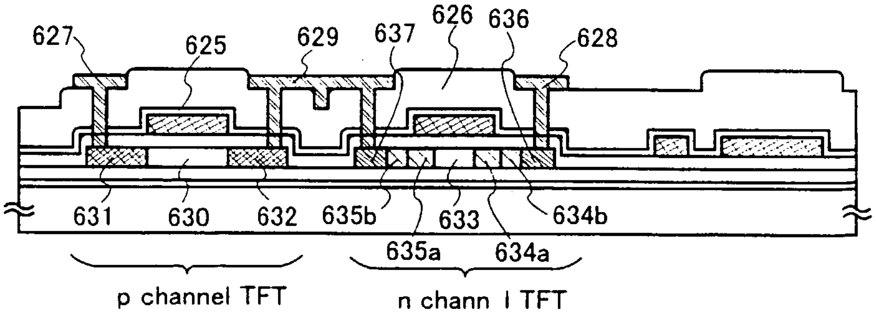


Fig. 6(F)

Fig. 7(A)

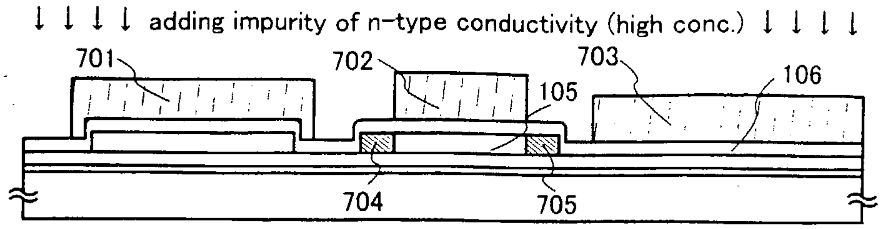


Fig. 7(B)

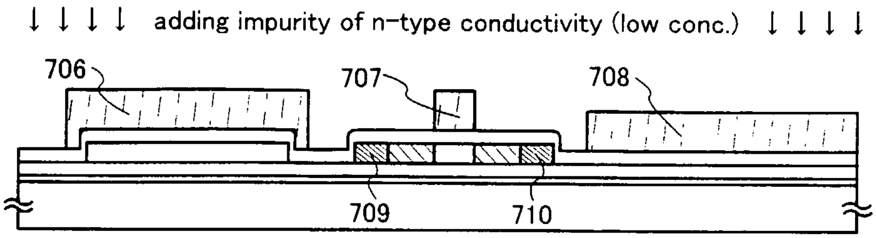


Fig. 7(C)

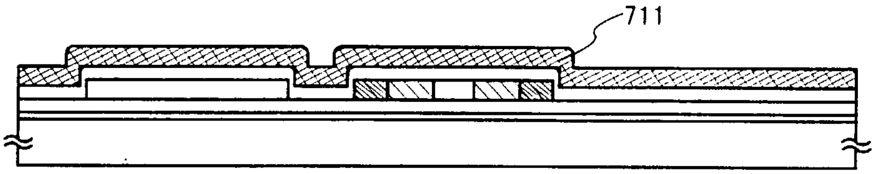


Fig. 7(D)

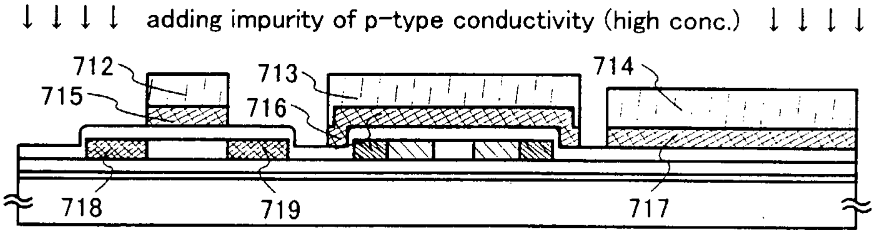


Fig. 7(E)

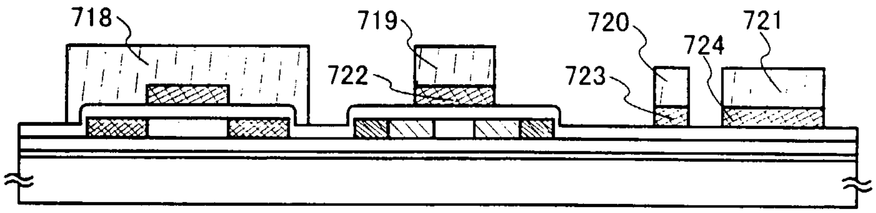


Fig. 7(F)

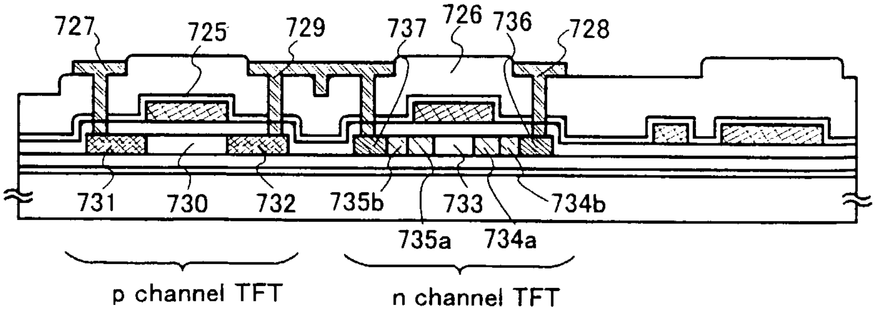


Fig. 8(A)

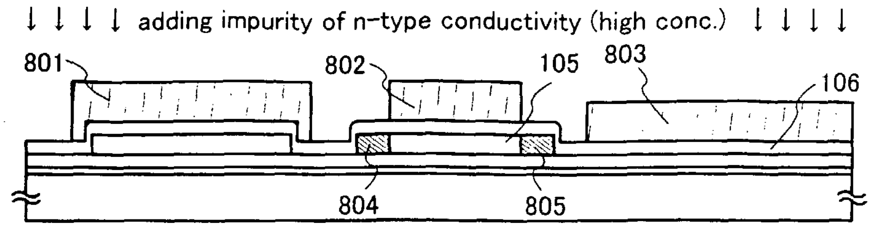


Fig. 8(B)

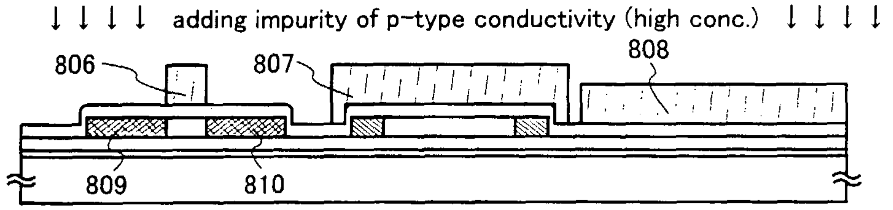


Fig. 8(C)

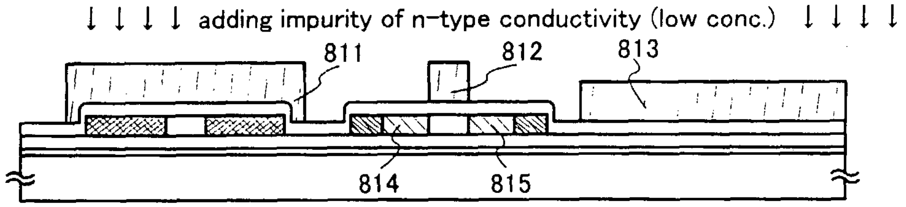
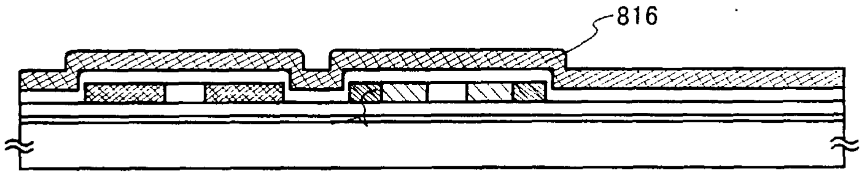


Fig. 8(D)



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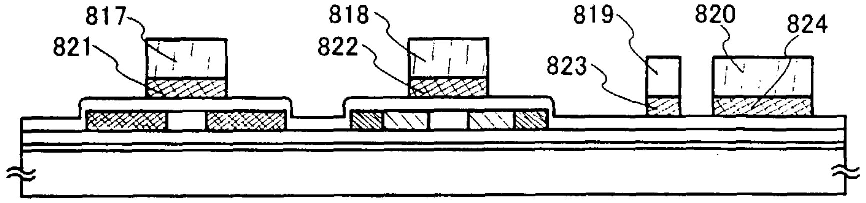
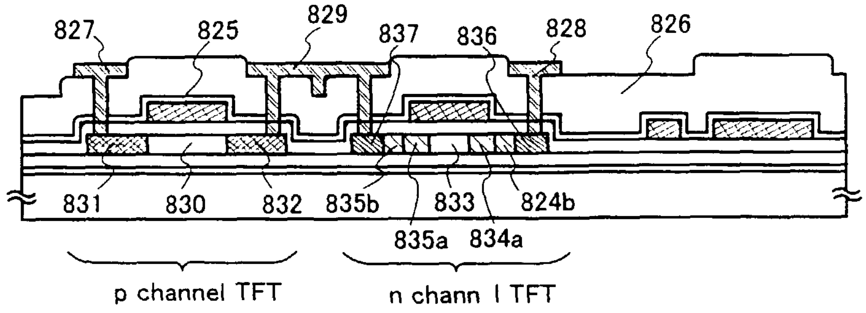


Fig. 8(F)



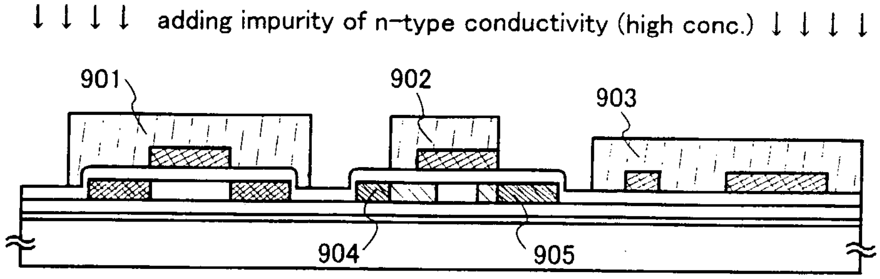

adding impurity of n-type conductivity (high conc.)
901
902
903
904
905

Fig. 9(A)

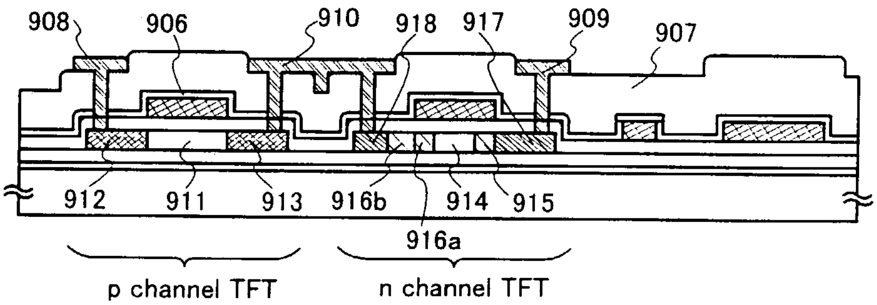
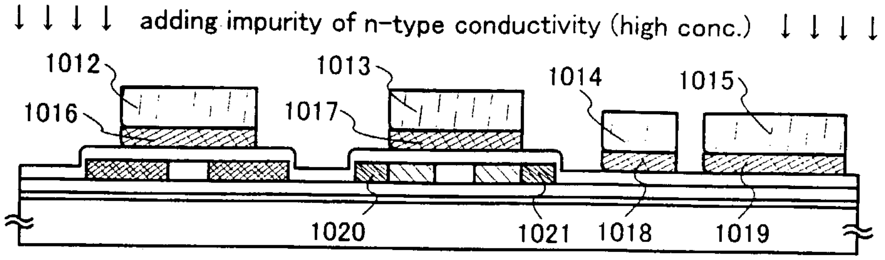

908
906
910
918
917
909
907
912
911
913
916b
914
915
916a
p channel TFT
n channel TFT

Fig. 9(B)



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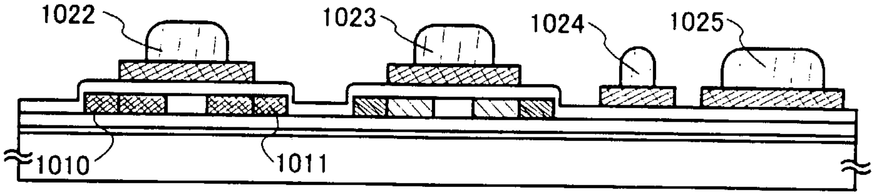


Fig. 10(B)

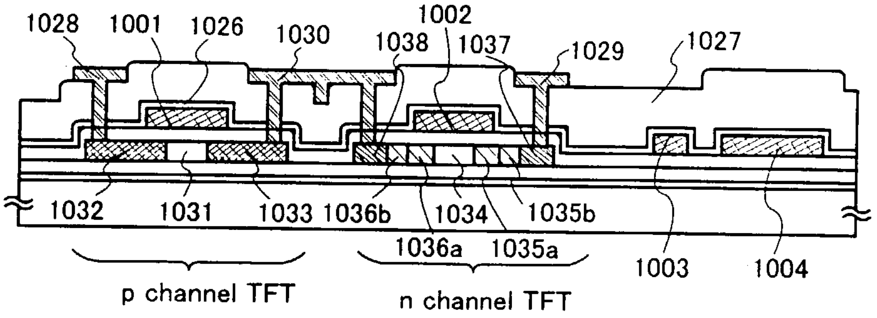


Fig. 10(C)

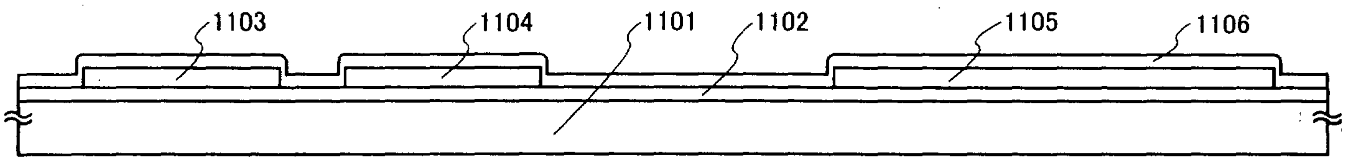


Fig. 11(A)

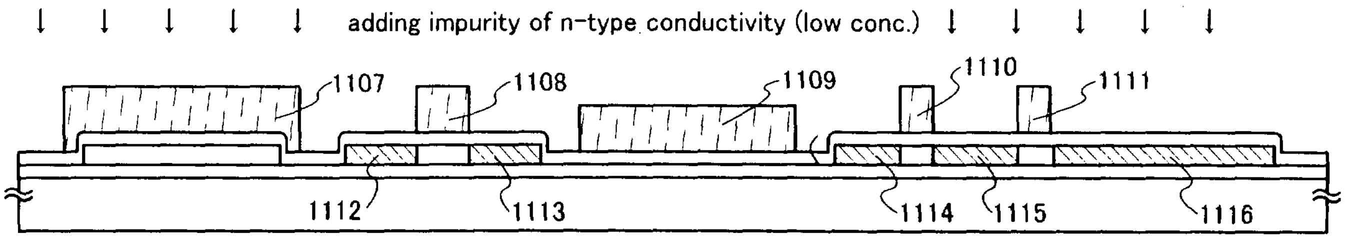


Fig. 11(B)

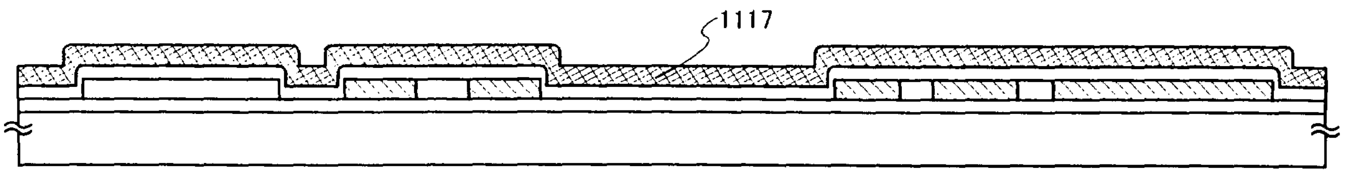


Fig. 11(C)

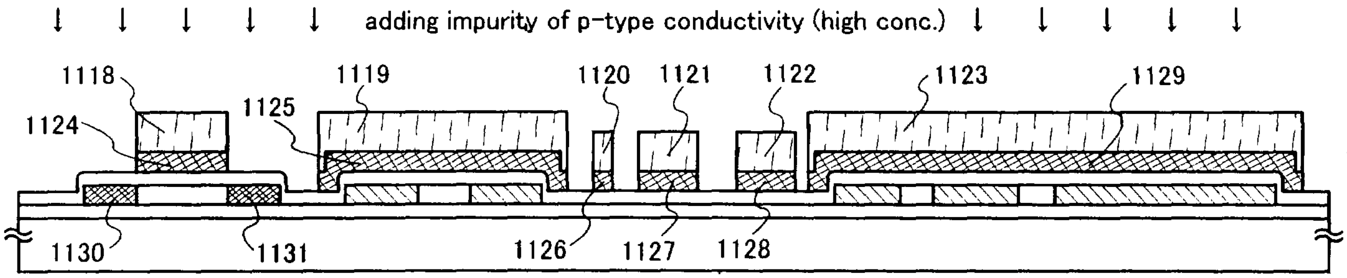


Fig. 12(A)

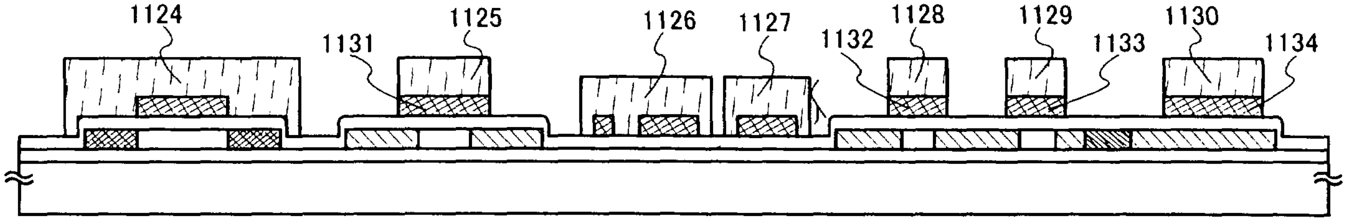


Fig. 12(B)

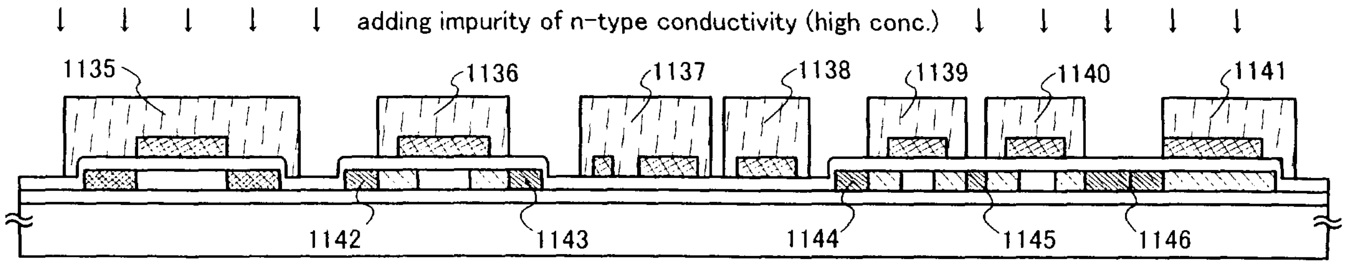
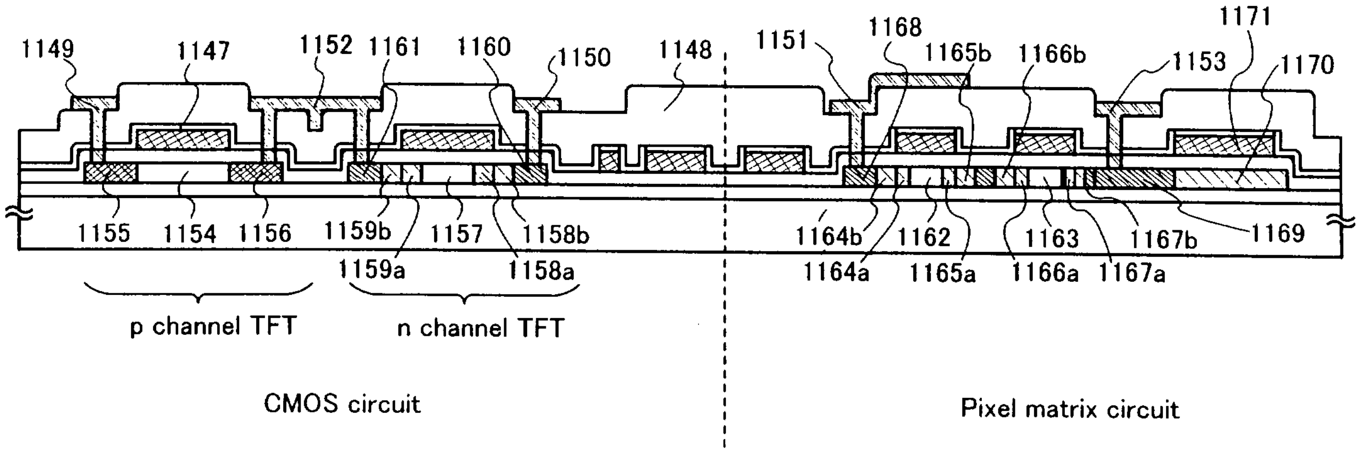


Fig. 12(C)

1149
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1156
1159b
1157
1158b
1159a
1158a
1164b
1162
1163
1167b
1169
1164a
1165a
1166a
1167a
p channel TFT
n channel TFT
CMOS circuit
Pixel matrix circuit

Fig. 13

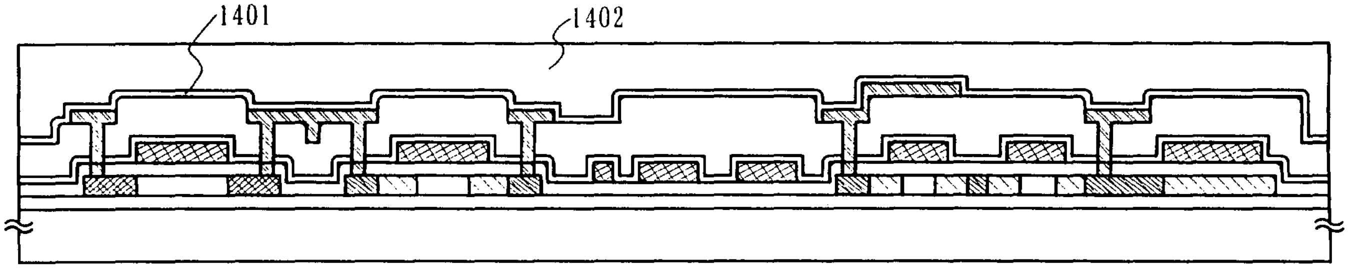


Fig. 14(A)

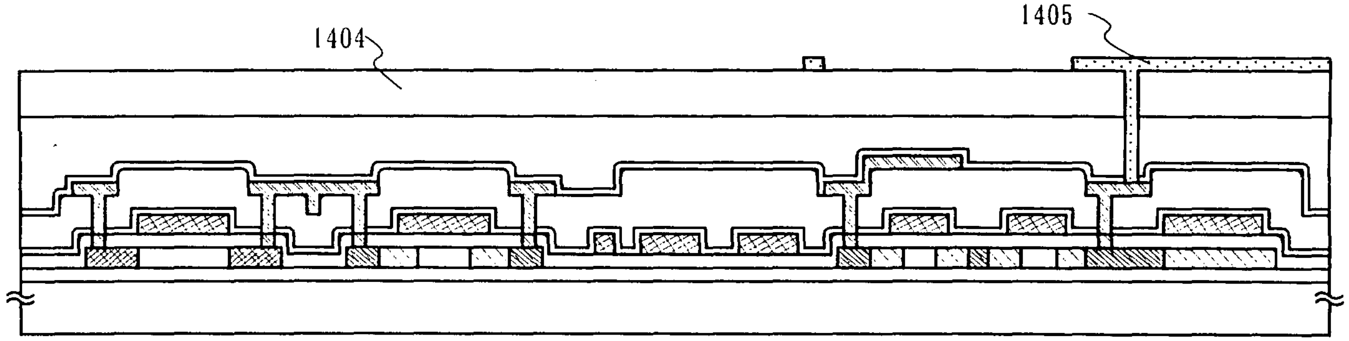


Fig. 14(B)

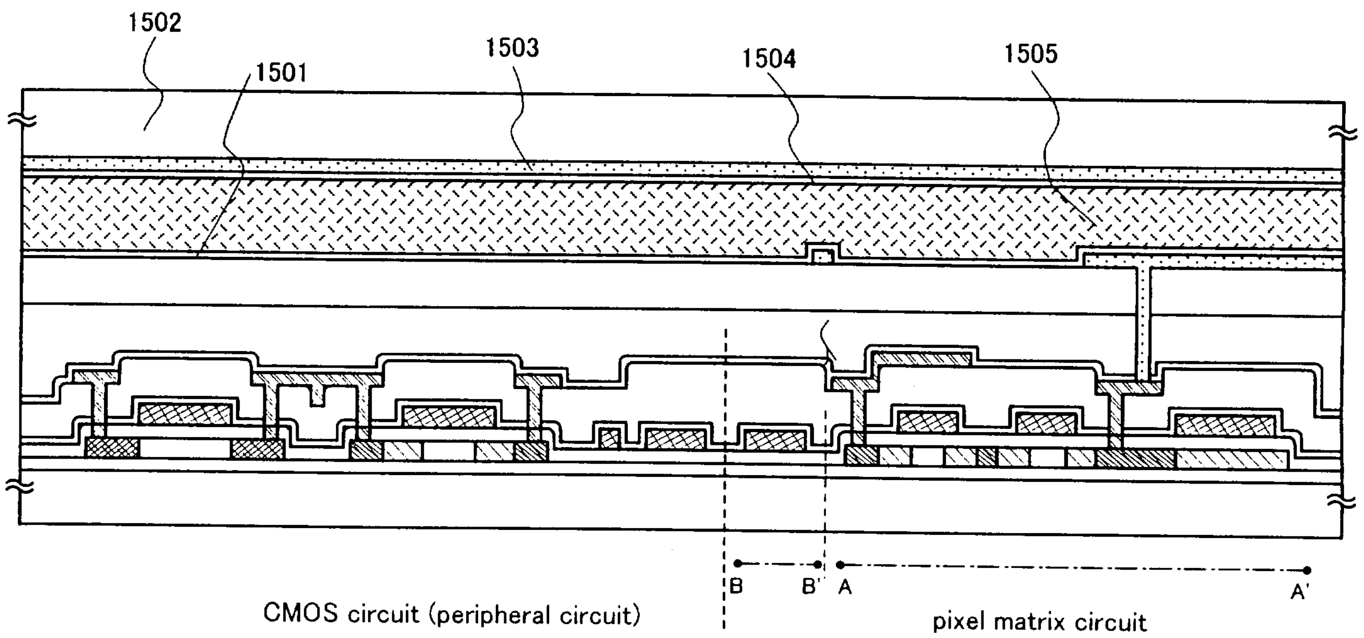

1502
1501
1503
1504
1505
B
B'
A
A'
CMOS circuit (peripheral circuit)
pixel matrix circuit

Fig. 15

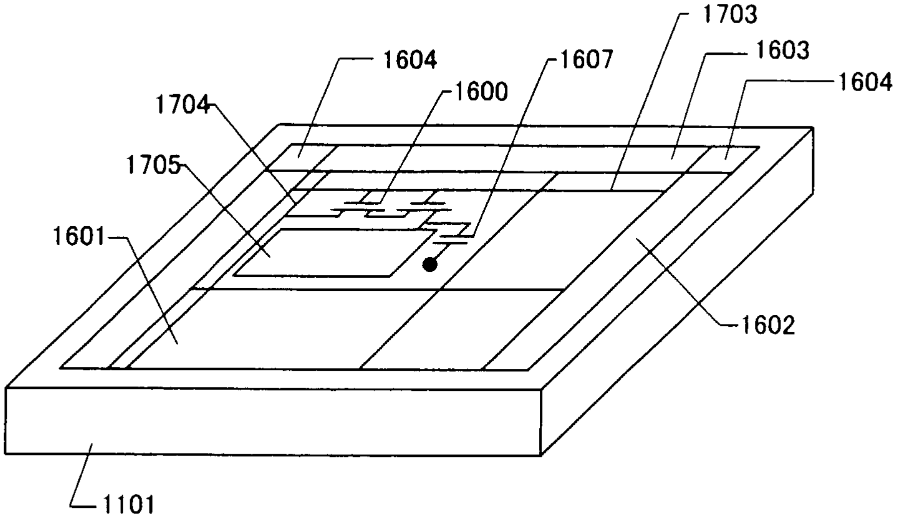


Fig. 16

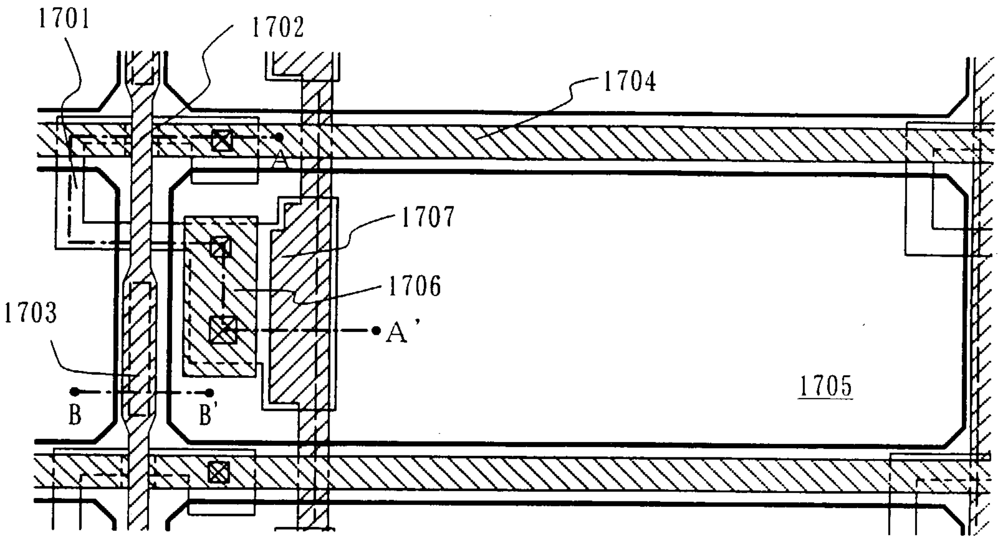


Fig. 17 Top View of a Pixel Matrix Circuit

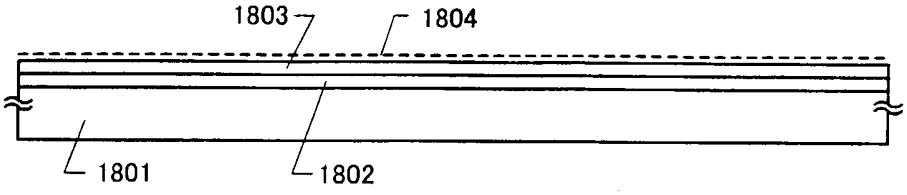


Fig. 18(A)

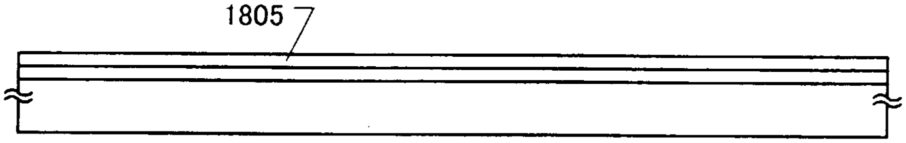


Fig. 18(B) Crystallization Process

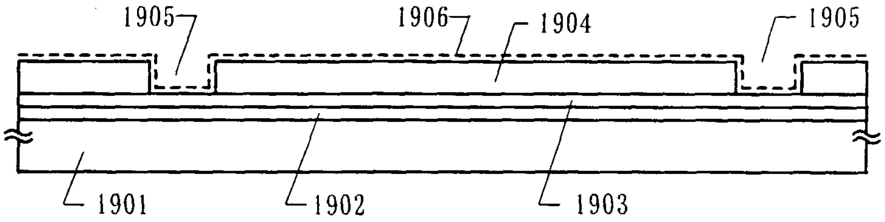


Fig. 19(A)

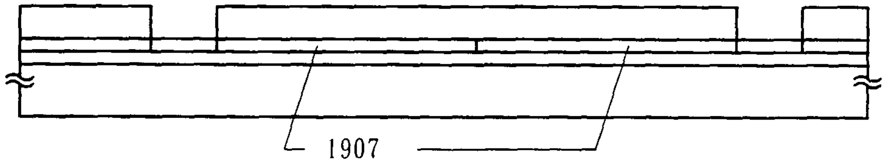


Fig. 19(B) Crystallization Process

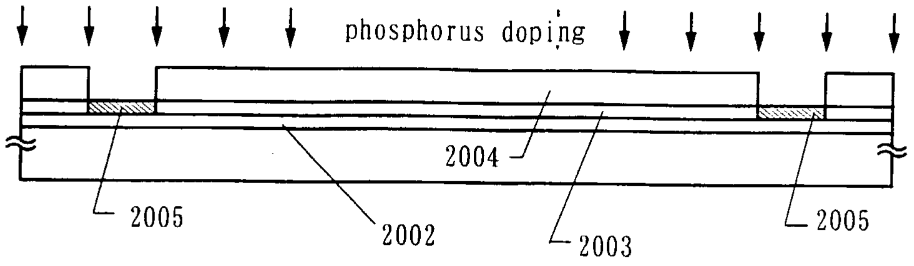


Fig. 20(A)

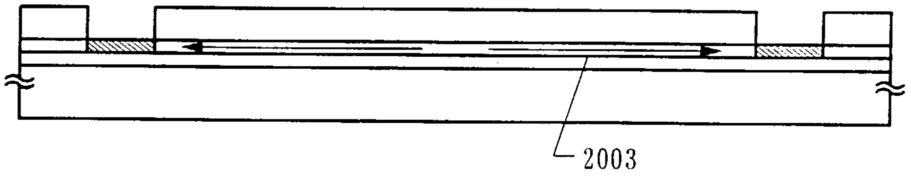


Fig. 20(B)

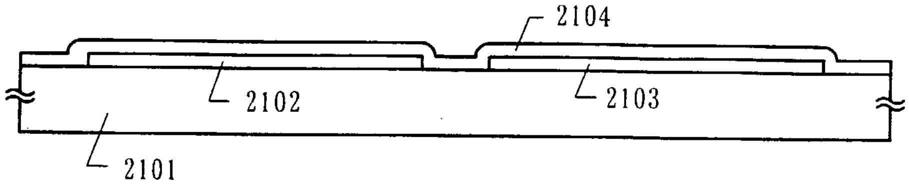


Fig. 21(A)

heat treatment in an atmosphere containing halogen element

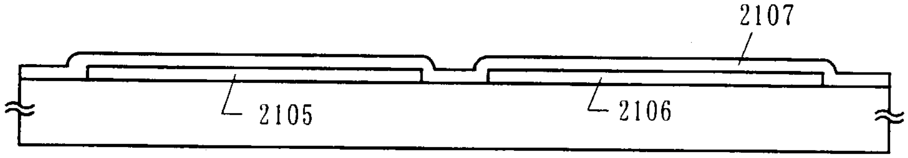


Fig. 21(B)

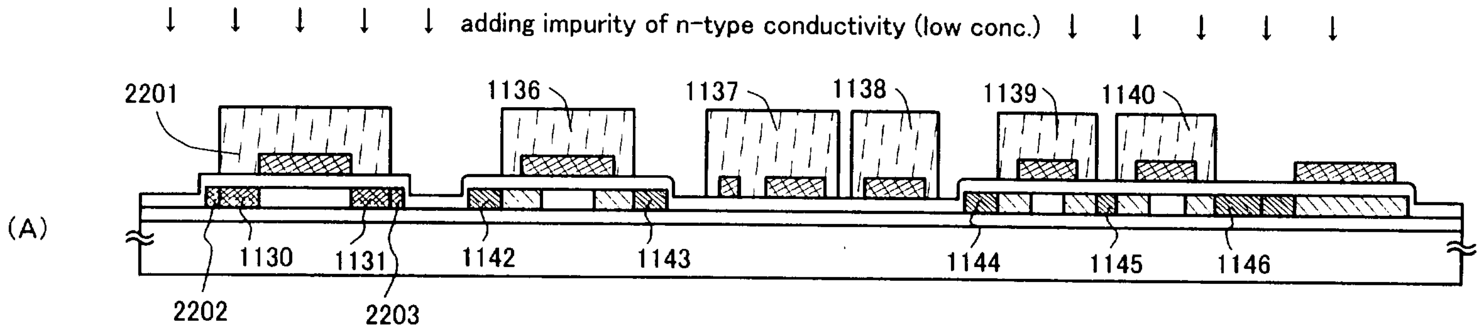


Fig. 22(A)

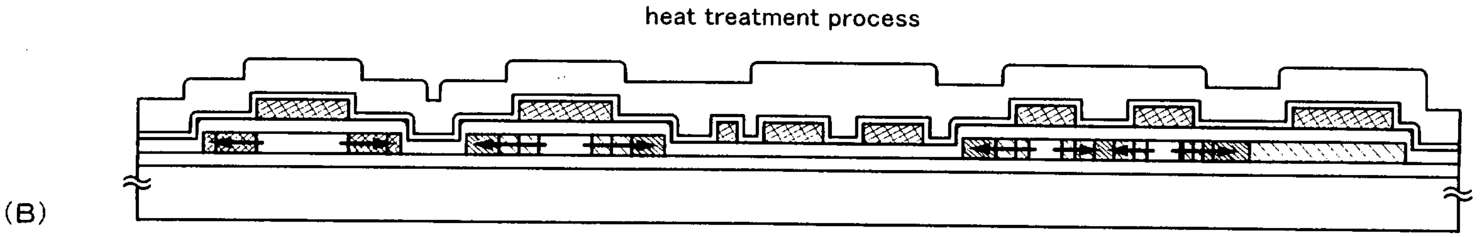


Fig. 22(B)

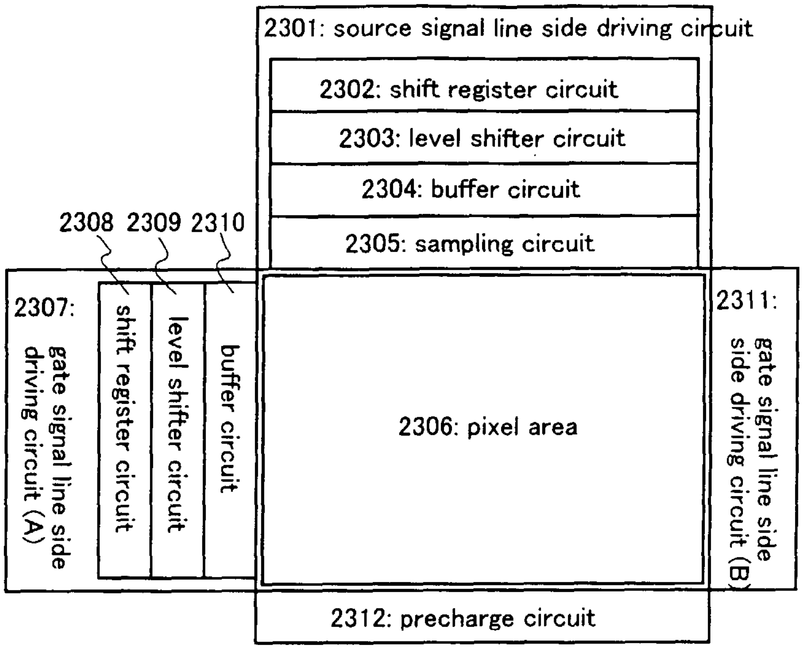

2301: source signal line side driving circuit
2302: shift register circuit
2303: level shifter circuit
2304: buffer circuit
2305: sampling circuit
2308
2309
2310
2307:
gate signal line side driving circuit (A)
shift register circuit
level shifter circuit
buffer circuit
2306: pixel area
2311:
gate signal line side driving circuit (B)
2312: precharge circuit

Fig. 23

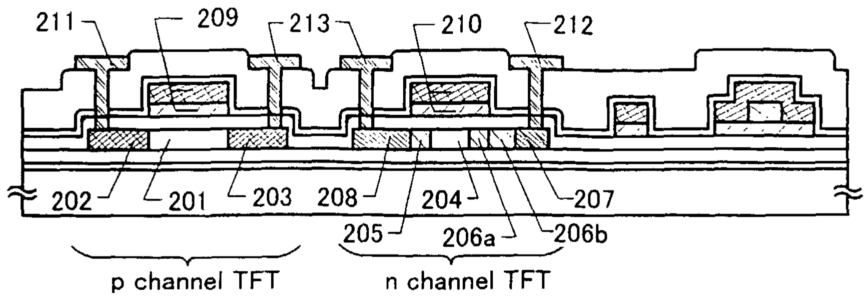


Fig. 24(A) Example of Construction of TFT in a Shift Register Circuit

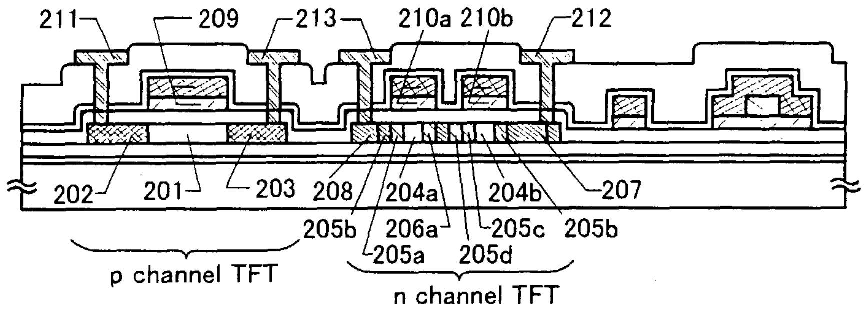


Fig. 24(B) Example of Construction of TFT in a Level Shifter Circuit and a Buffer Circuit

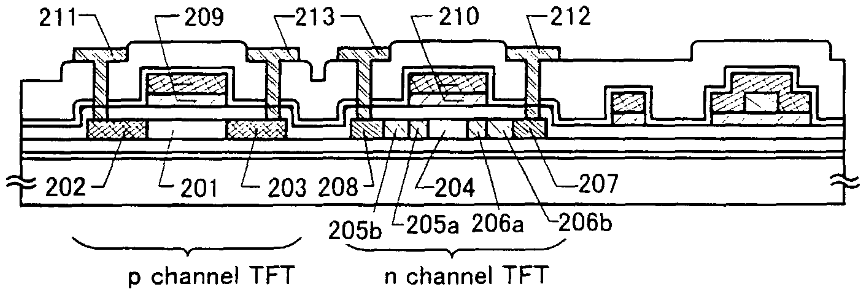


Fig. 24(C) Example of Construction of TFT in a Sampling Circuit

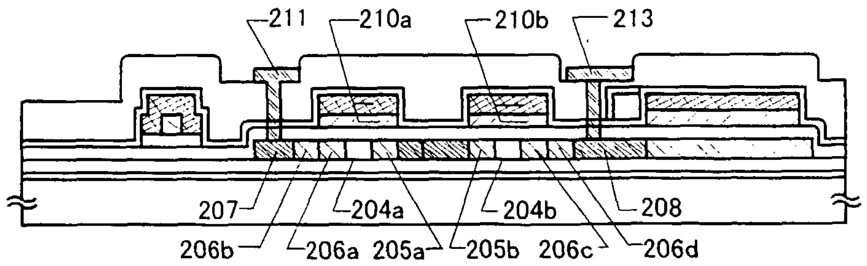


Fig. 24(D) Example of Construction of TFT in a Pixel Matrix Circuit

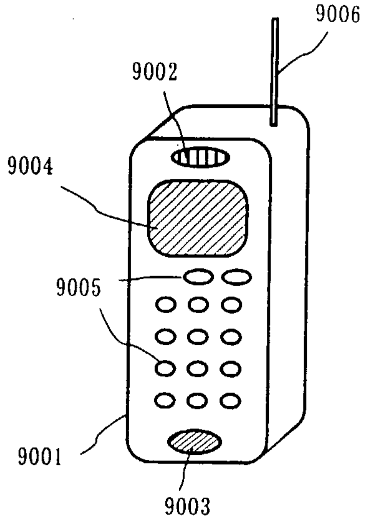


Fig. 25(A)

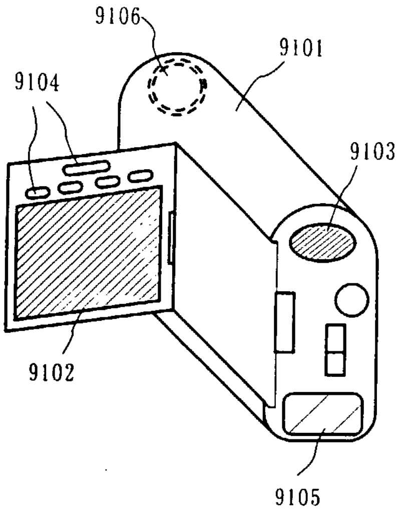


Fig. 25(B)

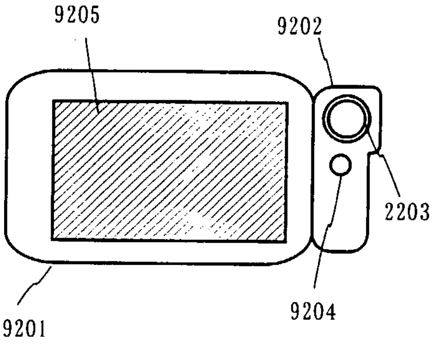


Fig. 25(C)

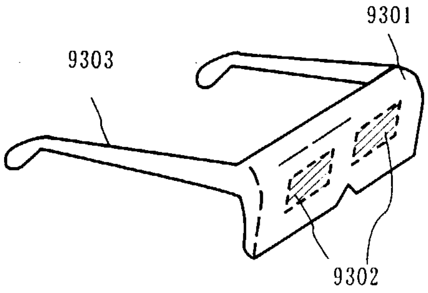


Fig. 25(D)

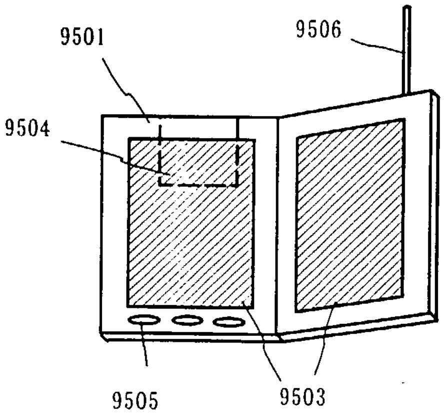


Fig. 25(E)

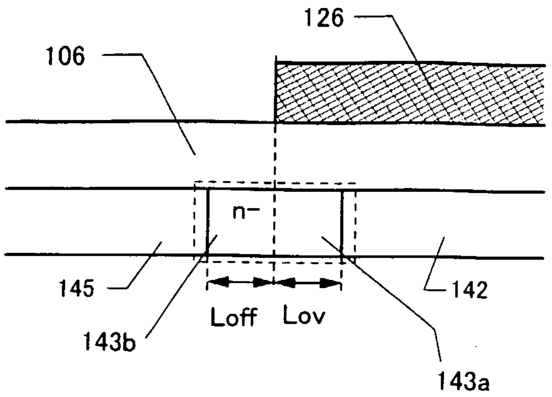


Fig. 26(A)

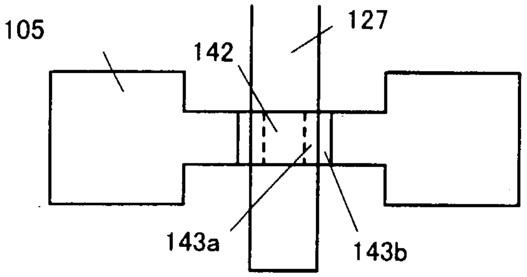


Fig. 26(B)

Example of Design Value

	TFT supply voltage	channel length μm	Lov μm	Loff μm
TFT of driver buffer circuit area	(16±2)V	5.0±1.5	2.5±0.3	2.5±0.5
	(20±3)V	5.0±2.0	3.0±0.5	3.0±0.5
TFT of shift register circuit area	(5±1)V	3.0±1.0	0.5±0.3	0.5±0.3
	(10±1)V	3.5±1.0	2.0±0.3	1.0±0.5
TFT of analog switching area	(16±2)V	3.0±1.0	1.5±0.5	1.5±0.5
TFT of pixel circuit area	(16±2)V	3.0±1.0	1.5±0.5	1.5±0.5

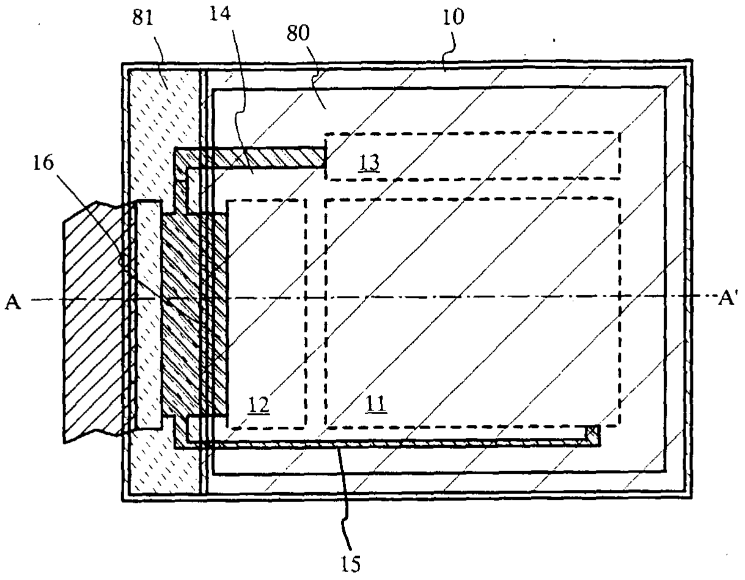


Fig. 27(A)

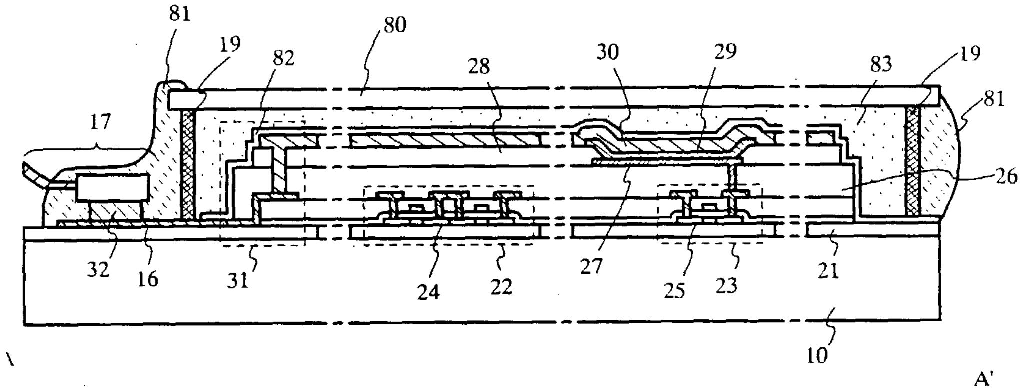


Fig. 27(B)

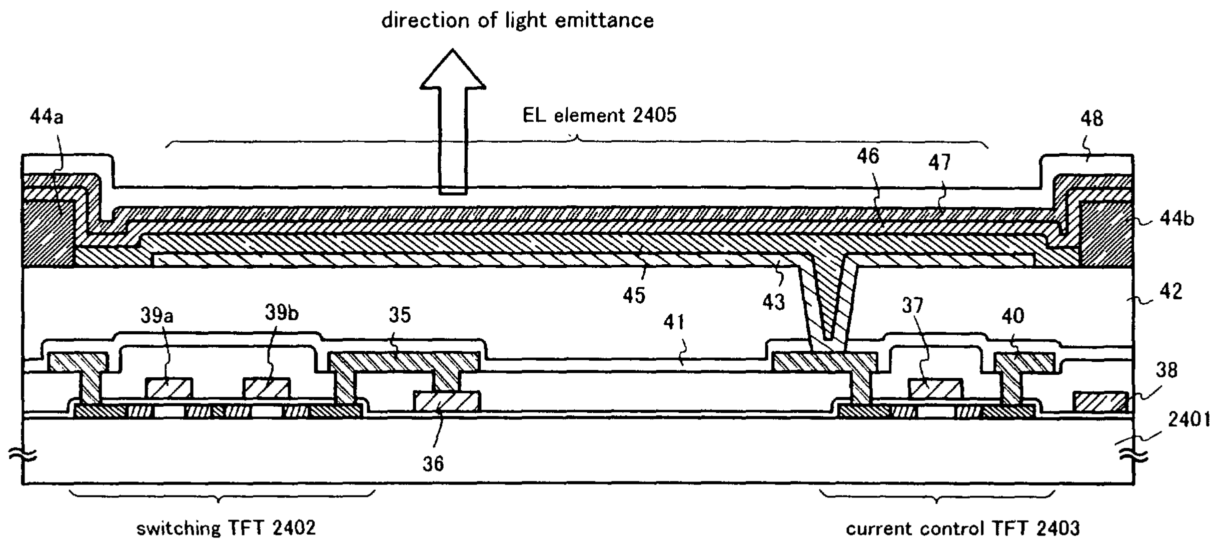

direction of light emittance
44a
EL element 2405
48
46
47
44b
42
45
43
39a
39b
35
41
37
40
38
2401
36
switching TFT 2402
current control TFT 2403

Fig. 28

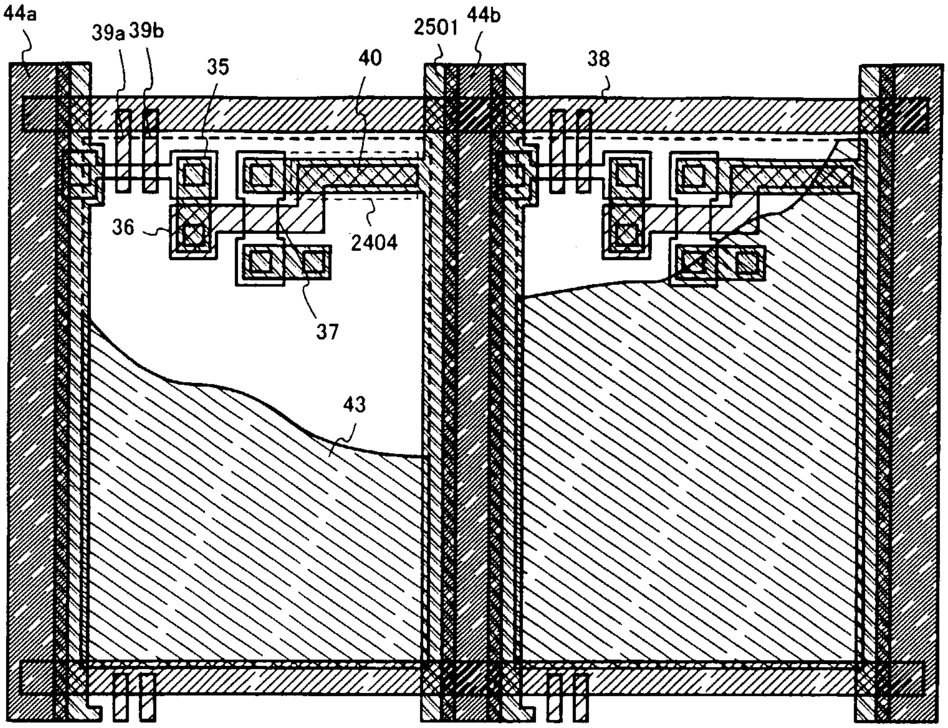


Fig. 29(A)

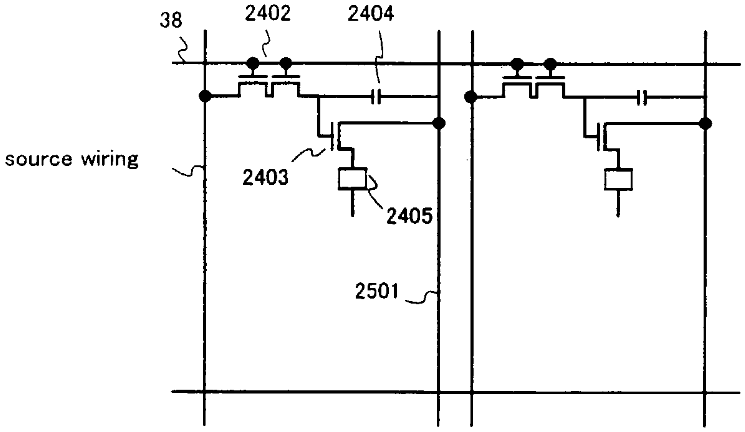


Fig. 29(B)

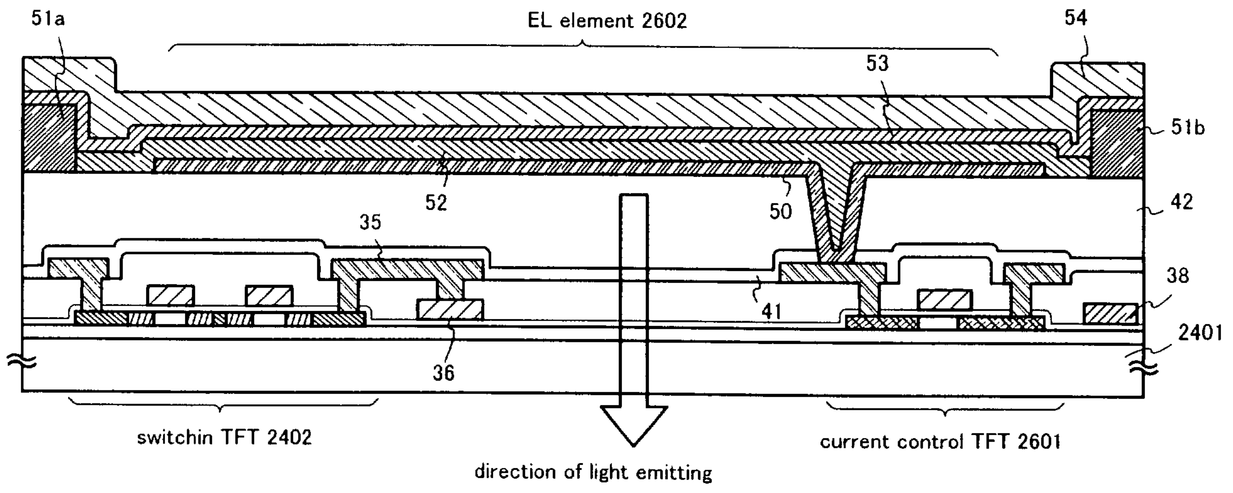

51a
EL element 2602
54
53
51b
52
50
42
35
38
41
2401
36
switchin TFT 2402
current control TFT 2601
direction of light emitting

Fig. 30

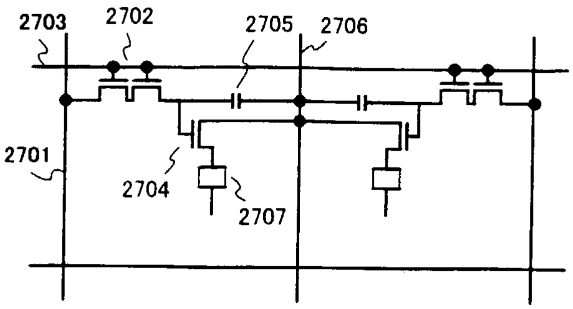


Fig. 31(A)

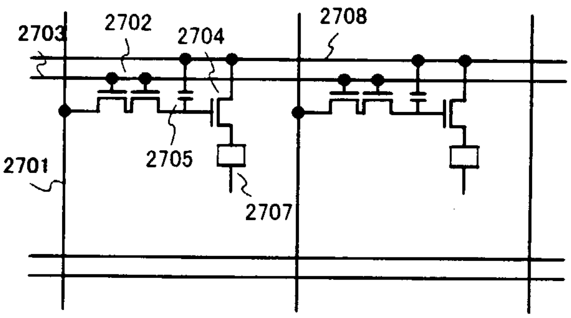


Fig. 31(B)

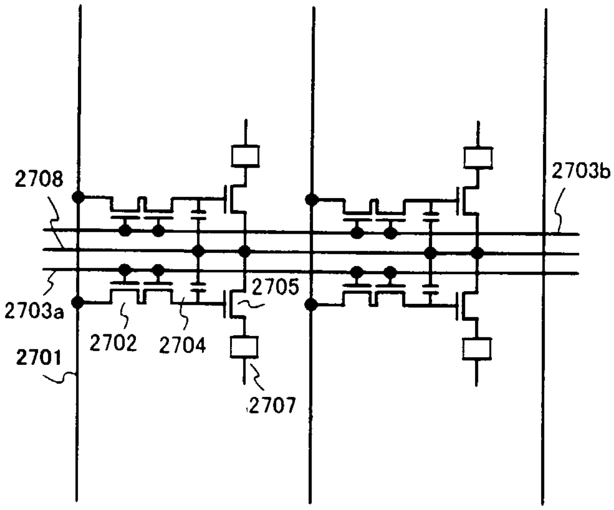


Fig. 31(C)

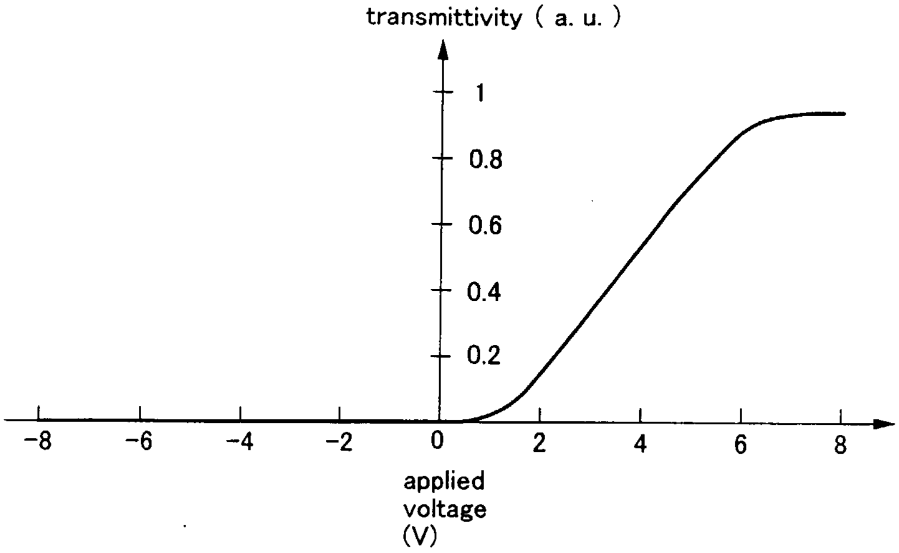
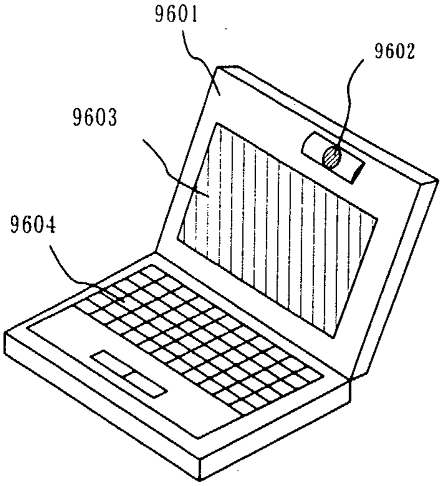


Fig. 32



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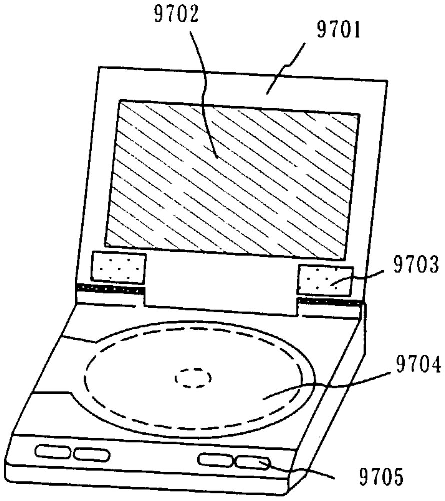


Fig. 33(B)

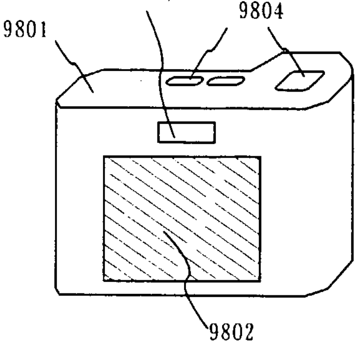


Fig. 33(C)

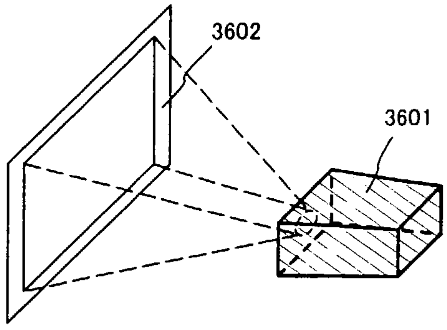
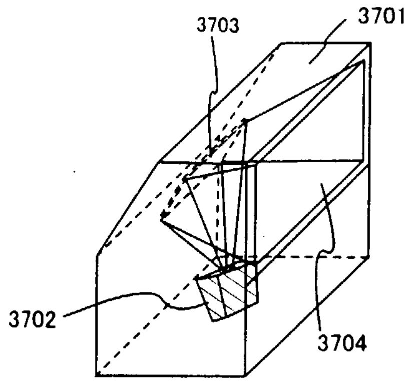


Fig. 34(A)



(B)

Fig. 34(B)

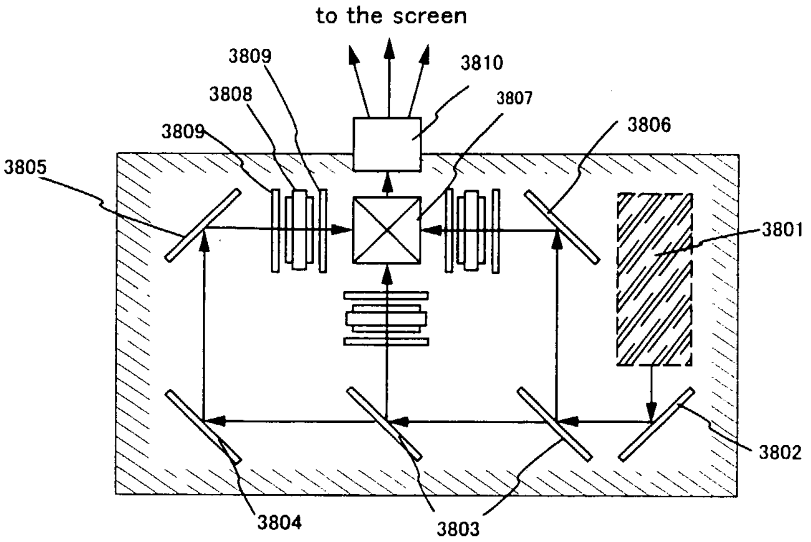


Fig. 34(C)

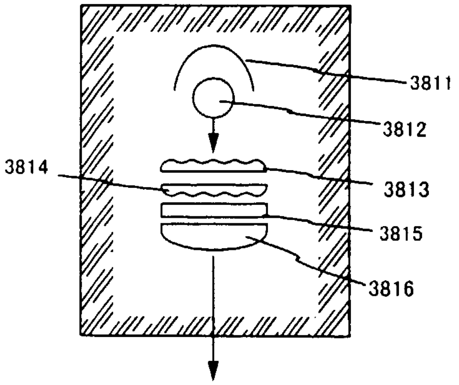
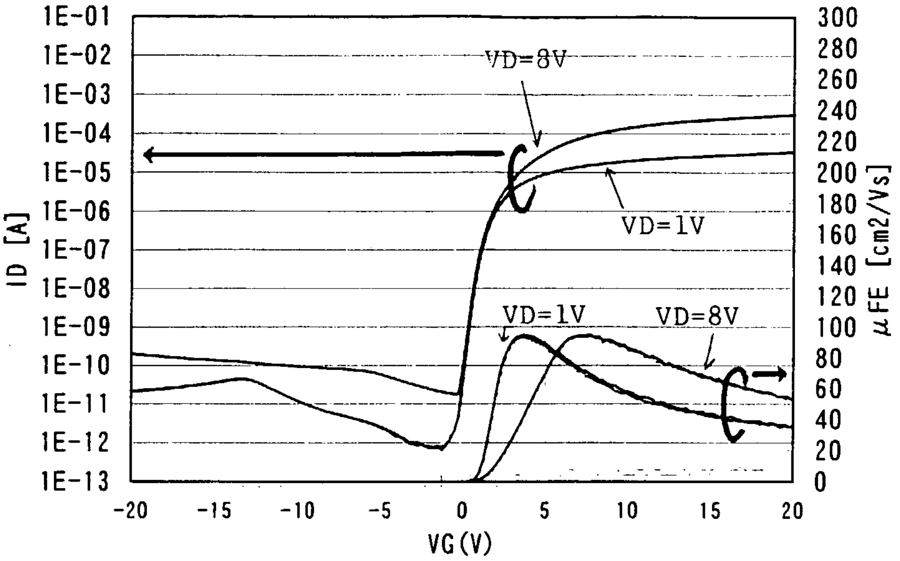


Fig. 34(D)



1E-01
1E-02
1E-03
1E-04
1E-05
1E-06
1E-07
1E-08
1E-09
1E-10
1E-11
1E-12
1E-13
ID [A]
300
280
260
240
220
200
180
160
140
120
100
80
60
40
20
0
μFE [cm2/Vs]
-20
-15
-10
-5
0
5
10
15
20
VG(V)
VD=8V
VD=1V
VD=1V
VD=8V

Fig. 35

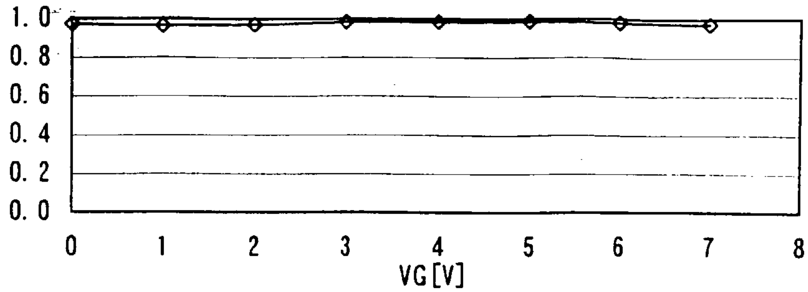


Fig. 36(A)

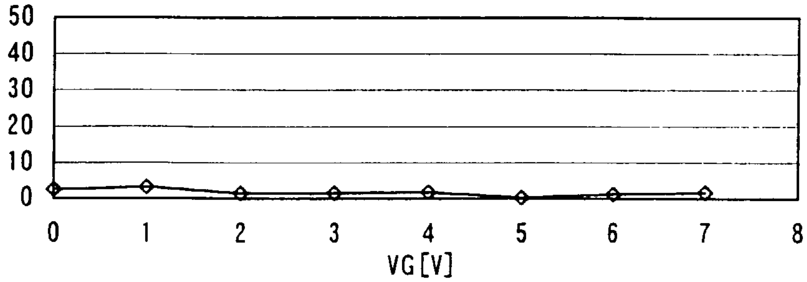


Fig. 36(B)

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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
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PJL
6/30/00

Continuing Data as Claimed by Applicant

Foreign Applications

JAPAN 11-033667 02/12/1999

If Required, Foreign Filing License Granted 04/07/2000

Title

Semiconductor device and method of manufacturing the same

Preliminary Class

257

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device having a circuit constituted by thin-film transistors (hereinafter referred to as TFTs). More particularly, the invention relates to an electronic device as represented by, for example, a liquid crystal display and to an electric appliance using such an electronic device as a display unit. In this specification, the semiconductor device refers to devices in general that work by utilizing the semiconductor characteristics. Therefore, electronic devices, semiconductor circuits and electric appliances are all semiconductor devices.

2. Description of the Related Art

Thin-film transistors (TFTs) can be formed on a transparent substrate and, hence, development has been positively forwarded for applying them to the active matrix-type liquid crystal display (hereinafter referred to as AM-LCD). The TFT using a crystalline semiconductor film (typically, a polysilicon film) exhibits a high mobility, and makes it possible to realize a highly precise image display by integrating functional circuits on the same board.

The AM-LCD basically comprises a pixel unit for displaying a picture, a gate drive circuit for driving TFTs of the pixels arranged in the pixel unit, and a source drive circuit (or a data drive circuit) for sending pixel signals to the TFTs, that are formed on the same substrate. In this specification, the gate drive circuit and the source drive circuit are all referred to as drive circuit units.

In recent years, there has been proposed a system-on-panel in which signal processing circuits such as signal-dividing circuit and Υ-correction circuit, too, are formed on the same substrate in addition to the pixel unit and the drive circuit unit.

However, the pixel unit and the drive circuit unit require different circuit performances, and it is difficult to satisfy all circuit specifications by the TFTs of the same structure. That is, the structure of the TFT has not yet been established to simultaneously satisfy the TFTs (hereinafter referred to as pixel TFTs) that constitute the drive circuit unit such as shift register circuit which gives importance on the high-speed operation and that also constitute the pixel unit which gives importance on the high breakdown voltage characteristics.

The present applicant therefore has filed an application covering a constitution in which the gate insulating film has a different thickness depending upon the TFTs (hereinafter referred to as drive TFTs) forming the drive circuit unit and the pixel TFTs (Japanese Patent Laid-Open No. 10-056184). Concretely speaking, in the above application, the thickness of the gate insulating film of the drive TFTs is decreased to be smaller than the thickness of the gate insulating film of the pixel TFTs.

In recent years, each pixel in the pixel unit has been formed having an area as very small as about 18 μm x 18 μm to realize a picture of as highly fine as XGA (eXtended Graphics Array, which is 1024 x 768 pixels) on a liquid crystal panel having a diagonal of 0.9 inch. It is expected that the size of the pixels will be further reduced in the future.

The greatest problem that stems from a reduction in the size of the pixels is a decrease in the numerical aperture in the transmission-type liquid crystal display. That is, the effective area for displaying the picture decreases, and the brightness decreases. If it is attempted to increase the numerical aperture, a countermeasure must be taken, such as decreasing the area occupied by the TFTs or decreasing the area occupied by the storage capacitors.

Thus, performance required for the TFTs and occupied areas are placed under very severe conditions accompanying a reduction in the size of the pixels and, besides, areas occupied by the storage capacitors are placed under severe conditions, too, making it very difficult to design the structure of the pixels.

SUMMARY OF THE INVENTION

The present invention was accomplished in view of the problems described above, and provides the structure of a pixel in which a highly reliable TFT is formed using a small area and the area occupied by the storage capacity is suppressed to a minimum degree. Thus, a bright and highly fine image picture is realized even by an electronic device of a pixel size which is as very small as a square of several tens of microns.

The invention further improves operation performance and reliability of the electronic device by suitably designing the structure of the TFTs arranged in the circuits depending on the functions of the circuits.

The invention further enhances operation performance and reliability of a semiconductor device (electric appliance) that uses the above electronic device (typically, a liquid crystal display, an electroluminescence display, an electrochromics display or a field emission display) as a display unit (display).

The constitution of the invention disclosed in this specification is concerned with a semiconductor device including a pixel unit and a drive circuit unit on the same substrate, wherein LDD regions of drive TFTs forming the drive circuit unit are so arranged as will be overlapped on the gate wirings of the drive TFTs to sandwich the gate-insulating films of the drive TFTs therebetween, LDD regions of pixel TFTs forming the pixel unit are so arranged as will not be overlapped on the gate wiring layers of the pixel TFTs so will not to sandwich the gate insulating films of the pixel TFTs therebetween, and the storage capacitors of the pixel unit are formed by a light-shielding film formed over the pixel TFTs, an oxide of the light-shielding film and pixel electrodes.

The constitution of the invention related to the method of manufacturing comprises:

a step for forming a channel-forming region, a source region, a drain region, and an LDD region sandwiched between the drain region and the channel-forming region in the active layers of NTFTs forming the drive circuit unit:

a step for forming a channel-forming region, a source region and a drain region in the active layers of PTFTs forming the drive circuit unit; and

a step for forming a channel-forming region, a source region, a drain region, and an LDD region sandwiched between the drain region and the channel-forming region in the active layers of pixel TFTs forming the pixel unit; wherein

the LDD regions of the NTFTs forming the drive circuit unit are so formed as will be overlapped on the gate wirings of the NTFTs forming the drive circuit unit to sandwich the gate-insulating films therebetween;

the LDD regions of the pixel TFTs are so formed as will not to be overlapped on the gate wirings of the pixel TFTs so will not to sandwich the gate insulating films therebetween; and

the storage capacitors in the pixel unit are formed by a light-shielding film formed over the pixel TFTs, an oxide of the light-shielding film and pixel electrodes.

More concretely, the invention is concerned with a method of manufacturing a semiconductor device which includes a pixel unit and a drive circuit unit on the same substrate, comprising:

a first step for forming an active layer on the substrate;

a second step for forming a gate-insulating film on the active layer;

a third step for forming an electrically conducting film on the gate-insulating film;

a fourth step for forming gate wirings of NTFTs that form the drive circuit unit by patterning the electrically conducting film;

a fifth step for forming n-regions in the active layers of NTFTs forming the drive circuit unit by adding an element belonging to the Group 15 of periodic table using the gate wirings of the NTFTs forming the drive circuit unit as a mask;

a sixth step for forming n^--regions under the gate wirings of the NTFTs forming the drive circuit unit by diffusing the n-regions by heat treatment;

a seventh step for forming gate wirings of the pixel TFTs forming the pixel unit by patterning the electrically conducting film;

an eighth step for forming n^{--}-regions in the active layers of the pixel TFTs by adding an element belong to the Group 15 of periodic table by using the gate wirings of the pixel TFTs as a mask;

a ninth step for forming n^+-regions in the active layers of NTFTs forming the drive circuit unit and in the active layer of the pixel TFTs by adding an element belonging the Group 15 of periodic table;

a tenth step for forming gate wirings of the PTFTs forming the drive circuit unit by patterning the electrically conducting film;

an eleventh step for forming p^+-regions in the active layers of PTFTs forming the drive circuit unit by adding an element belong to the Group 13 of periodic table by using the gate wirings of PTFTs forming the drive circuit unit as a mask;

a twelfth step for forming a interlayer-insulating film which is a resin film over the NTFTs and PTFTs forming the drive circuit unit and over the pixel TFTs forming the pixel unit;

a thirteenth step for forming a light-shielding film on the interlayer-insulating film;

a fourteenth step for forming an oxide of the light-shielding film on the surface of the light-shielding film; and

a fifteenth step for forming pixel electrodes in contact with the oxide of the light-shielding film and overlapped on the light-shielding film.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a view illustrating the structure of an AM-LCD in cross section;

Figs. 2A to 2D are views illustrating the steps for manufacturing the AM-LCD:

Figs. 3A to 3D are views illustrating the steps for manufacturing the AM-LCD;

Figs. 4A to 4D are views illustrating the steps for manufacturing the AM-LCD;

Figs. 5A and 5B are views illustrating the steps for manufacturing the AM-LCD;

Fig. 6 is a view illustrating a relation of concentration distribution of when impurity elements are added;

Figs. 7A and 7B are views illustrating the structure of a common potential-drawing terminal;

Figs. 8A and 8B are views illustrating the structure of a common potential-drawing terminal;

Figs. 9A to 9D are views illustrating the block constitution and circuit arrangement of the AM-LCD;

Fig. 10 is a view illustrating the structure of a drive TFT (CMOS circuit);

Fig. 11 is a view illustrating the appearance of the AM-LCD;

Figs. 12A and 12B are views illustrating the structure of a CMOS circuit in cross section;

Fig. 13 is a view illustrating the structure of a pixel unit in cross section;

Figs. 14A and 14B are views illustrating the structure of a pixel unit in cross section;

Figs. 15A and 15B are views illustrating the structure of the upper surface of the pixel unit;

Figs. 16A and 16B are views illustrating the steps for manufacturing the AM-LCD;

Fig. 17 is a view illustrating the circuit constitution of an active matrix-type EL display;

Figs. 18A and 18B are views illustrating the structure of the upper surface of the EL display device and the structure of the EL display device in cross section;

Figs. 19A to 19C are views illustrating the constitution of a pixel unit in the EL display device;

Figs. 20A to 20F are views illustrating electric appliances;

Figs. 21A to 21D are views illustrating electric appliances; and

Figs. 22A and 22B are views illustrating the structure of an optical engine.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the invention will now be described with reference to Fig. 1 which is a sectional view illustrating an AM-LCD in which a drive circuit unit and a pixel unit are formed integrally together on the same substrate. Here, a CMOS circuit is shown as a representative basic circuit for constituting the drive circuit unit, and TFTs of a double-gate structure are shown as pixel TFTs. It is allowable to use a triple-gate structure or a single-gate structure not being limited to the double-gate structure only, as a matter of course.

In Fig. 1, reference numeral 101 denotes a substrate having heat resistance, which may be a quartz substrate, a silicon substrate, a ceramics substrate or a metal substrate (typically, a stainless steel substrate). Whichever substrate is used, a base film (preferably, an insulating film comprising chiefly silicon) may be formed, as required.

Reference numeral 102 denotes a silicon oxide film formed as a base film on which are formed active layers of drive TFTs, active layers of pixel TFTs and semiconductor layers serving as lower electrodes of the storage capacitors. In this specification, the "electrode" is part of the "wiring", and represents a portion where it is electrically connected to other wiring or intersects the semiconductor layer. Therefore, though the words "wiring" and "electrode" are used separately for the sake of explanation, it should be noted that the "electrode" is always included in the word "wiring".

In Fig. 1, the active layer of the drive TFT is formed by a source region 103, a drain region 104, an LDD (lightly doped drain) region 105 and a channel-forming region 106 of an N-channel TFT (hereinafter referred to as NTFT), and by a source region 107, a drain region 108 and a channel-forming region 109 of a P-channel TFT (hereinafter referred to as PTFT).

Further, the active layer of the pixel TFT (an NTFT is used here) is formed by a source region 110, a drain region 111, LDD regions 112a to 112d and channel-forming regions 113a, 113b. Reference numeral 114 denotes an impurity region of a high concentration existing between the channel-forming regions 113a and 113b, and has the same composition as the source region 110 and the drain region 111 (contains the same impurity at the same concentration). This region works as a stopper region for preventing the minority carriers generated at a drain terminal from migrating into the source region, that could become a cause of off current.

A gate-insulating film is formed to cover the active layer. In this invention, the gate-insulating film 115 of the drive TFT is formed having a thickness smaller than that of the gate insulating film 116 of the pixel TFT. Typically, the gate-insulating film 115 is formed maintaining a thickness of from 5 to 50 nm (preferably, from 10 to 30 nm) and the gate-insulating film 116 is formed maintaining a thickness of from 50 to 200 nm (preferably, from 100 to 150 nm).

The gate-insulating film of the drive TFT needs to be limited to the one of a single thickness. That is, the drive TFTs having dissimilar insulating films may exist in the drive circuit unit. In this case, at least three or more kinds of TFTs having dissimilar gate-insulating materials exist on the same substrate.

Next, gate wirings 117 and 118 of the drive TFT and the gate electrodes 119a, 119b of the pixel TFT are formed on the gate-insulating films 115 and 116. A heat resistant electrically conducting film that withstands the temperature of 800 to 1150 °C (preferably 900 to 1100 °C) is used as a material for forming the gate wirings 117 to 119.

Typically, there may be used an electrically conducting silicon film (e.g., phosphor-doped silicon film, boron-doped silicon film, etc.), a metal film (e.g., tungsten film, tantalum film, molybdenum film, titanium film), a silicide film formed by transforming the metal film into a silicide thereof, or a nitrogenated film thereof (tantalum nitride film, tungsten nitride film, titanium nitride film, etc.). Or, these films may be laminated by freely combining them.

When the metal film is to be used, it is desired to employ a laminated structure with the silicon film in order to prevent the oxidation of the metal film (which increases the wiring resistance). From the standpoint of preventing oxidation, further, a structure is effective in which the metal film is covered with an insulating film containing silicon.

As the insulating film containing silicon, there can be used a silicon oxide film, a silicon nitride film, or a silicon oxynitride film. The silicon oxynitride film stands for an insulating film containing oxygen, nitrogen and silicon at a predetermined ratio.

An insulating film containing silicon may be formed as the uppermost layer at the time of forming the gate wiring using the above material, and the gate wiring pattern may be formed by etching the insulating film containing silicon and the above material at one time. In this case, the upper surface only of the gate wiring is protected by the silicon-containing insulating film.

Further, the laminated structure of the metal silicide film and the silicon film exhibits an increased heat resistance and is strong against the oxidation though the resistance increases to some extent as compared with when the metal film is used. In this case, the protection film is not particularly needed for preventing the oxidation. Despite the oxidation takes place, a silicon oxide film is simply formed on the surface, but the wiring resistance does not increase.

Reference numeral 120 denotes a first interlayer-insulating film (lower layer) and 121 denotes a first interlayer-insulating film (upper layer), which are formed of a silicon-containing insulating film. Upon them are formed source wirings 122 and 123 and drain wiring 124 of the drive TFT, or source wiring 125 and drain wiring 126 of the pixel TFT.

A passivation film 127 is formed thereon. The passivation film 127 has an opening 128 formed on the drain wiring 126, and a second interlayer-insulating film 129 is formed so as to cover them. A resin film having a small dielectric constant is desired as the second interlayer-insulating film 129. As the resin film, there can be used a polyimide film, an acrylic film, a polyamide film, a BCB (benzocyclobutene) film, and MSSQ (methyl silsesquioxane).

A light-shielding film 130 which is an aluminum film or a film comprising chiefly aluminum (film formed by adding other elements as impurities to the aluminum film) is formed on the second interlayer-insulating film 129, and on the surface thereof is formed an oxide (alumina film) 131 formed by oxidizing the light-shielding film 130. It is desired that the light-shielding film 130 is tapered at about 60 to 85 degrees for being patterned. The oxide 131 may be formed by the anodic oxidation method, hot oxidation method or plasma oxidation method. Examples of other elements used as impurities include titanium, scandium, neodymium and silicon.

A contact hole is formed in the second interlayer-insulating film 129 and, then, a pixel electrode 132 is formed. The pixel electrode 132 is electrically connected to the drain wiring 126 through the contact hole. Here, a transparent electrically conducting film may be used as a pixel electrode when the transmission-type AM-LCD is to be manufactured and a metal film having a high reflection factor may be used when the reflection-type AM-LCD is to be manufactured.

A storage capacity using the oxide 131 as a dielectric is formed in a region where the light-shielding film 130 and the pixel electrode 32 are overlapped one upon the other. The oxide 131 is an alumina film and has a dielectric constant of as large as 8 to 10, and has a thickness of as small as 30 to 100 nm (preferably, 50 to 70 nm) forming a large capacity despite of its small area.

The contact hole through which the pixel electrode 132 is electrically connected to the drain wiring 126 forms a gap in the light-shielding film and permits light to pass through. However, the underlying drain wiring 126 completely prevents the leakage of light.

Further, the pixel electrode 132 is covered with an alignment film 133. A liquid crystal 134 is held on the alignment film 133. The liquid crystal 134 is held on the pixel unit by a sealing member (not shown) that also works as a spacer relative to the opposing substrate.

On the liquid crystal 134 are provided an alignment film 135 on the side of the opposing substrate, an opposing electrode (also referred to as common electrode) 136 comprising a transparent electrically conducting film, and a glass substrate 137. The alignment film 135, opposing electrode and glass substrate 137 are collectively referred to as the opposing substrate. In the single-plate type liquid crystal display, a color filter is further provided on the side of the opposing substrate.

The semiconductor device of the invention having the above structure features the following points.

First, among the drive TFTs basically forming the drive circuit unit, the NTFT has the structure in which the LDD region 105 is completely overlapped on the gate wiring 117. This is to cope with the hot carriers like in the widely-known GOLD (Gate-Drain Overlapped LDD) structure. The PTFT, on the other hand, is little deteriorated by the hot carriers and may have the existing structure.

Further, a feature resides in that the gate-insulating film 115 of the drive TFT has a thickness which is about one-fifth to one-tenth that of the gate-insulating film 116 of the pixel TFT. This is to increase the operation speed. Since the operation voltage is low, the gate-insulating film may have a thickness of 5 to 50 nm.

The pixel TFT has basic circuit specifications which are different from those of the drive TFT. First, suppressing the off current (drain current that flows when the TFT is in the off state) takes precedence over the operation speed. Therefore, an ordinary LDD structure is employed. This makes a difference in the structure from the drive TFT in regard to that the LDD regions 112a to 112d are not overlapped on the gate wirings 119a and 119b.

Further, a high voltage of a maximum of about 16 V is applied to the gate-insulating film 116. Therefore, a countermeasure is taken for increasing the breakdown voltage by selecting the film thickness to be from 50 to 200 nm (preferably, from 100 to 150 nm).

The feature further resides in that the storage capacity is formed by using the oxide 131 formed on the light-shielding film 130 as a dielectric, in order to enhance the numerical aperture. The storage capacity is formed by the light-shielding film 130, oxide 131 and pixel electrode 132.

As described above, the semiconductor device of the invention has a variety of features in the drive circuit unit and in the pixel unit, forms a bright and highly fine picture owing to the synergistic effect of the features, making it possible to provide an electronic device that features high operation performance and high reliability. The invention further provides an electric appliance of high performance mounting the above electronic device as a part.

The thus constituted invention will now be described in further detail by way of embodiments.

[Embodiment 1]

This embodiment explains, with reference to Figs. 2A to 5B, the steps of manufacturing for realizing the structure of Fig. 1 described earlier.

First, a quartz substrate 201 is prepared, and on which are continuously formed a silicon oxide film 202 having a thickness of 20 nm and an amorphous silicon film 203 without exposing them to the open atmosphere. This prevents impurities such as boron and the like contained in the atmosphere from being adsorbed by the lower surface of the amorphous silicon film (Fig. 2A).

Though this embodiment uses an amorphous silicon film, any other semiconductor film may be used. There may be used a microcrystalline silicon film or an amorphous germanium film. The film is so formed as will finally has a thickness of from 25 to 40 nm by taking into consideration the subsequent step of thermal oxidation.

Next, the amorphous silicon film is crystallized. This embodiment employs technique disclosed in Japanese Patent Laid-Open No. 9-312260 as crystallization means. The technique disclosed in this publication uses an element selected from nickel, cobalt, palladium, germanium, platinum, iron, copper, tin and lead as a catalytic element for assisting the crystallization.

In this embodiment, nickel is selected as a catalytic element, a layer (not shown) containing nickel is formed on the amorphous silicon film 203 and is crystallized through the heat treatment at 550 °C for 4 hours. Thus, a crystalline silicon (polysilicon) film 204 is formed (Fig. 2B).

Here, an impurity element (phosphorus or boron) may be added to the crystalline silicon film 204 to control the threshold voltage of the TFT. Both phosphorus and boron may be added, or either one of them may be added. Here, if phosphorus is added in advance to the region that finally serves as the first capacitor electrode of the storage capacity, then, this region can be used as an electrode, which is desirable.

Next, a masking film 205 which is a silicon oxide film is formed maintaining a thickness of 100 nm on the crystalline silicon film 204, and a resist mask 206 is further formed thereon. The masking film 205 is etched using the resist mask 206 as a mask thereby to form openings 207 and 208.

In this state, an element (phosphorus in this embodiment) belonging to the Group 15 of periodic table is added to form phosphorus-doped regions (phosphorus-added regions 209 and 210. The concentration of phosphorus that is added is desirably from 5×10^{18} to 1×10^{20} atoms/cm^3 (preferably, 1×10^{19} to 5×10^{19} atoms/cm^3). Here, however, the concentration of phosphorus to be added varies depending upon the temperature and time in a subsequent gettering step and upon the area of the phosphorus-doped region, and is in no way limited within this range (Fig. 2C).

Next, the resist mask 206 is removed and is heat-treated at 450 to 650 °C (preferably, 500 to 600 °C) for 2 to 16 hours to getter nickel remaining in the crystalline silicon film. The gettering action is obtained requiring a temperature of about ±50 °C from a maximum temperature of thermal hysteresis. Here, since the heat treatment for crystallization is effected at 550 to 600 °C, the gettering action is obtained to a sufficient degree by the heat treatment at 500 to 650 °C.

In this embodiment, the heat treatment is effected at 600 °C for 8 hours, whereby nickel migrates in the directions of arrows (see Fig. 2D) so as to be gettered in the phosphorus-doped regions 209 and 210. Thus, the concentration of nickel remaining in the crystalline silicon films denoted by 211a and 211b decreases down to 2×10^{17} atoms/cm^3 or smaller (preferably, 1×10^{16} atoms/cm^3 or smaller). This concentration, however, is the result of measurement by the mass secondary ionic analysis (SIMS), and the concentration lower than this value has not at present been confirmed due to limitation of the measurement (Fig. 2D).

After the step of nickel gettering has been finished as described above, the crystalline silicon films 211a and 211b are patterned to form an active layer (semiconductor layer) 212 of the CMOS circuit and an active layer 213 of the pixel TFT. In this case, it is desired to completely remove the phosphorus-added region that has trapped nickel.

Then, an insulating film (not shown) is formed by the plasma CVD method or the sputtering method, and is patterned to form a gate-insulating film 214. The gate-insulating film is the one that serves as the gate-insulating film for the pixel TFT, and has a thickness of 50 to 200 nm. This embodiment uses a silicon oxide film having a thickness of 80 nm. There may be used other silicon-containing insulating film in the form of a single layer or laminated layers (Fig. 3A).

Here, the gate-insulating film 214 that is formed is allowed to remain on the pixel TFT but is removed from the region where the CMOS circuit is to be formed. Though this embodiment refers to the CMOS circuit only, the gate-insulating film, in practice, is removed from the region on where part of the drive circuit unit (group of circuits that must operate at high speeds) is to be formed. As far as the circuit in which a high voltage is applied to the gate-insulating film, such as a buffer circuit, is concerned, therefore, it is desired to leave the insulating film having a thickness equal to that of the gate-insulating film 214.

Next, the heat treatment is effected at a temperature of from 800 to 1150 °C (preferably, from 900 to 1100 °C) for 15 minutes to 8 hours (preferably, 30 minutes to 2 hours) in an oxidizing atmosphere (step of thermal oxidation). In this embodiment, the heat-treatment is effected in an oxygen atmosphere at 950 °C for 30 minutes.

The oxidizing atmosphere may be a dry oxygen atmosphere or a wet oxygen atmosphere. However, the dry oxygen atmosphere is suited for decreasing crystal defects in the semiconductor layer. It is further allowable to use an oxygen atmosphere which contains a halogen element. The effect for removing nickel can be expected through the step of thermal oxidation in an atmosphere containing a halogen element.

Through the step of thermal oxidation as described above, a silicon oxide film (thermally oxidized film) 215 is formed maintaining a thickness of from 5 to 50 nm (preferably, from 10 to 30 nm) on the portion where the gate-insulating film 214 was not formed (portion where the active layer is exposed). In this embodiment, the silicon oxide film 215 is formed maintaining a thickness of 30 nm, and finally serves as a gate-insulating film for the CMOS circuit.

The oxidation reaction also proceeds even on an interface between the gate-insulating film 214 which is the silicon oxide film remaining on the pixel TFT and the semiconductor layer 213 formed thereunder. Finally, therefore, the thickness of the gate-insulating film 216 of the pixel TFT becomes 50 to 200 nm (preferably, from 100 to 150 nm). In this embodiment, the thickness becomes 110 nm.

In this embodiment, the silicon oxide film 215 is formed by the thermal oxidation method. The thin silicon oxide film, however, may be formed by a low-pressure thermal CVD method. In this case, the film-forming temperature may be about 800 °C, and the film-forming gas may comprise silane and oxygen.

The step of thermal oxidation is followed by the formation of an electrically conducting film comprising a silicon film/tungsten silicide film of a laminated structure. The electrically conducting film is then patterned to form a gate wiring 217 of the NTFT in the CMOS circuit. In this case, the electrically conducting film 218 of the above constitution is left on the region on where PTFT and pixel TFT of the CMOS circuit are to be formed (Fig. 3B).

In this constitution, the silicon film located under the electrically conducting film may have a thickness of from about 20 to about 70 nm. Here, it is desired to employ the low-pressure thermal CVD method for forming films. This is because, the gate-insulating film of the CMOS circuit has a very small thickness and, hence, employment of the sputtering method or the plasma CVD method may leave damage in the insulating film.

The material of the gate wiring that can be used in this embodiment is not limited thereto only, but may be any material described earlier, as a matter of course.

In this embodiment, the electrically conducting film 218 has a thickness of 300 nm.

After the electrically conducting film has been patterned, an element (phosphorus in this embodiment) belonging to the Group 15 of periodic table is added using the gate wiring 217 and resist mask (not shown) used for forming the electrically conducting film 218, as a mask, thereby to form impurity regions (hereinafter, these regions are referred to as n-regions) 219a and 219b.

In this invention, the impurity element for imparting the type of electric conduction may be added by the ion implantation method that effects mass separation or by the plasma doping method that does not effect mass separation.

In this case, the setpoint dosage is so adjusted that phosphorus is contained in the n-regions 219a and 219b at a concentration (the concentration is denoted by n) of from 1 x 10^{18} to 1 x 10^{19} atoms/cm^3. The concentration has an important meaning in the step of heat treatment executed next time.

Next, the resist mask that is not shown is removed, and the heat treatment is effected in a temperature range of from 700 to 1000 °C (preferably, from 800 to 900 °C) to activate phosphorus. At the same time, phosphorus is diffused in the transverse direction to form low-concentration impurity regions (hereinafter referred to as n^--regions) 220a and 220b overlapped on the gate wiring 217. The n^--regions 220a and 220b contain phosphorus at a concentration of from 5 x 10^{17} to 5 x 10^{18} atoms/cm^3 (Fig. 3C).

The diffusing distance of the impurities can be controlled depending on the temperature and time of the heat treatment. Therefore, the length (width) of the n^--type regions 220a and 220b can be freely controlled. In this embodiment, the overlapping distance is adjusted to be from 0.3 to 1 μm (preferably, from 0.5 to 0.7 μm).

Thus, the concentration in the n-regions 219a and 219b is determined depending on the activation conditions and the phosphorus concentration and length required by the

n^--regions.

Through the step of heat treatment, the active layer of the CMOS circuit is oxidized again, and the thickness of the gate-insulating film 215 increases. Under the heat-treating conditions for forming the above n^--regions, the thickness increases typically by 20 to 50 nm. However, an increase in the film thickness can be prevented by a cap layer and then effecting the heat treatment to prevent oxidation.

At the same time, further, the gate wiring 217 and electrically conducting film 218 are oxidized to form a thermally oxidized film on the surfaces thereof. When the laminated film of the silicon film and the metal silicide film is used as in this embodiment, silicon is preferentially oxidized on the surface. Accordingly, the thermally oxidized film that is formed is a silicon oxide film.

Next, the electrically conducting film 218 is patterned to form gate wirings 221a and 221b of the pixel TFT. Here, the electrically conducting film 222 is left on the PTFT in the CMOS circuit (Fig. 3D).

Then, an element (phosphorus in this embodiment) belonging to the Group 15 of periodic table is added using the gate wirings 217, 221a and 221b and electrically conducting film 222 as masks to form low-concentration impurity regions 223a to 223c containing phosphorus at a concentration of from 5×10^{16} to 1×10^{18} atoms/cm^3 (hereinafter referred to as n^{--}-regions). In this case, phosphorus is added to the above n-regions 219a and 219b, too. However, the concentration of phosphorus added is very lower than that of phosphorus that has been contained in the n-regions, and an increase in the amount of phosphorus imposes no problem.

In this embodiment, further, the n^{--}-regions are formed in order to increase the resistance as much as possible and to suppress the off current. In the step of adding phosphorus, therefore, it is also possible to from the n^--regions instead of the n^{--}-regions.

Further, this step may be separately effected for the drive circuit unit where the gate-insulating film has a small thickness and for the pixel unit where the gate-insulating film has a large thickness. Or, the step may be effected simultaneously. Here, however, the concentration in the LDD region must be carefully conducted. In this embodiment, therefore, the concentration of phosphorus that is added is distributed (concentration profile) as shown in Fig. 6 based on the plasma doping method.

In Fig. 6, the gate-insulating film 601 on the side of the drive circuit unit and the gate-insulating film 602 on the side of the pixel unit have different thicknesses. Therefore, the distribution of phosphorus concentration differs in the direction of depth.

In this embodiment, the conditions for adding phosphorus (acceleration voltage, etc.) are so adjusted that the concentration is distributed as designated at 603 on the side of the drive circuit unit and that the concentration is distributed as designated at 604 on the side of the pixel unit. In this case, though the concentration distribution differs in the direction of depth, the phosphorus concentration eventually becomes nearly equal between the low-concentration impurity regions 605 and 606.

The step shown in Fig. 6 can be employed in all steps for adding impurities described in this specification.

Next, resist masks 224, 225a and 225b are formed, an element (phosphorus in this embodiment) belong to the Group 15 of periodic table is added to form high-concentration impurity regions 226 to 230 containing phosphorus at a concentration of from 5×10^{19} to 1×10^{21} atoms/cm^3 (hereinafter referred to as n^+-regions)(Fig. 4A).

Through this step, the source region 226, drain region 227, LDD region 231 and channel-forming region 232 are defined for the NTFT in the CMOS circuit. Further, the source region 228, drain region 229, LDD regions 233a and 233b and channel-forming regions 234a and 234b are defined for the pixel TFT.

The n^+-region 230 works as a stopper region for preventing the migration of minority carriers (positive holes in this embodiment) that become a cause of off current. Here, if not particularly, required, the LDD regions 233a and 233b may be contacted to each other.

After the state of Fig. 4A is obtained, the electrically conducting film 222 remaining on the region where the PTFT of CMOS circuit will be formed is patterned to form a gate wiring 235. By using the resist masks 236a to 236c, an element (boron in this embodiment) belonging to the Group 13 of periodic table is added to form high-concentration impurity regions 237 and 238 containing boron at a concentration of from 5×10^{19} to 1×10^{21} atoms/cm^3 (hereinafter referred to as P^+-regions)(Fig. 4B).

Through this step, the source region 237, drain region 238 and channel-forming region 239 are defined for the PTFT in the CMOS circuit.

Thus, the formation of all impurity regions is finished. The order of adding impurities is not limited to the one described in this embodiment but may be changed in various ways. The order of adding impurities can be suitably determined by a person who conducts the process by taking into consideration problems associated with the performance of the device.

After the impurity regions have been formed, the resist masks 236a to 236c are removed. An insulating film (silicon-containing insulating film) 240 is formed maintaining a thickness of from 60 to 200 nm (preferably, from 100 to 150 nm) under the first interlayer-insulating film. This insulating film works as a protection film for protecting the gate wiring from being oxidized, and it is, hence, desired to use a silicon oxynitride film.

After the first interlayer-insulating film (lower layer) 240 is formed, the heat treatment is effected at a temperature over a range of from 550 to 800 °C for 1 to 8 hours.

In this embodiment, the heat treatment is conducted at 600 °C for 2 hours in a nitrogen atmosphere (Fig. 4C).

This step activates phosphorus or boron added to the impurity regions and, at the same time, recovers damage given to the gate-insulating film and to the active layer due to the addition of impurities. Here, it is desired to activate phosphorus or boron while suppressing their diffusion as much as possible. When it is necessary to heat at high temperatures, attention must be given to that phosphorus and boron in each TFT tend to diffuse into the channel-forming region.

Further, the hydrogenation treatment is effected at 350 °C for one hour. The hydrogenation treatment is to expose impurities to hydrogen excited by heat or plasma.

After the state of Fig. 4C is obtained, a first interlayer-insulating film (upper layer) 241 is formed. As the first interlayer-insulating film (upper layer) 241, there may be used a silicon-containing insulating film (silicon oxide film in this embodiment).

Next, a contact hole is formed in the first interlayer-insulating film (upper layer) 241 and in the first interlayer-insulating layer film (lower layer) 240, and an electrically conducting film (not shown) of a three-layer structure is formed sandwiching the aluminum alloy layer (aluminum film to which 1% by weight of titanium is added) by titanium films. The electrically conducting film is then patterned to form source wirings 242 and 243 and drain wiring 244 of the CMOS circuit, and to form source wiring 245 and drain wiring 246 of the pixel TFT. Concerning the pixel TFT, the source wiring and the drain wiring are alternately interchanged.

After the source wirings and the drain wirings are formed as described above, a silicon nitride film is formed maintaining a thickness of 300 nm as a passivation film 247, followed by the hydrogenation treatment at 300 °C for one hour. The hydrogenation treatment is for exposing to hydrogen excited by heat or plasma. In this step, hydrogen emitted from the passivation film 247 and hydrogen contained in large amounts in the first interlayer insulating film (lower layer) 240 diffuse downward due to the hydrogenation (do not diffuse upward being blocked by the passivation film 247), and the active layer is terminated with hydrogen.

As the passivation film 247, there can be used a silicon oxynitride film, a silicon oxide film or a laminated film of these silicon-containing insulting films in addition to the silicon nitride film. In this embodiment, further, the plasma treatment is effectively conducted using a hydrogen-containing gas (typically, an ammonia gas) as a pretreatment for forming the passivation film 247. Owing to the pretreatment, hydrogen activated (excited) by the plasma is confined by the passivation film 247. Upon effecting the hydrogenation treatment, the hydrogenation efficiency is very improved.

By adding a nitrous oxide gas in addition to the hydrogen-containing gas, further, the surface of the material to be treated is washed by water that is formed, making it possible to effectively prevent contamination due to boron and the like contained in the open air.

After the hydrogenation treatment, the passivation film 247 is removed from the drain wiring 246 to form an opening 248. Next, an acrylic film is formed maintaining a thickness of 1 μm as the second interlayer-insulating film 249. There can be used such resin films as polyimide, polyamide, polyimideamide or BCB (benzocyclobutene) or the like in addition to acryl. Here it is desired to maintain a sufficient degree of flatness.

Then, a light-shielding film 250 which is an aluminum film is formed on the second interlayer-insulting film 249 by sputtering. The light-shielding film is formed of a material that satisfies such conditions that (1) an oxide thereof is easily formed on the surface, (2) the oxide has a high dielectric constant and a high breakdown voltage, and (3) it exhibits light-shielding property to a sufficient degree. In this sense, it can be said that the aluminum film or the aluminum alloy film is most suited.

In this embodiment, a high-purity aluminum film (five nine) is used to, first, form the light-shielding film maintaining a thickness of 135 nm. In this case, the light-shielding film 250 is formed so as to conceal the source wiring and gate wiring of the pixel TFT and to conceal the TFT body, and is formed like a matrix on the pixel unit. Here, a contact portion where the drain wiring will be electrically connected to the pixel electrode in a subsequent step is maintained opened without forming the light-shielding film therein.

In this embodiment, further, the surface of the second interlayer-insulating film 249 is plasma-treated by using a CF_4 gas as a pretreatment for forming the light-shielding film 250. Due to this treatment, the adhesion is enhanced between the light-shielding film 250 which is the aluminum film and the second interlayer-insulating film 249 which is the resin film.

Next, the light-shielding film 250 is anodically oxidized to form an anodic oxide 241 on the surface (Fig. 5A).

This embodiment uses a formation solution of a mixture of a 15% ammonium tartarate solution and an ethylene glycol solution at a ratio of 2 to 8. Then, the substrate is immersed in the solution maintained at 10 °C, and a formation current (60 mA/cm^2 in this embodiment) is supplied to effect the anodic oxidation. After the formation voltage has reached 35 V, this voltage is maintained constant for 15 minutes to complete the anodic oxidation.

Thus, the anodic oxide (alumina in this embodiment) is formed maintaining a thickness of about 50 nm on the surface of the light-shielding film 250. Therefore, the light-shielding film 250 finally possesses a thickness of 150 nm.

The second-layer insulating film 249 is etched on the inside of a gap in the light-shielding film in the contact portion between the drain wiring and the pixel electrode, thereby to form a contact hole (contact portion) 252 reaching the drain wiring 246. Then, a pixel electrode 253 which is a transparent electrically conducting film (ITO film in this embodiment) is formed thereon maintaining a thickness of 100 nm (Fig. 5B).

Here, the region 254 where the pixel electrode 253 is overlapped on the light-shielding film 250 works as a storage capacitor. Since the alumina film which is the dielectric has a thickness of as small as about 50 nm and a dielectric constant of as high as 8 to 9, there can be formed a large capacity.

The portion where the contact hole (contact portion) 252 is formed is a gap in the light-shielding film 250 and does not shield light. However, light is completely shielded by the underlying drain wiring 246, and there arouses no problem. It is therefore desired that the contact hole (contact portion) 252 is formed on the inside maintaining a margin of at least 0.5 μm (preferably, 1 μm) from the end of the drain wiring 246.

Thus, the active matrix substrate is completed having a structure as shown in Fig. 5B. Thereafter, the AM-LCD shown in Fig. 1 is fabricated through the known steps of assembling the cells.

The AM-LCD of the invention has several structural features, and exhibits very high operation performance and reliability due to synergistic effects thereof. One of the structural features is that the gate-insulating film has different thicknesses between the drive circuit unit and the pixel unit that formed on the same substrate. Typically, the drive TFTs in part (circuit that must operate at high speeds) of the drive circuit unit has the gate-insulating film of a thickness smaller than that of the pixel TFTs.

Thus, the TFTs having a very high electric-field effect mobility can be arranged in the circuit that must operate at high speeds to satisfy the circuit requirements to a sufficient degree. Then, the TFTs that give importance to the breakdown voltage characteristics rather than the operation speed are arranged in the circuits (pixel unit, buffer circuit, analog switching circuit, etc.) that require a high gate-insulating breakdown voltage.

This does not mean that the thickness of the gate-insulating film must not be the same between the drive circuit unit and the pixel unit. There exists a trade-off relationship between the operation speed and the gate-insulating breakdown voltage, and the above structure is desired in the above-mentioned case.

Another feature is that an ordinary LDD structure is employed for the circuit that gives importance for decreasing the off current like in the pixel unit, and an LDD region overlapped on the gate wiring like the so-called GOLD structure, is arranged in the circuit that gives importance for coping with the hot carriers like in the drive circuit unit. This makes it possible to arrange the TFTs having a sufficient degree of reliability to meet the circuit performance.

A further feature resides in the use of the oxide of the light-shielding film as a dielectric for forming the storage capacity using the light-shielding film and the pixel electrode. A feature also resides in the use of an aluminum film or a film comprising chiefly aluminum as the light-shielding film. This makes it possible to maintain a large capacity with a very small area and, hence, to increase the effective display area of the pixel (to increase the numeral aperture).

According to the manufacturing steps of the embodiment, the final active layer (semiconductor layer) of the TFT is formed of a crystalline silicon film of a particular crystalline structure having continuity in the crystal lattice. Features will now be described.

As a first feature, the crystalline silicon film formed according to the manufacturing steps of the embodiment has a crystalline structure in which a plurality of needle-like or rod-like crystals (hereinafter simply abbreviated as rod-like crystals) are collected and arranged if viewed microscopically. This is easily confirmed by an observation based on the TEM (transparent-type electron microscopic method).

As a second feature, a plane {110} can be confirmed, by utilizing electron ray diffraction, as a main orientation plane in which the crystal axis is deviated to some extent in the surface (channel-forming portion) of the crystalline silicon film formed according to the production steps of the embodiment. This is confirmed from the fact that diffraction spots are appearing having a particular regularity on the plate {110} when the electron ray diffraction photograph having a spot diameter of about 1.35 μm is observed. It is further confirmed that the spots are distributed in a concentric manner.

As a third feature, it is confirmed that the orientation ratio of the plane {220} is not smaller than 0.7 (typically, not smaller than 0.85) if the orientation ratio is calculated by using the X-ray diffraction method (strictly, by using the X-ray diffraction method based on the θ-2θ method). Here, the orientation ratio is calculated according to a method disclosed in Japanese Patent Laid-Open No. 7-321339.

As a fourth feature, the present applicant has confirmed the continuity in the crystalline lattice on the crystalline grain boundary by observing the crystalline grain boundary formed by the rod-like crystals that are contacting to each other based on the HR-TEM (high-resolution transmission-type electron microscopic method). This can be easily confirmed from the fact that the observed crystal lattices are continuing on the crystalline grain boundaries.

The continuity of the crystalline lattice on the crystalline grain boundaries stems from the crystalline grain boundary which is the so-called "planar grain boundary". In this specification, the plane granular boundary is as defined in "Characterization of High-Efficiency Cast-Si Solar Cell Wafers by MBIC Measurement, Ryuichi Shimokawa and

Yutaka Hayashi, Japanese Journal of Applied Physics, Vol. 27, No. 5, pp. 751-758, 1988".

According to the above paper, the planar grain boundary includes twin grain boundaries, special laminate defects and special twisted grain boundaries. The planar grain boundary has a feature in that it is electrically inactive. That is, despite it is a crystalline grain boundary, the planar grain boundary does not exhibit a trapping function for hindering the migration of carriers and can, hence, be regarded to be not substantially existing.

In particular, when the crystal axis (axis perpendicular to the crystal surface) is an $\langle 110 \rangle$ direction, the twin grain boundary $\{211\}$ is also called a corresponding grain boundary of $\Sigma 3$. The value Σ is a parameter indicating the degree of matching of the corresponding grain boundary, and it has been known that the matching increases with a decrease in the value Σ. In the crystalline grain boundary formed between the two crystalline grains, for example, it has been known that when the plane azimuths of the two crystals are $\{110\}$ and when the angle subtended by the lattice stripes corresponding to a plane $\{111\}$ is denoted by θ, then, the corresponding grain boundary of $\Sigma 3$ is obtained when $\theta = 70.5^{\circ}$.

In the crystalline silicon film formed according to the embodiment, when the crystalline grain boundary formed between the two crystalline particles is observed based on the HR-TEM, the lattice stripe of the neighboring crystalline particles is continuing, in many cases, at an angle of about 70.5°. It is, therefore, estimated that the crystalline grain boundary is the corresponding grain boundary of $\Sigma 3$, i.e., the twin grain boundary $\{211\}$.

This crystalline structure (correctly, structure of a crystalline grain boundary) indicates that two different crystalline grains are joined together maintaining very good matching on the crystalline grain boundary. That is, the crystal lattices are continuing on the crystalline boundary very suppressing the trapping level that stems from crystalline defects or the like. Therefore, it can be regarded that the crystalline grain boundary does not substantially exist in the semiconductor thin film having such a crystalline structure.

It has further been confirmed by the TEM observation that most of defects existing in the crystalline particles are extinguished by the heat treatment at a temperature of as high as from 700 to 1150 °C (thermal oxidation step or gettering step in this embodiment). This is obvious from the fact that the number of defects are greatly decreasing before and after the step of heat treatment.

The difference in the number of defects appear as a difference in the spin density through the electron spin resonance analysis (ESR). At present, it has been learned that the crystalline silicon film formed through the manufacturing steps of the embodiment has a spin density of at least not larger than 5×10^{17} spins/cm^3 (preferably not larger than 3×10^{17} spins/cm^3). However, this measured value is close to a limit that can be detected by the existing measuring apparatus and it is expected that the practical spin density may be lower than the above value.

As described above, the crystalline grain boundary does not substantially exist in the crystalline silicon film formed by the embodiment. Therefore, the crystalline silicon film may be considered to be a single crystalline silicon film or a substantially single crystalline silicon film.

(Knowledge concerning Electric Characteristics of the TFT)

The TFT (having the same structure as the CMOS circuit shown in Fig. 1) prepared according to this embodiment exhibits electric properties comparable to those of the MOSFET. The following data are obtained from the TFT (the active layer has a thickness of 35 nm and the gate-insulating film has a thickness of 80 nm) prepared by the present applicant on a trial basis.

The sub-threshold coefficient which is an indication of the switching performance (swiftness of the switching on/off operation) is as small as from 80 to 150 mV/decade(typically, from 100 to 120 mV/decade) for both the N-channel TFT and the P-channel TFT.

The electric-field effect mobility (μ_{FE}) which is an indication of the operation speed of the TFT is as large as from 150 to 650 cm^2/Vs (typically, from 200 to 500 cm^2/Vs) for the N-channel TFT, and from 100 to 300 cm^2/Vs (typically, from 120 to 200 cm^2/Vs) for the P-channel TFT.

The threshold voltage (V_{th}) which is an indication of the drive voltage of the TFT is as small as from -0.5 to 1.5 V for the N-channel TFT and from -1.5 to 0.5 V for the P-channel TFT. As described above, it has been confirmed that very excellent switching characteristics and high-speed operation characteristics are realized.

[Embodiment 2]

In the embodiment 1, the light-shielding film 250 may be maintained at a common potential or may be floated. There will be no problem when it is floated. When pulled down to the common potential, however, a connection terminal is necessary for pulling the light-shielding film down to the common potential. This embodiment deals with this structure with reference to Figs. 7A and 7B.

In Fig. 7A, reference numeral 701 is a common source feeder line which is a wiring formed simultaneously with the source wiring and the drain wiring. Further, reference numeral 702 denotes a second interlayer-insulating film, 703 denotes a light-shielding film, and 704 denotes an anodic oxide.

In this case, prior to forming the light-shielding film 250 through the step of Fig.

5A, a contact hole (contact portion) 705 (Fig. 7A) may be formed in the second interlayer-insulating film 249 (corresponds to 702 in Fig. 7A) and, then, the light-shielding film 250 (corresponds to 703 in Fig. 7A) may be formed. Thus, the light-shielding film 703 can be easily maintained at the common potential.

Fig. 7B illustrates this state that is viewed from the upper surface. Fig. 7A is a sectional of the upper plan view of Fig. 7A along the line A-A'. Reference numerals should be referred to those shown in Fig. 7A. This embodiment is one of the examples of the embodiment 1, and the conditions of the manufacturing steps should be referred to those of the embodiment 1.

[Embodiment 3]

This embodiment is another example of the embodiment 2. The structure of this embodiment is shown in Figs. 8A and 8B. In Fig. 8A, reference numeral 801 denotes a common power feeder line which is a wiring formed simultaneously with the source wiring and the drain wiring. Reference numeral 802 denotes a second interlayer-insulating film, 803 denotes a light-shielding film, 804 denotes an anodic oxide and 805 denotes a transparent electrically conducting film formed simultaneously with the pixel electrode.

Here, in forming the contact hole (contact portion) 252 in the second interlayer-insulating film 249 through the step of Fig. 5B, the second interlayer-insulating film 802 is partly removed at the connection terminal portion to expose the common power feeder line 801 as shown in Fig. 8A. Then, a transparent electrically conducting film 805 is formed on the connection terminal portion simultaneously with the formation of the pixel electrode 253.

In this case, the anodic oxide 804 exists between the light-shielding film 803 and the transparent electrically conducting film 805 to form a capacitor 806. When the AC drive is taken into consideration, however, it can be regarded that the capacitor 806 is substantially short-circuited, and the light-shielding film 803 and the common power feeder line 801 are electrically connected together.

Fig. 8B illustrates this state as viewed from the upper surface. Fig. 8A is a sectional view of the upper plan view of Fig. 8B along the line A-A'. Reference numerals should be referred to those of Fig. 8A. This embodiment is one of the examples of the embodiment 1, and the conditions of the manufacturing steps should be referred to those of the embodiment 1.

[Embodiment 4]

In Fig. 1, a capacitive coupling takes place between the light-shielding film 130 and an opposing electrode 136 on the side of the opposing substrate, with the liquid crystal 134 as a dielectric (strictly speaking, the alignment films 133 and 135 and oxide 131 are also included). When the capacitive coupling is large, therefore, the light-shielding film 130 is maintained at the common potential due to the effect of coupling.

That is, the light-shielding film 130 can be maintained at the common potential due to the capacitive coupling to the opposing electrode without connecting any other wiring. In this embodiment, the light-shielding film 130 is thus maintained at the common potential. This embodiment is one of the examples of the embodiment 1, and the conditions of the manufacturing steps should be referred to those of the embodiment 1.

[Embodiment 5]

This embodiment concretely explains the TFTs of what structure be arranged in what circuit with reference to Figs. 9A to 9D.

The AM-LCD has a minimum required operation voltage (power-source voltage) that differs depending on the circuit. In the pixel unit, for example, the operation voltage ranges from 14 to 20 V by taking into consideration the voltage applied to the liquid crystals in the pixel unit and the voltage for driving the pixel TFTS. Therefore, the TFTs must be capable of withstanding the application of such high voltages.

The shift resister circuit used for the source drive circuit and the gate drive circuit needs have an operation voltage of from about 5 to about 10 V at the highest. The lower voltage offers compatibility to the external signals and suppresses the consumption of electric power. However, the high break-down voltage-type TFT operates at a low speed though it exhibits favorable breakdown voltage characteristics, and is not suited for a circuit that must operate at high speeds, such as a shift register circuit.

Thus, the circuits formed on the substrate are divided into those circuits that use the TFTs giving importance to the breakdown voltage characteristics and those circuits that use the TFTs giving importance to the operation speed.

Figs. 9A to 9D concretely illustrates the constitution of this embodiment. Fig. 9A is a block diagram of the AM-LCD of when it is viewed from the upper side. Reference numeral 901 denotes a pixel unit. Each pixel includes a pixel TFT and a storage capacity, and functions as a display unit. Reference numeral 902a denotes a shift register circuit, 902b denotes a level shifter circuit, and 902c denotes a buffer circuit. These circuits as a whole forms a gate-drive circuit unit.

In the AM-LCD shown in Fig. 9A, the gate-drive circuit units are provided with the pixel unit being sandwiched therebetween, and have the same gate wiring, respectively. That is, redundancy is provided such that even in case defect occurs in either one gate driver, a voltage is applied to the gate wiring.

Reference numeral 903a denotes a shift register circuit, 903b denotes a level shifter circuit, 903c denotes a buffer circuit, and 903d denotes a sampling circuit. These circuits as a whole form a source-drive circuit. A precharging circuit 904 is provided on the side opposite to the source-drive circuit with the pixel unit sandwiched therebetween.

In the thus constituted AM-LCD, the shift register circuits 902a and 903a are the circuits that must operate at high speeds, operate at a voltage of as low as from 3.3 to 10 V (typically, from 3.3 to 5 V), and do not require particularly high breakdown voltage characteristics. It is therefore desired that the gate-insulating film has a thickness of as small as from 5 to 50 nm (preferably, from 10 to 30 nm).

Fig. 9B is a schematic view of the CMOS circuit chiefly used for the circuit that must operate at high speeds, like the shift register and the signal-dividing circuit. In Fig. 9B, reference numeral 905 denotes a gate-insulating film having a thickness of as small as from 5 to 50 nm (preferably, from 10 to 30 nm).

It is further desired that the LDD region 906 has a length of from 0.1 to 1 μm (typically, from 0.3 to 0.5 μm). When the operation voltage is as sufficiently low as from 2 to 3 V, the LDD region may not be provided. The LDD region is completely overlapped on the gate wiring to prevent deterioration caused by hot carriers, as a matter of course.

Next, the CMOS circuit shown in Fig. 9C is chiefly adapted to level shifter circuits 902b and 903b, buffer circuits 902c, 903c, sampling circuit 903d and precharging circuit 904. These circuits must flow heavy currents and operate at voltages as high as from 14 to 16 V. On the gate driver side, in particular, an operation voltage of as high as 19 V may often be required. Therefore, the TFTs having very good breakdown voltage characteristics (high breakdown voltage characteristics) must be used.

In the CMOS circuit shown in Fig. 9C, the thickness of the gate-insulating film 907 is selected to be from 50 to 200 nm (desirably, from 100 to 150 nm). In the circuit that requires a high gate-insulating breakdown voltage, it is desired that the gate-insulating film has a thickness larger than that of the TFTs in the shift register circuit.

It is desired that the LDD region 908 has a length of from 1 to 3 μm (typically, from 1.5 to 2 μm). A portion of the LDD region overlapped on the gate wiring may have a length of from 0.5 to 2 μm (preferably, from 1 to 1.5 μm). The remainder of the LDD region is not overlapped on the gate wiring. Arrangement of such a region makes it possible to effectively suppress the off current. The CMOS circuit shown in Fig. 9C receives a high voltage comparable to that applied to the pixel like the buffer circuit. It is therefore desired that the LDD region has a length comparable to, or close to, that of the pixel.

Fig. 9D is a view schematically illustrating the pixel unit 901. The pixel TFT requires an operation voltage of from 14 to 16 V since it is added up with a voltage applied to the liquid crystal. Further, the electric charge stored in the liquid crystal and in the storage capacity must be maintained for a period of one frame and, hence, the off current must be as small as possible.

On account of these reasons in this embodiment, the double-gate structure is employed by using the NTFTs, and the thickness of the gate-insulating film 909 is selected to be from 50 to 200 nm (preferably, from 100 to 150 nm). This film thickness may be the same as, or different from, the thickness of the film in the CMOS circuit shown in Fig. 9C.

It is further desired that the LDD regions 910a and 910b have a length of from 2 to 4 μm (typically, from 2.5 to 3.5 μm). The pixel TFT shown in Fig. 9D has a feature in that the LDD regions 910a and 910b are not overlapped on the gate wiring, since the off current must be decreased as much as possible.

Even with reference to the AM-LCD as described above, a variety of circuits are often provided on the same substrate, and different operation voltages (power-source voltages) are required by the circuits. In such a case, the TFTs having gate-insulating films of different thicknesses must be arranged depending on the circuits as in this invention.

The circuit shown in the embodiment 1 is effective in realizing the constitution of this embodiment.

[Embodiment 6]

In conducting the step for selectively removing the gate-insulating film in the embodiment 1, it is desired that the removal from the region where the drive TFT is to be formed is conducted in a manner as shown in Fig. 10. In Fig. 10, reference numeral 11 denotes an active layer, 12 denotes an end of the gate-insulating film, and 13 and 14 denote gate wirings. As shown in Fig. 10, it is desired to leave the gate-insulating film at an end of the active layer 11 on a portion 15 where the gate wiring rides over the active layer 11.

A phenomenon called edge thinning occurs at the end of the active layer 11 in a subsequent step of thermal oxidation. This is the phenomenon in which the oxidation reaction so proceeds as to dive under the end of the active layer, causing the end to become thin and swell upward. Therefore, the edge-thinning phenomenon arouses a problem in that the gate wiring breaks down when it rides over.

When the gate-insulating film is removed so as to establish the structure as shown in Fig. 10, however, the edge-thinning phenomenon is prevented from occurring at a portion 15 where the gate wiring rides over. This makes it possible to prevent in advance the problem of breakage of the gate wiring. The constitution of this embodiment can be effectively used for the embodiment 1.

[Embodiment 7]

This embodiment deals with the case where the AM-LCD is really manufactured by forming the TFTs on the substrate through the manufacturing steps shown in the embodiment 1.

After the state of Fig. 5B is obtained, the alignment film is formed maintaining a thickness of 80 nm on the pixel electrode 253. Next, the opposing substrate is prepared by forming a color filter, a transparent electrode (opposing electrode) and alignment films on a glass substrate. Then, the alignment films are rubbed, and the substrate on which the TFTs are formed is stuck to the opposing substrate using a sealing member. Liquid crystals are held therebetween. The cells can be fabricated by using known means which is not described here in detail.

The spacer may be provided as required for maintaining a cell gap. Therefore, the spacer may not be particularly provided when the cell gap can be maintained like in the AM-LCD of a diagonal of not larger than an inch.

Fig. 11 shows the appearance of the thus manufactured AM-LCD. On the active matrix substrate (the one in which the TFTs are formed) 21 are formed the pixel unit 22, source drive circuit 23, gate drive circuit 24, and signal processing circuit (signal-dividing circuit, D/A converter circuit, γ-correction circuit, differential amplifier circuit, etc.) 25, and to which is attached an FPC (flexible printed circuit) 26. Reference numeral 27 denotes an opposing substrate.

This embodiment can be combined with any one of the embodiments 1 to 6.

[Embodiment 8]

This embodiment deals with the case where another means is employed for forming the crystalline silicon film in the embodiment 1.

Concretely speaking, technique disclosed in the embodiment 2 of Japanese Patent Laid-Open No. 7-130652 (corresponds to U.S. Patent No. 5,643,826) is employed for crystallizing the amorphous silicon film. The technique disclosed in this application is the one according to which a catalytic element (typically, nickel) for promoting the crystallization is selectively held on the surface of the amorphous silicon film, and this portion is crystallized as a seed for growing the nuclei.

According to this technique, particular directivity can be imparted to the growth of crystals making it possible to form a highly crystalline silicon film.

It is also possible to form an insulating masking film for selectively holding the catalytic element, for masking phosphorus that is added for gettering. This makes it possible to decrease the number of the steps. This technique has been closely disclosed in Japanese Patent Laid-Open No. 10-247735 filed by the present applicant.

The constitution of this embodiment can be freely combined with the constitution of any one of the embodiments 1 to 7.

[Embodiment 9]

Phosphorus is used for gettering nickel (catalytic element used for crystallizing the silicon film) described in the embodiment 1. This embodiment deals with the case where nickel is gettered by using another element.

First, the state of Fig. 2B is obtained according to the step of the embodiment 1. In Fig. 2B, reference numeral 204 denotes a crystalline silicon film. In this embodiment, however, the concentration of nickel used for the crystallization is suppressed to be as low as possible. Concretely speaking, a layer containing nickel in an amount of from 0.5 to 3 ppm reckoned as weight is formed on the amorphous silicon film, and the heat treatment is effected for crystallization. The nickel concentration in the thus formed crystalline silicon film is from 1 x 10^{17} to 1 x 10^{19} atoms/cm^3 (typically, from 5 x 10^{17} to 1 x 10^{18} atoms/cm^3).

After the crystalline silicon film is formed, the heat-treatment is conducted in an oxidizing atmosphere containing halogen element. The temperature is from 800 to 1150 °C (preferably, from 900 to 1000 °C) and the treating time is from 10 minutes to 4 hours (preferably, from 30 minutes to one hour).

In this embodiment, the heat treatment is conducted at 950 °C for 30 minutes in an atmosphere, i.e., in an oxygen atmosphere containing 3 to 10% by volume of hydrogen chloride.

Through this step, nickel is released from the crystalline silicon film as volatile nickel chloride into the treating atmosphere. That is, nickel is removed by the gettering action of a halogen element. When the nickel concentration existing in the crystalline silicon film is too high, however, there arouses a problem in that the oxidation abnormally proceeds on a portion where nickel has segregated. Therefore, the concentration of nickel must be suppressed to be as low as possible in the step of crystallization.

The constitution of this embodiment can be freely combined with any one of the constitutions of the embodiments 1 to 8.

[Embodiment 10]

This embodiment deals with the case where the CMOS circuit and the pixel unit shown in the embodiment 1 have different structures. Concretely speaking, the arrangement of the LDD region is differed depending upon the specifications required by the circuits.

The basic structures of the CMOS circuit and the pixel unit were shown already in Fig. 1. Therefore, this embodiment describes required portions only by attaching reference numerals thereto. As for the TFT structure of this embodiment, further, reference should basically be made to the manufacturing method of the embodiment 1.

First, the circuit shown in Fig. 12A has a feature in that the LDD region 31 of NTFT is provided being contacted to the channel-forming region 32 of the side of the drain region 33 only in the CMOS circuit. This structure is realized by concealing the side of the source region with the resist mask.

The CMOS circuit used for the drive circuit unit must operate at a high speed and, hence, the resistance component that could decrease the operation speed must be excluded as much as possible. However, the LDD region necessary for enhancing resistance against the hot carriers works as a resistance component, sacrificing the operation speed.

However, the hot carriers are poured at an end of the channel-forming region on the side of the drain region, and the countermeasure against the hot carriers is sufficient if there exists the LDD region at that portion being overlapped on the gate wiring. Therefore, the LDD region needs not be provided to an excess degree at an end of the channel-forming region on the side of the source region.

The structure of Fig. 12A cannot be adapted for the case where the source region and the drain region are interchanged like the pixel TFT. In the case of the CMOS circuit, the source region and the drain region are usually secured, and the structure of Fig. 12A can be realized.

Next, the circuit shown in Fig. 12B shows the case where the NTFT has the double-gate structure and the PTFT has the single-gate structure in the CMOS circuit. This structure is used for the drive circuit unit (typically, buffer circuit or sampling circuit) that requires a high breakdown voltage).

In this case, a feature resides in that the LDD regions 34a and 34b of NTFT are provided by the sides of the channel-forming regions 35a and 35b on the side of the drain regions 36 (or on the side close to the drain regions 36).

Upon employing this structure, no resistance component is contained in the LDD regions on the side of the source regions. Further, the double-gate structure disperses and relaxes the electric field across the source and the drain.

The constitution of this embodiment can be freely combined with any one of the constitutions of the embodiments 1 to 9.

[Embodiment 11]

In the embodiment 1, providing the light-shielding film under the TFT (concretely speaking, under the active layer), as required, is effective in suppressing the leakage of current caused by optical excitation. In particular, the light-shielding film is effective when it is provided under the pixel TFT for which the leakage of current (or off current) must be suppressed as much as possible.

As the light-shielding film, there can be used a metal film or a black resin film. When the metal film is used, a storage capacity can be formed between the light-shielding film and the active layer. In this case, a net of two storage capacitors are connected in parallel, making it possible to obtain a sufficient amount of storage capacity.

The constitution of this embodiment can be freely combined with any one of the constitutions of the embodiments 1 to 10.

[Embodiment 12]

This embodiment offers technique for enhancing the adhesion between the light-shielding film and the underlying second interlayer-insulating film (resin film) in the pixel unit shown in the embodiment 1.

In this embodiment, after the second interlayer-insulating film 41 of acrylic film is formed, a silicon oxide film is formed maintaining a thickness of from 10 to 30 nm by sputtering and, then, an aluminum film of a high purity is continuously formed. This film is etched at one time to form the light-shielding film. In Fig. 13, reference numeral 42 is a silicon oxide film, and 43 is an aluminum film of a high purity.

The silicon oxide film 42 works as a buffer layer for improving adhesion between the second interlayer-insulating film 41 which is the acrylic film and the light-shielding film 43 which is the aluminum film of a high purity. Upon providing the silicon oxide film 42, a favorable adhesion is maintained even when the oxide 44 is formed by the anodic oxidation method.

The constitution of this embodiment can be freely combined with any one of the constitutions of the embodiments 1 to 11.

[Embodiment 13]

This embodiment deals with the case where the storage capacitor has a structure different from that of Fig. 1. Reference is made to Figs. 14A and 14B.

In Fig. 14A, first, the state of Fig. 5A is obtained according to the steps of the embodiment 1. Next, the third interlayer-insulating film 51 is formed by using the resin film (acrylic film in this embodiment), and openings 52a and 52b are formed therein. Upon forming the openings 52a and 52b, the light-shielding film 250 (strictly, an oxide 251 on the surface thereof) is exposed. Here, the contact hole 53 is also formed simultaneously.

Thereafter, the pixel electrode 54 which is an ITO film is formed. Thus, storage capacitors are formed by the light-shielding film 250, oxide 251 of the light-shielding film and the pixel electrode 54 in the openings 52a and 52b. Upon employing this structure, the pixel electrode 54 does not have to ride over the end of the light-shielding film 250, and the problem such as short-circuiting is prevented from occurring at the end.

In Fig. 14B, the steps up to that of Fig. 5A (but prior to forming the oxide 251) are executed according to the steps of the embodiment 1. That is, the steps are conducted up to forming the light-shielding film 250 of the aluminum film on the second interlayer-insulating film 249.

Next, the third interlayer-insulating film 55 of an acrylic film is formed, and openings 56a and 56b are formed therein. Here, the contact hole 57 is also formed simultaneously.

Then, in this state, an oxide 58 is formed on the exposed surface of the light-shielding film 250. In this embodiment, the oxide 58 is formed by the anodic oxidation method. However, there may be employed the thermal oxidation method or the plasma oxidation method.

Thus, after the oxide 58 is formed on part of the surface (upper surface) of the light-shielding film 250, then, the pixel electrode 59 of an ITO film is formed. Thus, the storage capacitors are formed by the light-shielding film 250, oxide 58 of the light-shielding film and pixel electrode 59 in the openings 56a and 56b. In this constitution, too, the pixel electrode is prevented from being short-circuited at the end of the light-shielding film like in Fig. 14A.

The constitution of this embodiment can be freely combined with any one of the constitutions of the embodiments 1 to 12.

[Embodiment 14]

This embodiment deals with the structure of the pixel unit formed by the invention with reference to Figs. 15A to 15B. The basic sectional structures were described already with reference to Figs. 1 to 5B. Here, therefore, the description proceeds paying attention to a positional relationship (position for forming the storage capacity) between the light-shielding film and the pixel electrode.

First, the step of Fig. 15A is the one where the steps have been finished up to the step shown in Fig. 4D, wherein reference numeral 61 denotes an active layer, 62 denotes a gate wiring, 63 denotes a source wiring, 64 denotes a contact portion between the active layer and the source wiring, 65 denotes a drain wiring (drain electrode), and 66 denotes a contact portion between the active layer and the drain wiring.

Next, the step of Fig. 15B is the one where the steps have been finished up to the step shown in Fig. 5B. This state is the one where the light-shielding film 67 and the pixel electrode 68 are overlapped one upon the other. The pixel electrode 68 is partly represented by a dotted line in order to clarify the positional relationship of the underlying layer relative to the light-shielding film.

Referring to Fig. 15B, the pixel electrode 68 is so formed as to be overlapped on the light-shielding film 67 along the outer peripheral portion of the picture display region 69. The region 70 where the pixel electrode 68 and the light-shielding film 67 are overlapped one upon the other, works as a storage capacity.

Reference numeral 71 denotes a contact portion between the drain wiring 65 and the pixel electrode 68. The contact portion 71 cannot be provided with the light-shielding film 67. However, light is completely shielded by the drain wiring layer 65, and the TFT is never exposed to light.

The structure of this embodiment has an advantage in that there is no need of separately forming a wiring for forming the capacitor, and the numerical aperture of the pixels can be enhanced. The storage capacity 70 is formed on the source wiring 63 or on the gate wiring 62, and does not substantially decrease the numerical aperture.

Accordingly, the picture display region 69 is maximized, and a bright picture is obtained.

The constitution of this embodiment can be freely combined with any one of the constitutions of the embodiments 1 to 13.

[Embodiment 15]

This embodiment deals with a case where the crystalline silicon film is formed by means different from that of the embodiment 1.

In the embodiment 1, a catalytic element (nickel) was used for crystallizing the amorphous semiconductor film (concretely, amorphous silicon film). This embodiment, however, deals with the case where the amorphous semiconductor film is thermally crystallized without using the catalytic element.

In the case of this embodiment, the amorphous silicon film that is formed is crystallized through the heat treatment at a temperature of from 580 to 640 °C (typically, 600 °C) for 12 to 30 hours (typically, from 16 to 24 hours) to obtain a crystalline silicon film. Therefore, the gettering step shown in the embodiment 1 can be omitted.

With the structure of the invention being realized as described above, the invention can be easily combined with a process which uses the crystalline silicon film which is the so-called high-temperature polysilicon.

The constitution of this embodiment can be freely combined with any one of the embodiments 1 to 7 and 9 to 14.

[Embodiment 16]

This embodiment deals with an example of forming the first interlayer-insulating film by a method different from that of the embodiment 1. The description refers to Figs. 16A and 16B.

First, the steps are effected up to the activation step shown in Fig. 4C according to the manufacturing steps of the embodiment 1. In this embodiment, a silicon oxynitride film (described here as silicon oxynitride film (A) 1601) is used as the silicon oxynitride film 240. After the activation step has been finished, a silicon oxynitride film (B) 1602 is formed thereon maintaining a thickness of from 600 nm to 1 μm (800 nm in this embodiment). Then, a resist mask 1603 is formed thereon (Fig. 16A).

The silicon oxynitride film (A) 1601 and the silicon oxynitride film (B) 1602 have different composition ratios of nitrogen, oxygen, hydrogen and silicon. The silicon oxynitride film (A) 1601 contains 7% of nitrogen, 59% of oxygen, 2% of hydrogen and 32% of silicon, and the silicon oxynitride film (B) 1602 contains 33% of nitrogen, 15% of oxygen, 23% of hydrogen and 29% of silicon. The composition ratios are not limited thereto only, as a matter of course.

Further, the resist mask 1603 has a large thickness and is capable of completely flattening the undulations on the surface of the silicon oxynitride film (B) 1602.

Next, the resist mask 1603 and the silicon oxynitride film (B) 1602 are etched by the dry etching method using a mixture gas of carbon tetrafluoride and oxygen. In the case of this embodiment, the silicon oxynitride film (B) 1602 and the resist mask 1603 are etched at nearly an equal rate by the dry etching using the mixture gas of carbon tetrafluoride and oxygen.

Through the step of etching, the resist mask 1603 is completely removed as shown in Fig. 16B, and the silicon oxynitride film (B) is partly etched (from the surface to a depth of 300 nm in this embodiment). As a result, the flatness of the surface of the resist mask 1603 is directly reflected onto the flatness on the surface of the silicon oxynitride film (B) that is etched.

Thus, there is obtained a first interlayer-insulating film 1604 having a very high degree of flatness. In the case of this embodiment, the first interlayer-insulating film 1604 has a thickness of 500 nm. As for the subsequent steps, reference should be made to the manufacturing steps of the embodiment 1.

The constitution of this embodiment can be freely combined with any one of the embodiments 1 to 15.

[Embodiment 17]

A variety of known liquid crystal materials can be used for the AM-LCD manufactured according to the invention. Examples of the materials include TN liquid crystal, PDLC (polymer-dispersed liquid crystal), FLC (ferroelectric liquid crystal), AFLC (antiferroelectric liquid crystal) and a mixture of FLC and AFLC.

For example, there can be used materials disclosed in "H. Furue et al.; Characteristics and Driving Scheme of Polymer-Stabilized Monostable FLCD Exhibiting Fast Response Time and High Contrast Ratio with Gray-Scale Capability, SID, 1998", "T. Yoshida et al.; A full-Color Thresholdless Antiferroelectric LCD Exhibiting Wide Viewing Angle with Fast Response time, 841, SID 97 DIGEST, 1997" and U.S. Patent No. 5,594,569.

By using the thresholdless antiferroelectric liquid crystal, in particular, the power-source voltage needs be about 5 to 8 volts since the liquid crystal operates on a voltage of about ±2.5 V. That is, it is allowed to operate the drive circuit unit and the pixel unit on the same power-source voltage and, hence, to decrease the amount of electric power consumed by the whole AM-LCD.

Further, the ferroelectric liquid crystal and the antiferroelectric liquid crystal have advantage in that they exhibit a response speed faster than that of the TN liquid crystal. This advantage could not be obtained with the conventional TFTs. When there is used the TFTs having the crystalline structure as explained in the embodiment 1, however, there are realized the TFTs that operate at a very high speed, making it possible to realize the AM-LCD that exhibits a high picture response speed by utilizing the high response speed of the ferroelectric liquid crystal or of the antiferroelectric liquid crystal to a sufficient degree.

It needs not be pointed out that the AM-LCD of this embodiment can be used as a display unit for an electric appliance such as a personal computer or the like.

The constitution of this embodiment can be freely combined with any one of the constitutions of the embodiments 1 to 16.

[Embodiment 18]

This invention permits the formation of an interlayer-insulating film on the conventional MISFET and the formation of a TFT further thereon. In other words, the invention makes it possible to realize a semiconductor device of the three-dimensional structure in which the reflection-type AM-LCD is formed on the semiconductor circuit.

Further, the semiconductor circuit may be formed on an SOI substrate such as SIMOX, Smart-Cut (registered trademark of SOITEC Co.) or ELTRAN (registered trademark of Canon Co.).

This embodiment can be put into practice by being combined with any one of the constitutions of the embodiments 1 to 17.

[Embodiment 19]

This invention can also be adapted to the active matrix-type EL (electroluminescence) display (often referred to as EL display device). An example is shown in Fig. 17.

Fig. 17 is a circuit diagram of the active matrix-type EL display, wherein reference numeral 81 denotes a display region which is surrounded by an X-direction (source side) drive circuit 82 and a Y-direction (gate side) drive circuit 83. Each pixel in the display region 81 includes a switching TFT 84, a capacitor 85, a current-control TFT 86 and an EL element 87. To the switching TFT 84 are connected an X-direction signal line (source signal line) 88a or 88b, and a Y-direction signal line (gate signal line) 89a, 89b or 89c. To the current-control TFT 86 are connected power-source lines 90a and 90b.

In the active matrix-type EL display of this embodiment, the gate-insulating film of the TFTs used in the X-direction drive circuit 82 and the Y-direction drive circuit 83 has a thickness smaller than the gate-insulating film of the switching TFTs 84 or the current-control TFTs 86. Further, the capacitor 85 is formed by the storage capacitor of the present invention.

The active matrix-type EL display of this invention can be combined with any one of the constitutions of the embodiments 1 to 16 and 18.

[Embodiment 20]

This embodiment deals with an EL (electroluminescence) display device manufactured according to the present invention. Here, Fig. 18A is a top view of the EL display device of this invention, and Fig. 18B is a sectional view thereof.

In Fig. 18A, reference numeral 4001 denotes a substrate, 4002 denotes a pixel unit, 4003 denotes a source-side drive circuit, and 4004 denotes a gate-side drive circuit. These drive circuits are connected to an FPC (flexible printed circuit) 4006 through wirings 4005, and are connected to an external unit.

Here, a first sealing member 4101, a cover member 4102, a filler member 4103 and a second sealing member 4104 are so provided as to surround the pixel unit 4002, source-side drive circuit 4003 and gate-side drive circuit 4004.

Fig. 18B is a sectional view along the line A-A' of Fig. 18A, and wherein the substrate 4001 has, formed thereon, drive TFTs (n-channel TFTs and p-channel TFTs are shown here) 4201 included in the source-side drive circuit 4003 and current-control TFTs (TFTs for controlling current to the EL elements) 4202 included in the pixel unit 4202.

In this embodiment, the drive TFT 4201 has the same structure as that of the drive circuit unit of Fig. 1, and the current-control TFT 4202 has the same structure as that of the pixel unit of Fig. 1. The pixel unit 4002 is provided with a storage capacitor (corresponding to the capacitor 85 of Fig. 17) connected to the gate of the current-control TFT 4202. This storage capacitor (not shown) has the same structure as that of the storage capacitor 254 shown in Fig. 5B.

An interlayer-insulating film (flat film) 4301 of a resin material is formed on the drive TFT 4201 and on the pixel TFT 4202, and a pixel electrode (anode) 4302 is formed thereon so as to be electrically connected to the drain of the pixel TFT 4202. A transparent electrically conducting film having a large work function is used as the pixel electrode 4302. The transparent electrically conducting film can be formed of a compound of indium oxide and tin oxide or a compound of indium oxide and zinc oxide.

An insulating film 4303 is formed on the pixel electrode 4302. An opening is formed in the insulating film 4303 on the pixel electrode 4302. An EL (electroluminescence) layer 4304 is formed in the opening on the pixel electrode 4302. A known organic EL material or inorganic EL material can be used as the EL layer 4304. The organic EL material may be either of the low-molecular type (monomer type) or of the high-molecular type (polymer type).

The EL layer 4304 may be formed relying on a known technique. The EL layer may have a laminated-layer structure in which a positive hole-injection layer, a positive hole transport layer, a light-emitting layer and an electron transport layer or an electron injection layer are freely combined together, or may have a single-layer structure.

A cathode 4305 of a light-shielding electrically conducting film (typically, an electrically conducting film chiefly comprising aluminum, copper or silver, or a laminated-layer film thereof with other electrically conducting film) is formed on the EL layer 4304. It is desired that moisture or oxygen is removed as much as possible from the interface between the cathode 4305 and the EL layer 4304. Therefore, the two layers are continuously formed in vacuum, or the EL layer 4304 is formed in a nitrogen atmosphere or in a rare gas atmosphere, and the cathode 4305 is formed being kept away from oxygen or moisture. In this embodiment, the above film is formed by using a film-forming apparatus of a multi-chamber type (cluster tool type).

The cathode 4305 is electrically connected to the wiring 4005 on a region denoted by 4306. The wiring 4005 is for applying a predetermined voltage to the cathode 4305, and is electrically connected to the FPC 4006 through an electrically conducting material 4307.

Thus, an EL element is formed comprising the pixel electrode (anode) 4302, EL layer 4304 and cathode 4305. The EL element is surrounded by the first sealing member 4101 and by the covering member 4102 stuck to the substrate 4001 with the first sealing member 4101, and is filled with a filler 4103.

As the covering member 4102, there can be used a glass plate, a metal plate (typically, a stainless steel plate), a ceramics plate, an FRP (fiber glass-reinforced plastics) plate, a PVF (polyvinyl fluoride) film, a mylar film, a polyester film or an acrylic film. There can be further used a sheet of a structure in which an aluminum foil is sandwiched by the PVF films or the mylar films.

When light is radiated from the EL element toward the covering member, however, the covering member must be transparent. In such a case, there is used a transparent material such as glass plate, plastic plate, polyester film or acrylic film.

As the filler 4103, there can be used an ultraviolet-ray curing resin or a thermosetting resin, such as PVC (polyvinyl chloride), acrylic, polyimide, epoxy resin, silicone resin, PVB (polyvinyl butyral) or EVA (ethylenevinyl acetate). A hygroscopic material (preferably, barium oxide) is provided in the filler 4103 to suppress the deterioration of the EL element.

A spacer may be contained in the filler 4103. Here, hygroscopic property can be imparted to the spacer itself when it is formed of barium oxide. When the spacer is provided, further, a resin film formed on the anode 4305 effectively works as a buffer layer for relaxing pressure from the spacer.

The wiring 4005 is electrically connected to the FPC 4006 through the electrically conducting material 4305. The wiring 4005 transmits to the FPC 4006 a signal that is sent to the pixel unit 4002, source-side drive circuit 4003 and gate-side drive circuit 4004, and is electrically connected to an external unit through the FPC 4006.

In this embodiment, further, the second sealing member 4104 is so provided as to cover an exposed portion of the first sealing member 4101 and a portion of the FPC 4006, in order to thoroughly shut off the EL element from the open atmosphere. Thus, the EL display device is obtained having a sectional structure as shown in Fig. 18B. The EL display device of this embodiment may be manufactured in combination with any one of the constitutions of the embodiments 1 to 16 and 18.

[Embodiment 21]

Figs. 19A to 19C illustrate the structure of a pixel that can be used in the pixel unit of the EL display device of the embodiment 20. In this embodiment, reference numeral 4401 denotes a source wiring of a switching TFT 4402, reference numeral 4403 denotes a gate wiring of the switching TFT 4402, reference numeral 4404 denotes a current-control TFT, 4405 denotes a capacitor, 4406 and 4408 denote current feeder lines, and reference numeral 4407 denotes an EL element.

Fig. 19A illustrates an example in which the current feeder line 4406 is used in common for the two pixels. That is, the feature resides in that the two pixels are formed symmetrically with the current feeder line 4406 as a center. In this case, the number of the power feeder lines can be decreased, enabling the pixel unit to be more finely fabricated.

Fig. 19B illustrates a case where the current feeder line 4408 is formed in parallel with the gate wiring 4403. In Fig. 19B, the current feeder line 4408 is not overlapped on the gate wiring 4403. However, they may be formed so as to be overlapped on upon the other via an insulating film provided they are formed in different layers. In this case, the power feeder line 4408 and the gate wiring 4403 are allowed to share their areas, making it possible to more finely fabricate the pixel unit.

Further, Fig. 19C has a feature in that the current feeder line 4408 is formed in parallel with the gate wiring 4403a and 4403b like in the structure of Fig. 19B, and the two pixels are symmetrically formed with the current feeder line 4408 as a center. It is further effective if the current feeder line 4408 is so formed as to be overlapped on either one of the gate wirings 4403a and 4403b. In this case, the number of the power feeder lines can be decreased, making it possible to further finely fabricate the pixel unit.

[Embodiment 22]

The electro-optical device and semiconductor circuit of this invention can be used as a display unit or a signal processing circuit of electric appliances. Examples of the electric appliances include a video camera, a digital camera, a projector, a projection TV, a goggle-type display (head-mount display), a navigation system, an acoustic reproduction apparatus, a notebook personal computer, a game device, a portable data terminal (mobile computer, portable telephone, portable game machine, digital book, etc.), and picture reproducing apparatus equipped with a recording medium. Concrete examples of the electric appliances are shown in Figs. 20A to 22B.

Fig. 20A shows a portable telephone constituted by a main body 2001, a voice output unit 2002, a voice input unit 2003, a display unit 2004, operation switches 2005 and an antenna 2006. The electro-optical device of the invention can be used as the display unit 2004, and the semiconductor circuit of the invention can be used as the voice output unit 2002, voice input unit 2003, or as CPU or memory.

Fig. 20B illustrates a video camera constituted by a main body 2101, a display unit 2102, a voice input unit 2103, operation switches 2104, a battery 2105 and an image-receiving unit 2106. The electro-optical device of the invention can be used as the display unit 2102, and the semiconductor circuit of the invention can be used as the voice input unit 2103, CPU or memory.

Fig. 20C illustrates a mobile computer which is constituted by a main body 2201, a camera unit 2202, an image-receiving unit 2203, operation switches 2204 and a display unit 2205. The electro-optical device of the invention can be used as the display unit 2205, and the semiconductor circuit of the invention can be used as CPU or memory.

Fig. 20D shows a goggle-type display constituted by a main body 2301, a display unit 2302 and an arm unit 2303. The electro-optical device of the invention can be used as the display unit 2302, and the semiconductor circuit of the invention can be used as CPU or memory.

Fig. 20E shows a rear projector (projection TV) constituted by a main body 2401, a light source 2402, a liquid crystal display device 2403, a polarized beam splitter 2404, reflectors 2405, 2406, and a screen 2407. The invention can be used as the liquid crystal display device 2403, and the semiconductor circuit of the invention can be used as CPU or memory.

Fig. 20F shows a front projector constituted by a main body 2501, a light source 2502, a liquid crystal display device 2503, an optical system 2504 and a screen 2505. The invention can be used as the liquid crystal display device 2503, and the semiconductor circuit of the invention can be used as CPU or memory.

Fig. 21A shows a personal computer which includes a main body 2601, an image input unit 2602, a display unit 2603 and a keyboard 2604. The electro-optical device of the invention can be used as the display unit 2603, and the semiconductor circuit of the invention can be used as CPU or memory.

Fig. 21B shows an electronic play machine (game machine) including a main boy 2701, a recording medium 2702, a display unit 2703, and a controller 2704. The voice and image output from the electronic play machine are reproduced by the display that includes a housing 2705 and a display unit 2706. Wired communication, wireless communication or optical communication can be used as communication means between the controller 2704 and the main body 2701 or as communication means between the electronic play machine and the display. In this embodiment, infrared rays are detected by sensors 2707 and 2708. The electro-optical device can be used as the display units 2703 and 2706, and the semiconductor circuit of the invention can be used as CPU or memory.

Fig. 21C shows a player (picture reproducing apparatus) using a recording medium storing a program (hereinafter referred to as recording medium), which includes a main body 2801, a display unit 2802, a speaker unit 2803, a recording medium 2804 and operation switches 2805. This picture reproducing apparatus uses a DVD (digital versatile disk) or a CD as a recording medium, and enables the user to enjoy listening to music, viewing a movie, playing a game, or playing an internet system. The electro-optical device of the invention can be used as the display unit 2802, CPU or memory.

Fig. 21D shows a digital camera that includes a main body 290a, a display unit 2902, an eyepiece unit 2903, operation switches 2904, and an image-receiving unit (not shown). The electro-optical device of the present invention can be used as the display unit 2902, CPU and memory.

Figs. 22A to 22B illustrates in detail an optical engine that can be used as the rear projector of Fig. 20E or as the front projector of Fig. 2F, and wherein Fig. 22A illustrates the optical engine, and Fig. 22B illustrates a light source optical system contained in the optical engine.

The optical engine shown in Fig. 22A includes a light source optical system 3001, mirrors 3002, 3005 to 3007, dichroic mirrors 3003 and 3004, optical lenses 3008a to 3088c, a prism 3011, a liquid crystal display device 3010, and a projection optical system 3012. The projection optical system 3012 is the one equipped with a projection lens. This embodiment deals with an example of a three-plate type using three liquid crystal display devices 3010, which, however, may be of a single-plate type. An optical lens, a film having a polarizing function, a film for adjusting the phase difference or an IR film may be provided in the optical paths indicated by arrows in Fig. 22A.

As shown in Fig. 22B, further, the light source optical system 3001 includes light sources 3013 and 3014, a synthesizer prism 3015, collimator lenses 3016 and 3020, lens arrays 3017 and 3018, and a polarization conversion element 3019. The light source optical system shown in Fig. 22B uses two light sources. However, only one light source may be used or three or more light sources may be used. Further, an optical lens, a film having a polarizing function, a film for adjusting the phase difference or an IR film may be provided somewhere in the optical path of the light source optical system.

As described above, this invention can be applied over a very wide range and can be adapted to electric appliances of any field. Further, the electric appliances of the embodiment can be realized by using the constitution of any combination of the embodiments 1 to 21.

This invention makes it possible to form TFTs having gate-insulating films of different thicknesses on the same substrate. It is therefore allowed to arrange the circuits having suitable performances that meet specifications required for the circuits in the electronic devices as represented by the AM-LCD or in the semiconductor devices inclusive of electric appliances having such electronic devices as display units, making it possible to greatly enhance the performance and reliability of the semiconductor devices.

In the pixel unit of electronic devices as represented by the AM-LCD, furthermore, a storage capacitor having a large capacity can be formed occupying a small area. This makes it possible to maintain a sufficiently large storage capacity even in the electronic devices having a display unit of a diagonal of not larger than one inch without decreasing the numerical aperture.

WHAT IS CLAIMED IS:

1. A semiconductor device having a pixel unit and a drive circuit unit over a same substrate, comprising:

a plurality of drive TFTs forming said drive circuit unit; and

a plurality of pixel TFTs forming said pixel unit,

wherein at least one of said drive TFTs and one of said pixel TFTs have lightly doped regions in active layers of said drive TFTs and said pixel TFTs, respectively,

wherein said lightly doped region of drive TFTs is arranged to be overlapped on gate wirings of said drive TFTs with a gate-insulating film of said drive TFTs interposed therebetween,

wherein said lightly doped region of pixel TFTs is arranged not to be overlapped on gate wirings of said pixel TFTs with a gate insulating film of said pixel TFTs interposed therebetween, and

wherein at least one storage capacitor of said pixel TFTs are formed by a light-shielding film formed over said pixel TFTs, an oxide of said light-shielding film and pixel electrodes.

2. A semiconductor device having a pixel unit and a drive circuit unit over a same substrate, comprising:

a plurality of drive TFTs forming said drive circuit unit; and

a plurality of pixel TFTs forming said pixel unit,

wherein at least one of said drive TFTs and one of said pixel TFTs have lightly doped regions in active layers of said drive TFTs and said pixel TFTs, respectively,

wherein said lightly doped region of drive TFTs is arranged to be overlapped on gate wirings of said drive TFTs with a gate-insulating film of said drive TFTs interposed therebetween,

wherein said lightly doped region of pixel TFTs is arranged not to be overlapped on gate wirings of said pixel TFTs with a gate insulating film of said pixel TFTs interposed therebetween, and

wherein at least one storage capacitor of said pixel TFTs are formed by a light-shielding film formed over a resin film, an oxide of said light-shielding film and pixel electrodes.

3. A semiconductor device according to claim 1 or 2, wherein said gate-insulating film of said drive TFT has a thickness smaller than a thickness of said gate-insulating film of said pixel TFT.

4. A semiconductor device according to claim 1 or 2, wherein said light-shielding film is an aluminum film or a film comprising mainly aluminum.

5. A semiconductor device according to claim 1 or 2, wherein said oxide is an alumina film.

6. A semiconductor device according to claim 1 or 2, wherein said semiconductor device is an EL display device.

7. A semiconductor device according to claim 1 or 2, wherein said semiconductor device is one selected from the group consisting of a portable telephone, a video camera, a personal computer, a goggle-type display, and a projector.

8. A method of manufacturing a semiconductor device having a pixel unit and a drive circuit unit over a same substrate, comprising:

forming a channel-forming region, a source region, a drain region and at least one lightly doped region sandwiched between either of said source and drain region and said channel-forming region in an active layer of NTFT forming said drive circuit unit;

forming a channel-forming region, a source region and a drain region in an active layer of PTFT forming said drive circuit unit; and

forming a channel-forming region, a source region, a drain region, and at least one lightly doped region sandwiched between either of said source and drain region and said channel-forming region in an active layer of pixel TFT forming said pixel unit,

wherein said lightly doped region of said NTFT forming said drive circuit unit are formed to be overlapped on said gate wiring of said NTFT forming said drive circuit unit with said gate-insulating film interposed therebetween,

wherein said lightly doped region of said pixel TFT are formed not to be overlapped on said gate wiring of said pixel TFT with said gate insulating film interposed therebetween, and

wherein a storage capacitor in said pixel unit are formed by a light-shielding film formed over said pixel TFT, an oxide of a light-shielding film and a pixel electrode.

9. A method of manufacturing a semiconductor device having a pixel unit comprising a plurality of pixel TFTs and a drive circuit unit comprising a plurality of drive TFTs over a same substrate, comprising:

forming an active layer comprising a semiconductor film over said substrate;

forming a gate-insulating film on said active layer;

forming an electrically conducting film on said gate-insulating film;

forming a gate wiring of NTFT forming said drive circuit unit by patterning said electrically conducting film;

forming n-type regions in said active layer of NTFT forming said drive circuit unit by adding an element belonging to the Group 15 of periodic table using said gate wiring of said NTFT forming said drive circuit unit as a mask;

forming n-type regions under said gate wiring of said NTFT forming said drive circuit unit by diffusing said n-type regions by heat treatment;

forming a gate wiring of said pixel TFT by patterning said electrically conducting film;

forming n^{--}-type regions in said active layer of said pixel TFT by adding an element belong to the Group 15 of periodic table by using said gate wiring of said pixel TFT as a mask;

forming n^{+}-type regions in said active layers of NTFTs forming said drive circuit unit and in said active layers of said pixel TFT by adding an element belonging to the Group 15 of periodic table;

forming a gate wiring of said PTFT forming said drive circuit unit by patterning said electrically conducting film;

forming p^{+}-type regions in said active layer of PTFT forming said drive circuit unit by adding an element belong to the Group 13 of periodic table by using said gate wiring of PTFT forming said drive circuit unit as a mask;

forming an interlayer-insulating film comprising a resin film over said NTFT and PTFT forming said drive circuit unit and over said pixel TFT;

forming a light-shielding film on said interlayer-insulating film;

forming an oxide of said light-shielding film on said surface of said light-shielding film; and

forming a pixel electrode in contact with said oxide of said light-shielding film and to be overlapped on said light-shielding film.

10. A method of manufacturing a semiconductor device according to claim 8 or 9, wherein said light-shielding film is an aluminum film or a film comprising mainly aluminum.

11. A method of manufacturing a semiconductor device according to claim 8 or 9, wherein said oxide is an alumina film formed by an anodic oxidation method, a plasma oxidation method or a thermal oxidation method.

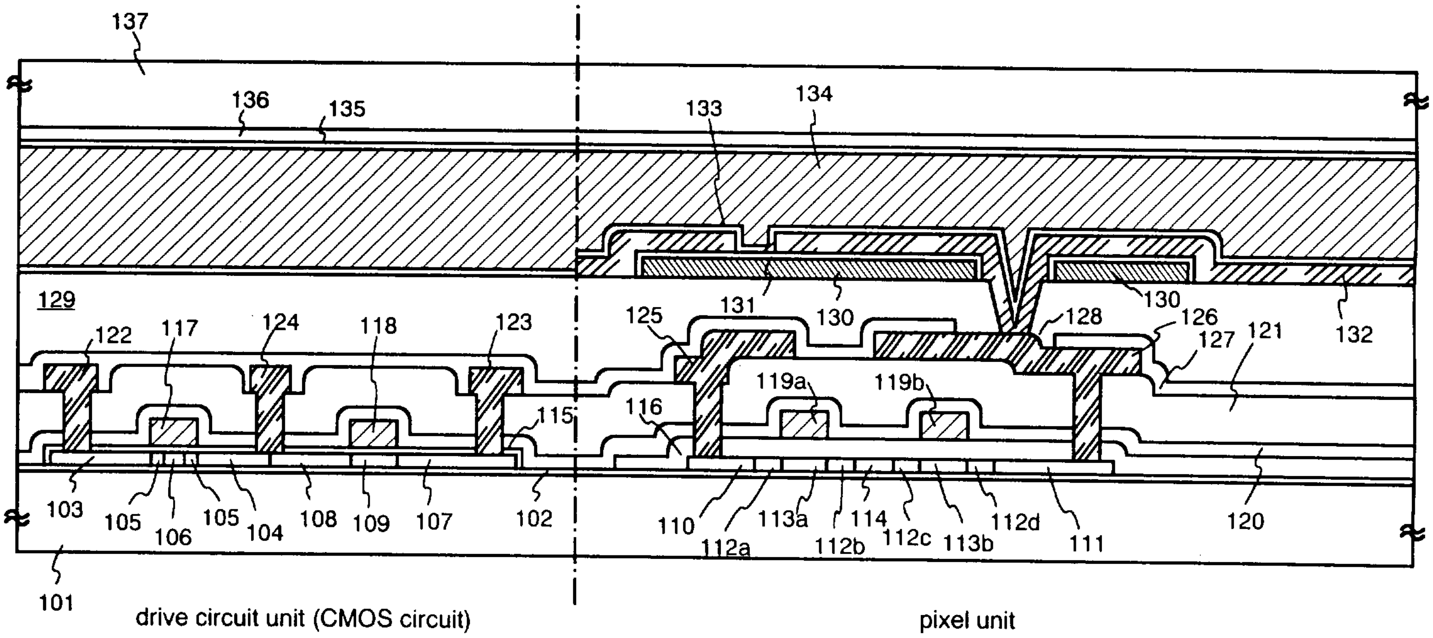
12. A method of manufacturing a semiconductor device according to claim 8 or 9, wherein said semiconductor device is an EL display device.

13. A method of manufacturing a semiconductor device according to claim 8 or 9, wherein said semiconductor device is one selected from the group consisting of a portable telephone, a video camera, a personal computer, a goggle-type display, and a projector.

ABSTRACT OF THE DISCLOSURE

A semiconductor device in which TFTs of suitable structures are arranged depending upon the performances of the circuits, and storage capacitors are formed occupying small areas, the semiconductor device featuring high performance and bright image. The thickness of the gate-insulating film is differed depending upon a circuit that gives importance to the operation speed and a circuit that gives importance to the gate-insulating breakdown voltage, and the position for forming the LDD region is differed depending upon the TFT that gives importance to the countermeasure against the hot carriers and the TFT that gives importance to the countermeasure against the off current. This makes it possible to realize a semiconductor device of high performance. Further, the storage capacity is formed by a light-shielding film and an oxide thereof to minimize its area, and a semiconductor device capable of displaying a bright picture is realized.

Fig. 1



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119a
119b
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108
109
107
102
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112a
113a
112b
114
112c
113b
112d
111
120
101
drive circuit unit (CMOS circuit)
pixel unit

Fig. 2A

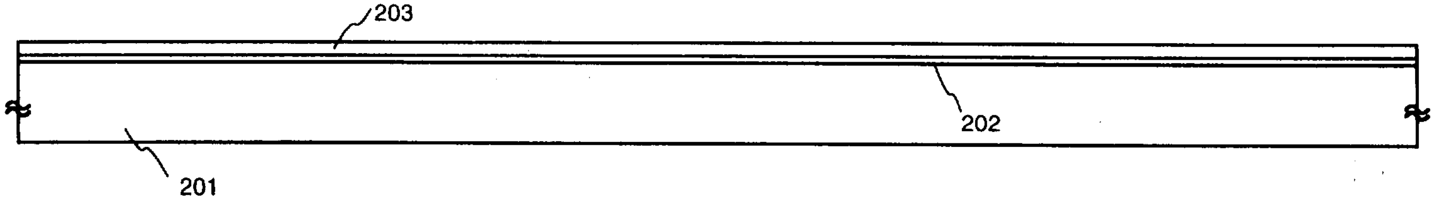


Fig. 2B

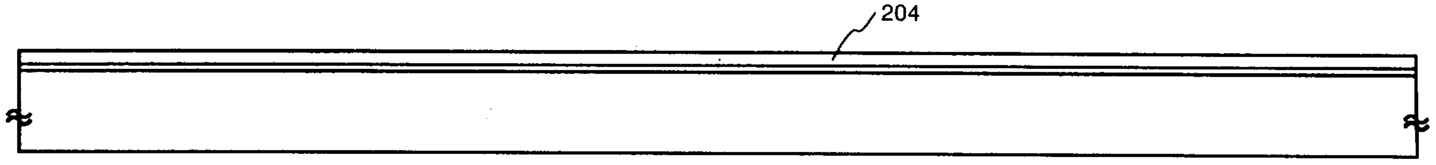


Fig. 2C

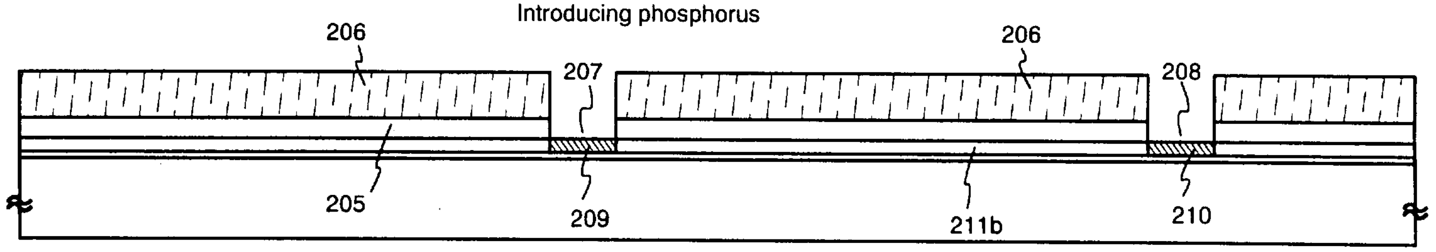


Fig. 2D

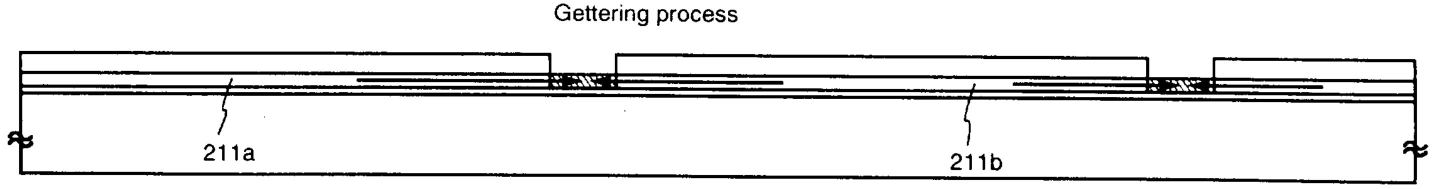


Fig. 3A

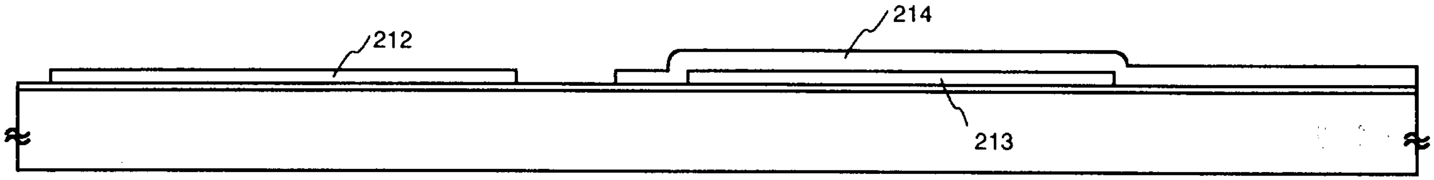


Fig. 3B

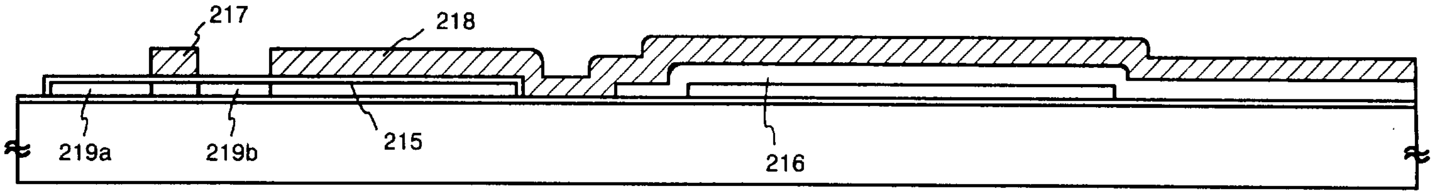


Fig. 3C

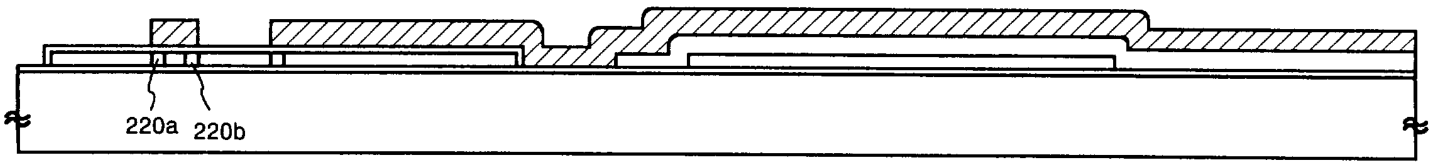


Fig. 3D

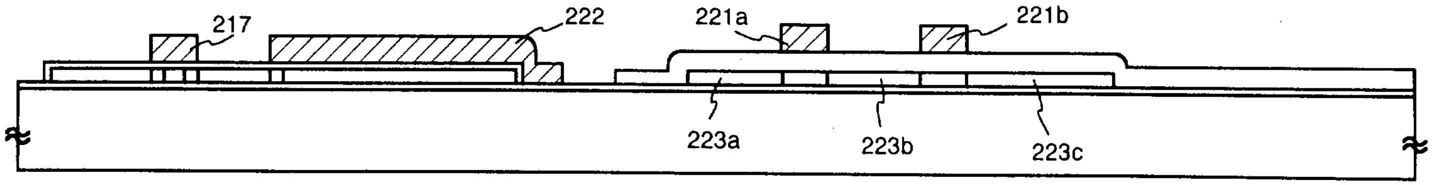


Fig. 4A

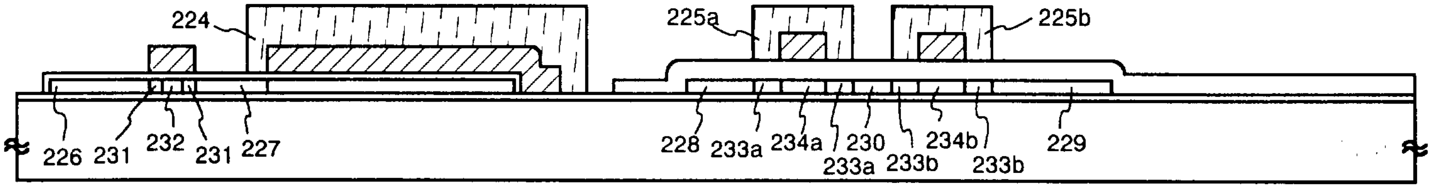


Fig. 4B

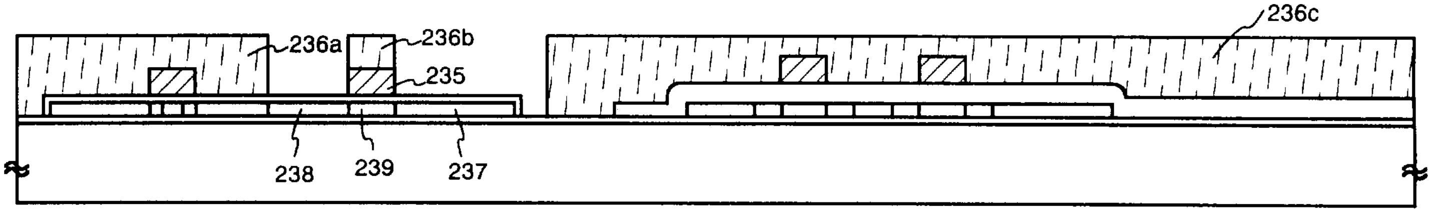


Fig. 4C

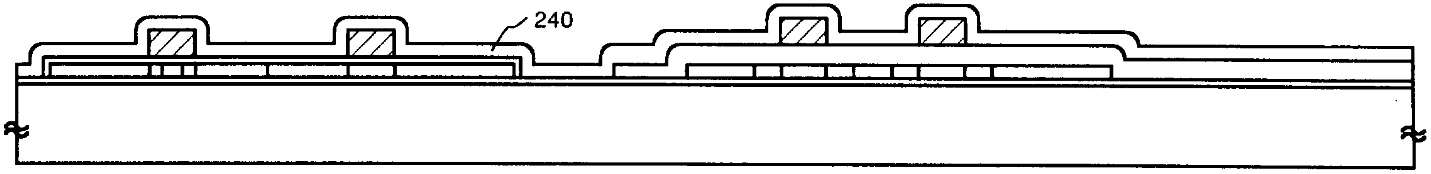


Fig. 4D

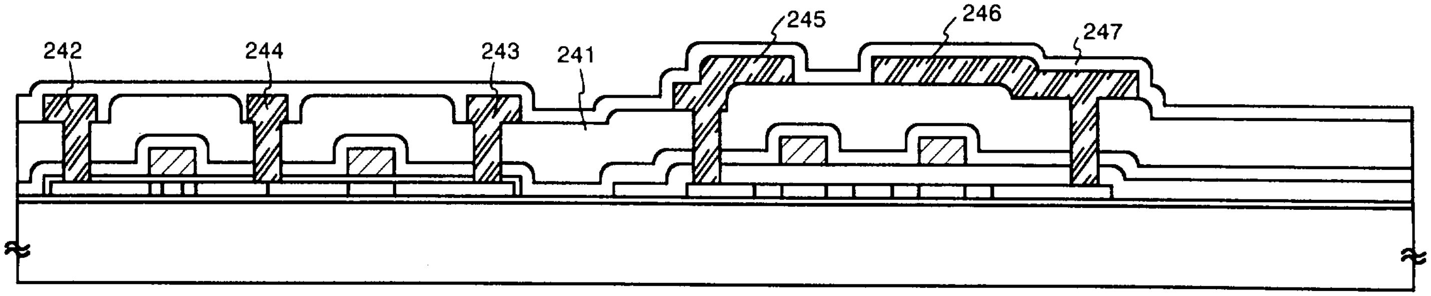


Fig. 5A

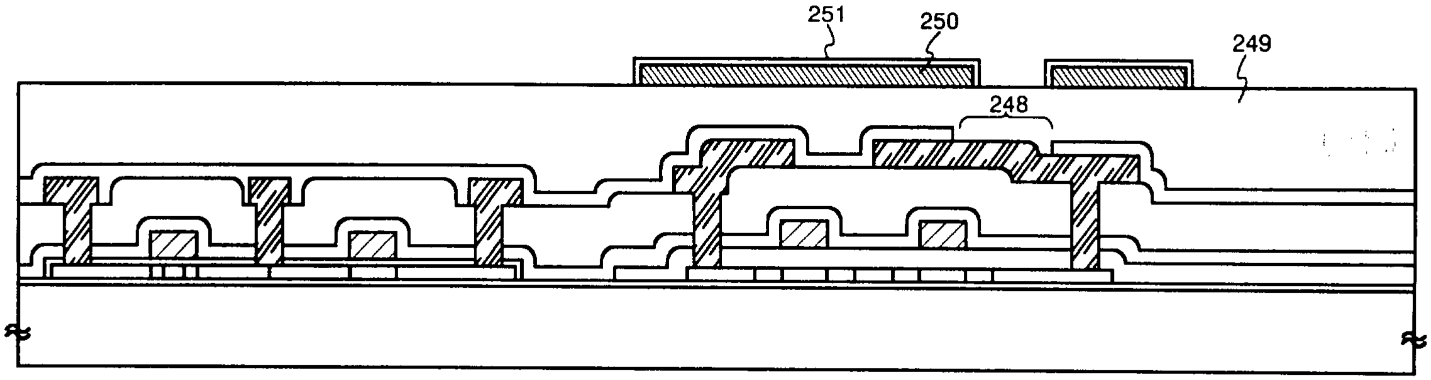

251
250
249
248

Fig. 5B

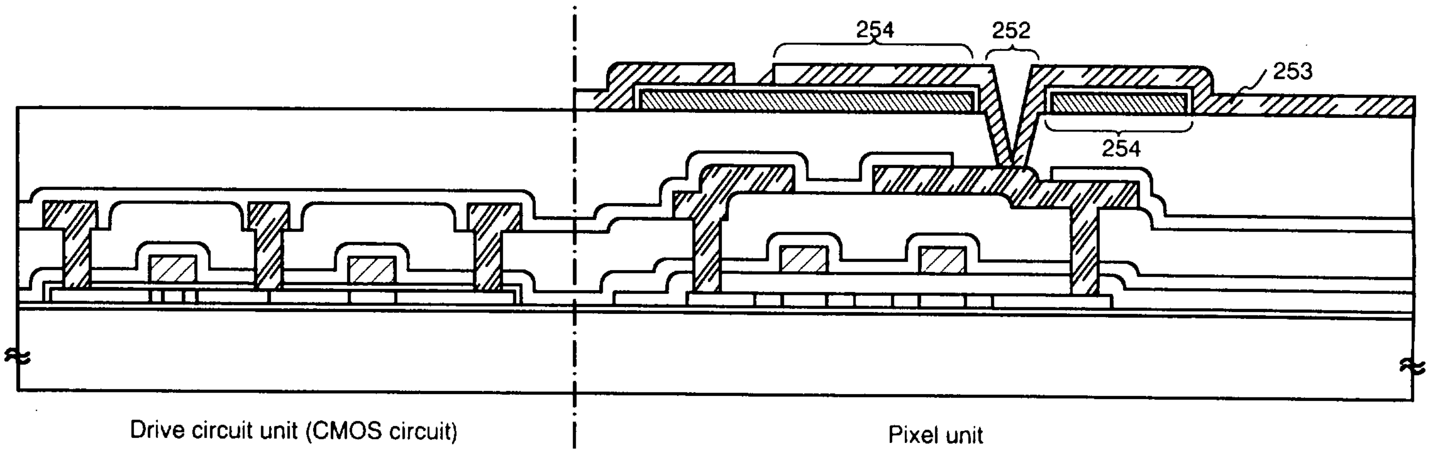

254
252
253
254
Drive circuit unit (CMOS circuit)
Pixel unit

Fig. 6

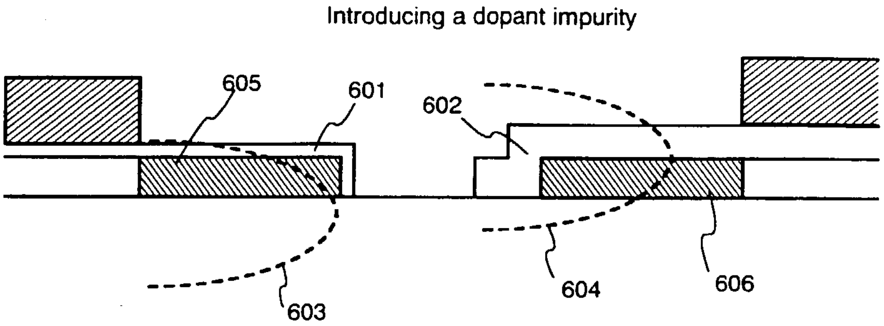


Fig. 7A

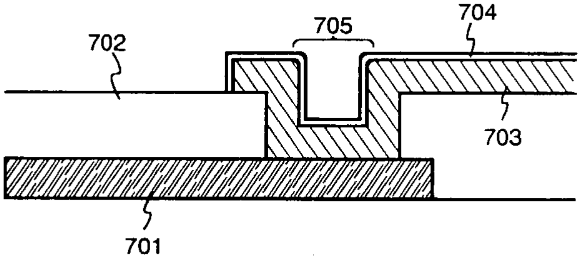


Fig. 7B

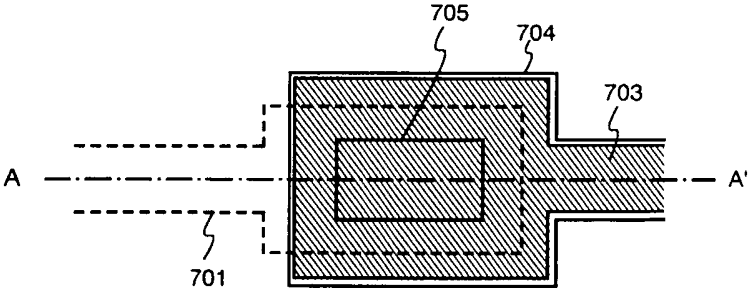


Fig. 8A

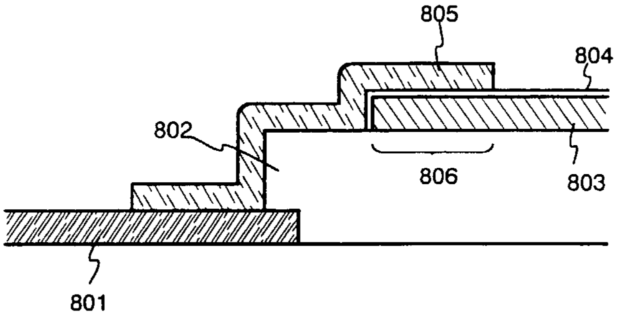


Fig. 8B

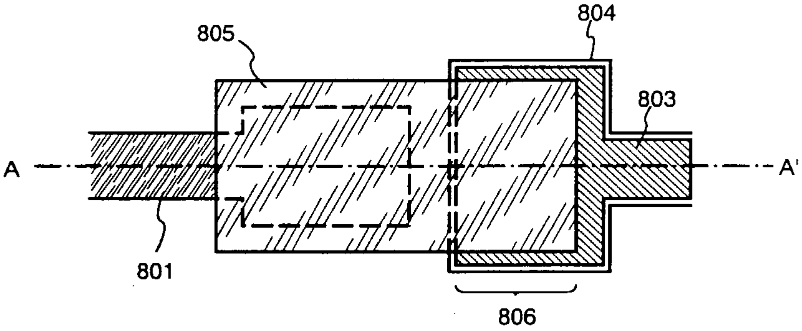


Fig. 9A

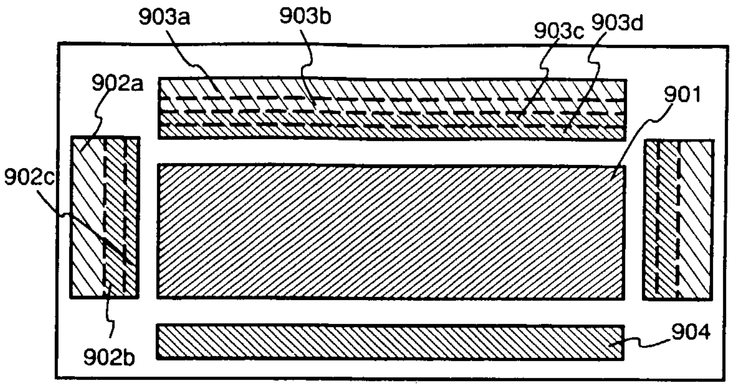
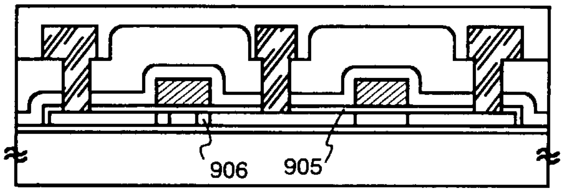
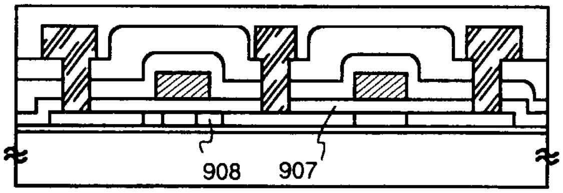


Fig. 9B



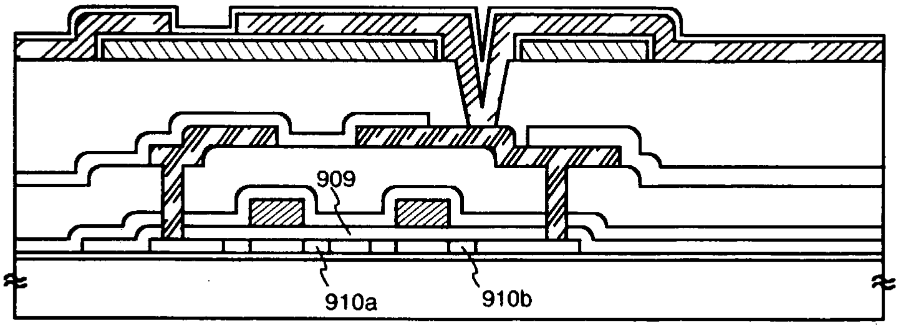
CMOS circuit region shown by the hatching ▧

Fig. 9C



CMOS circuit region shown by the hatching ▨

Fig. 9D



Pixel matrix circuit region shown by the hatching ▨

Fig. 10

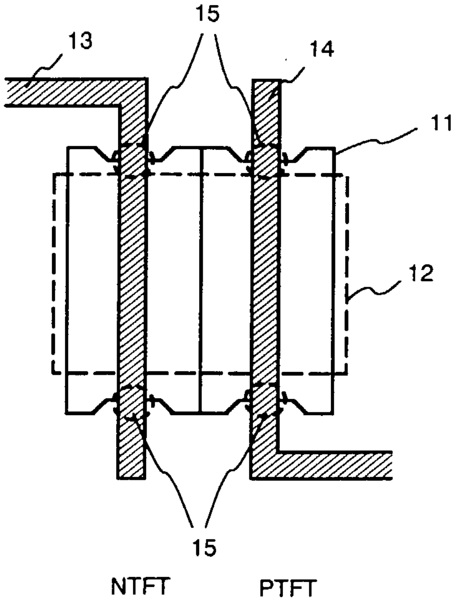


Fig. 11

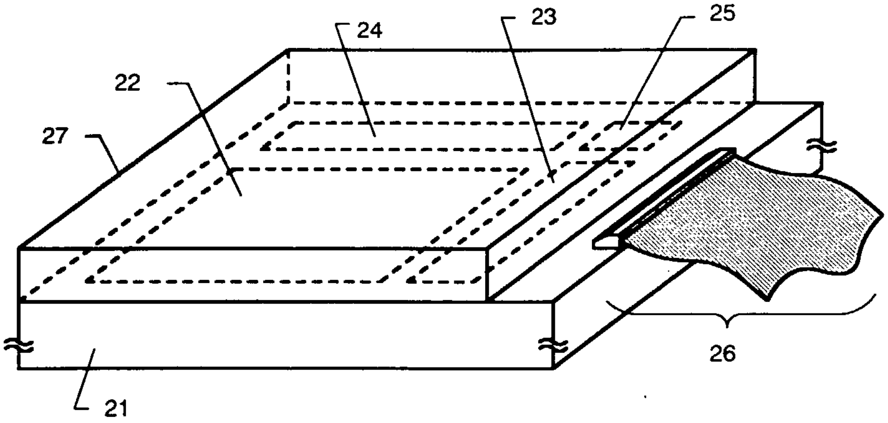


Fig. 12A

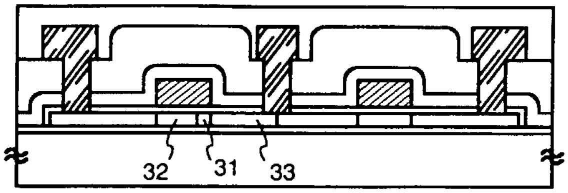


Fig. 12B

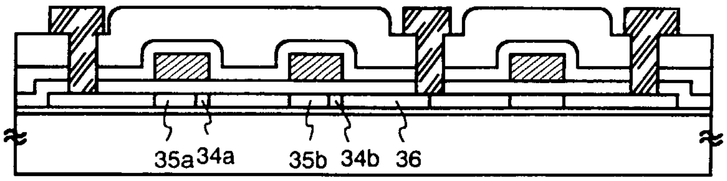


Fig. 13

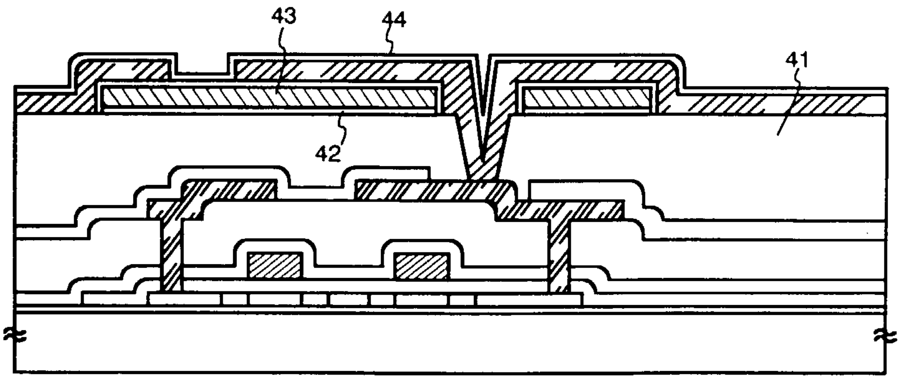


Fig. 14A

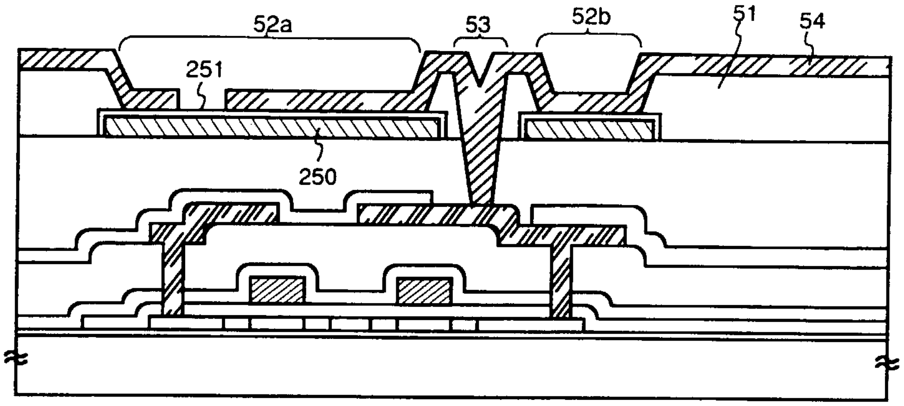
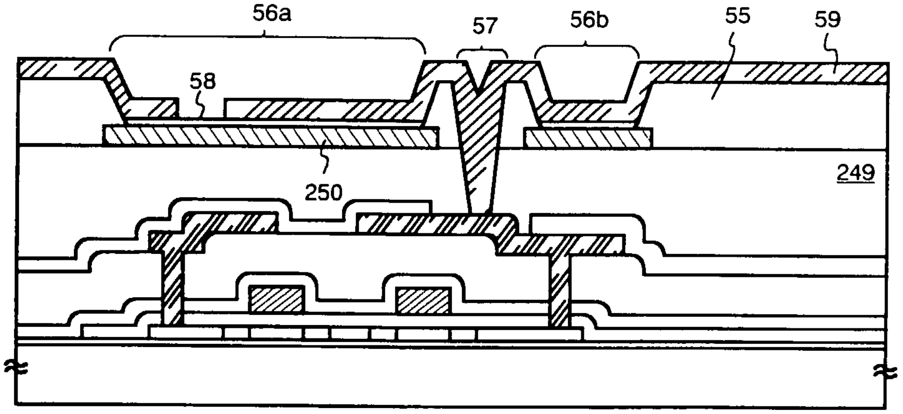


Fig. 14B



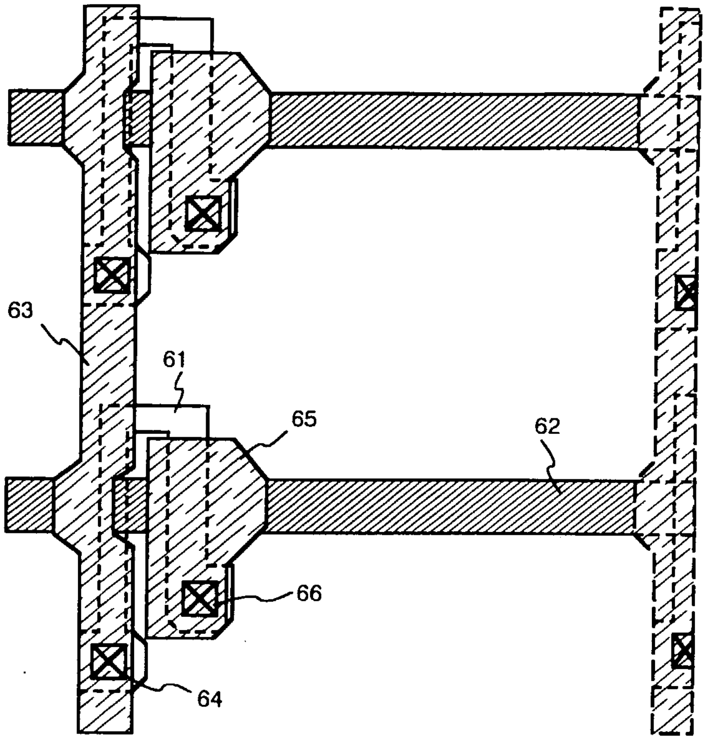


Fig. 15A

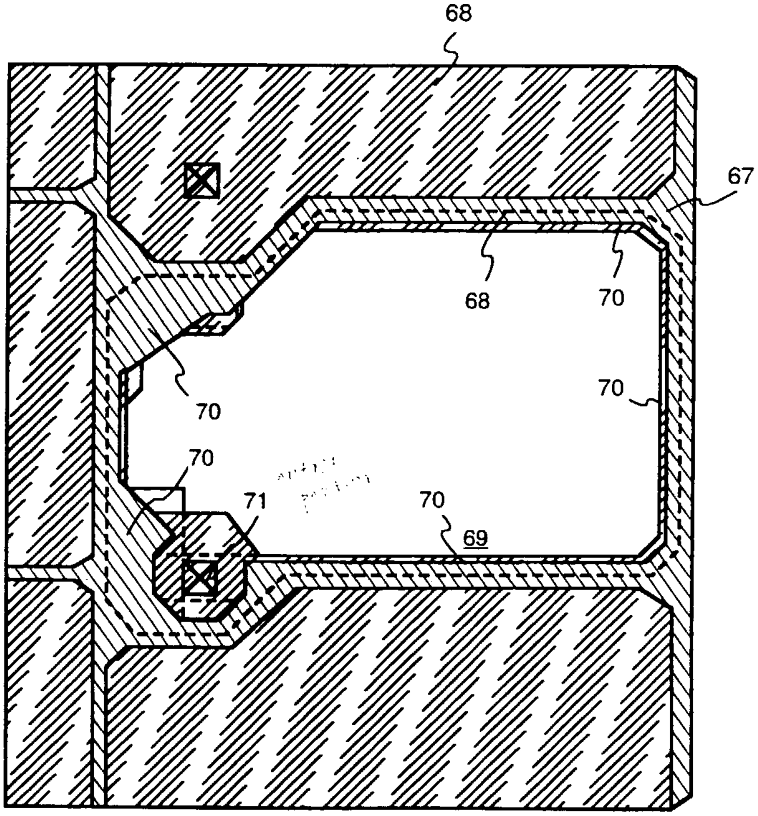


Fig. 15B

Fig. 16A

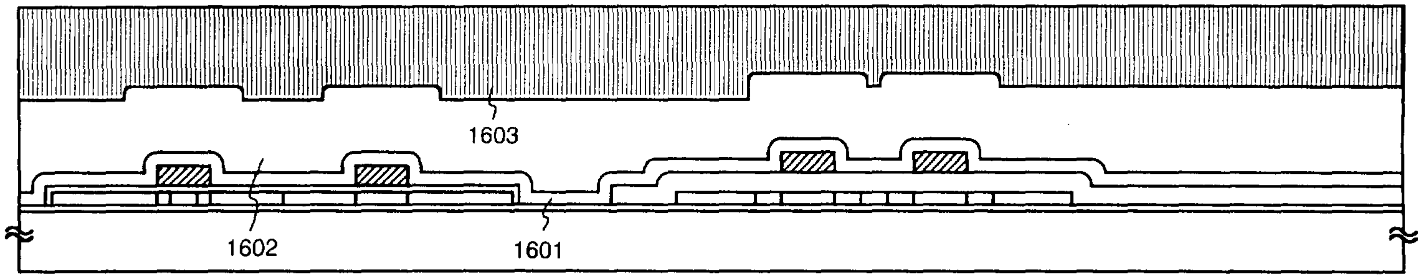


Fig. 16B

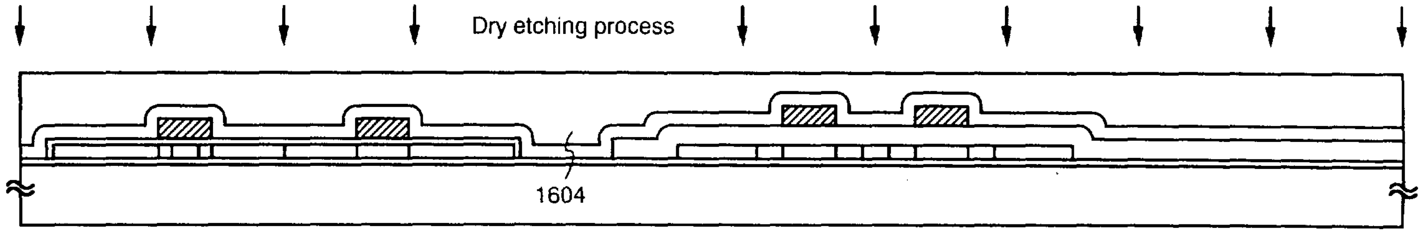
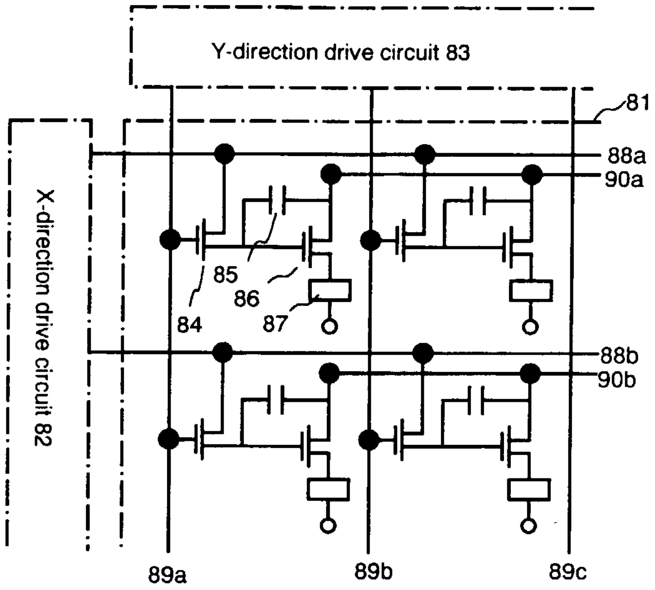


Fig. 17


Y-direction drive circuit 83
81
88a
90a
X-direction drive circuit 82
85
86
84
87
88b
90b
89a
89b
89c

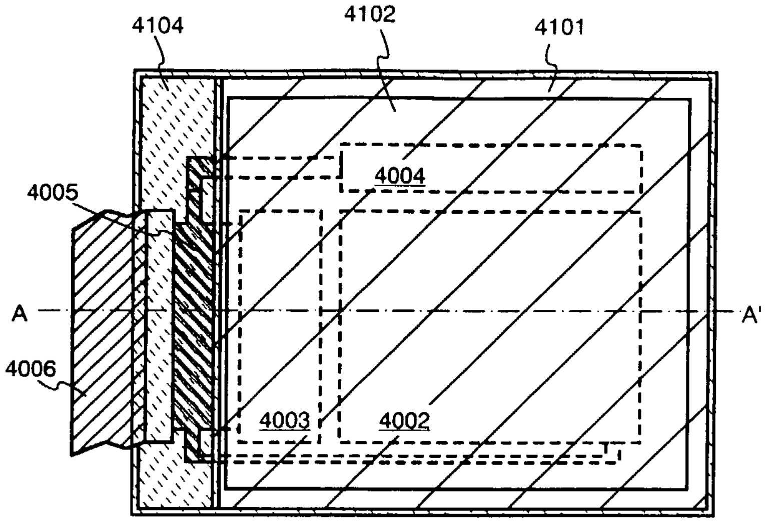


Fig. 18A

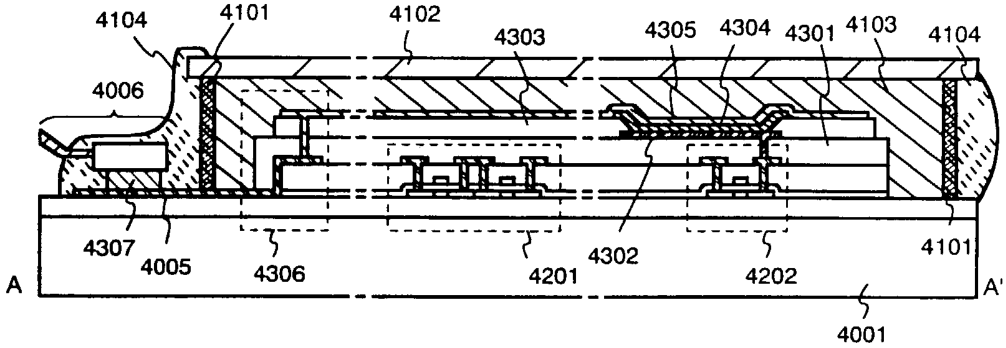


Fig. 18B

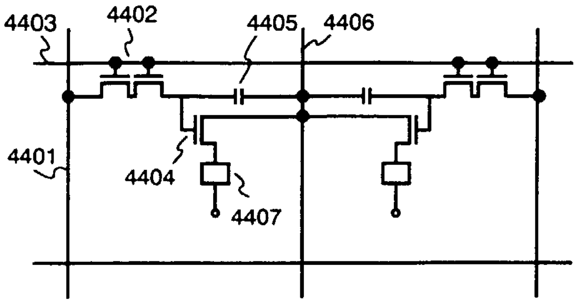


Fig. 19A

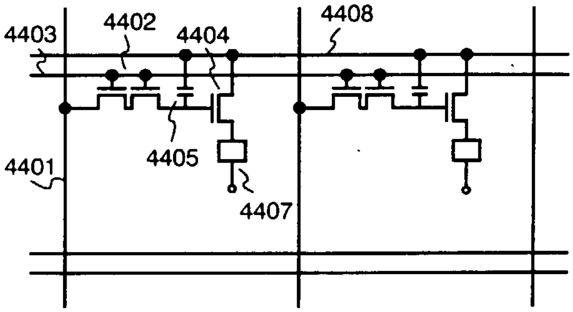


Fig. 19B

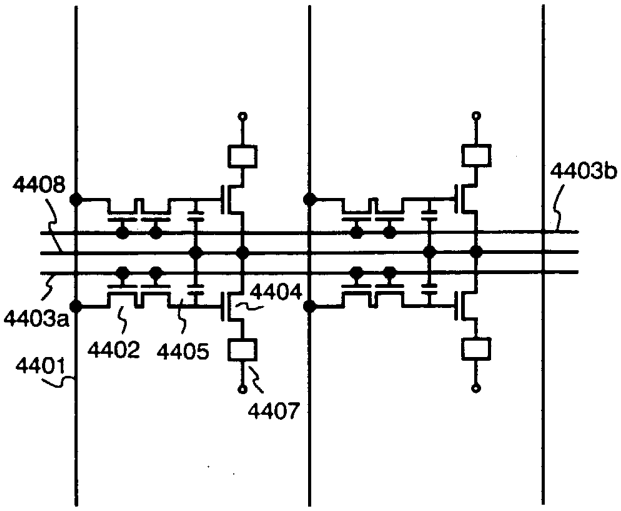


Fig. 19C

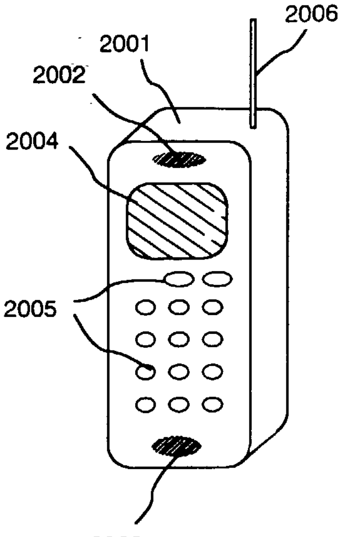


Fig. 20A

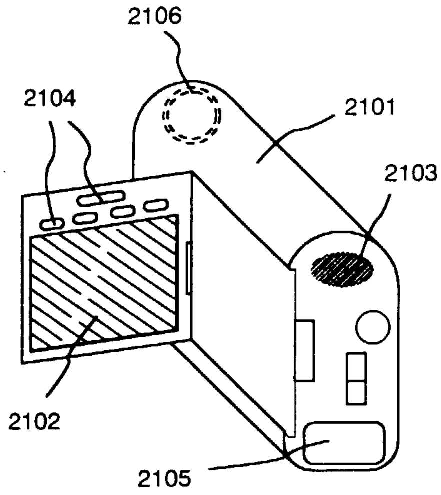


Fig. 20B

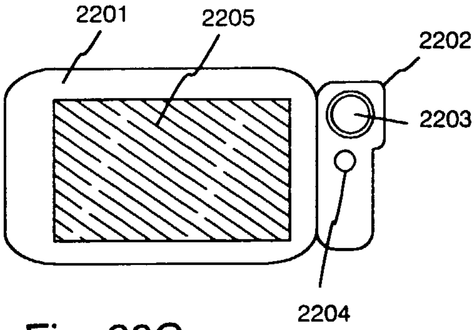


Fig. 20C

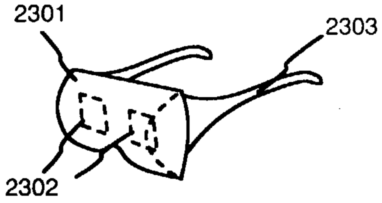


Fig. 20D

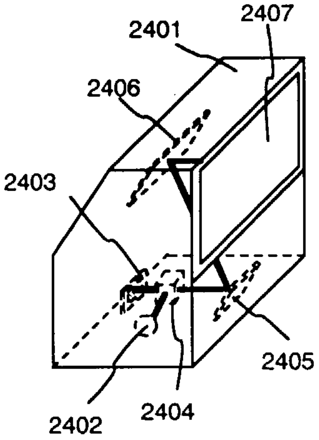


Fig. 20E

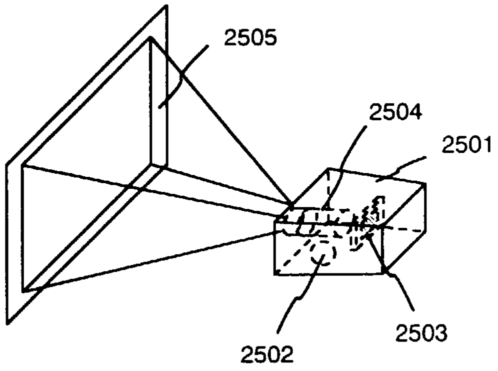


Fig. 20F

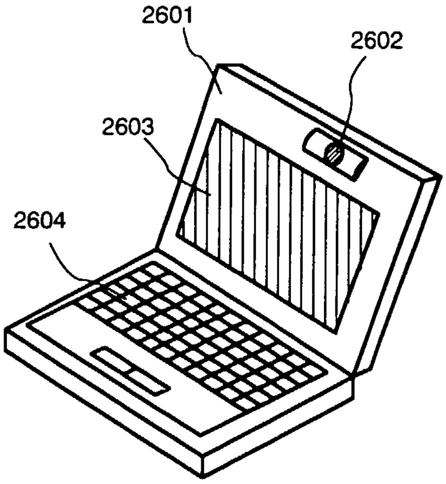


Fig. 21A

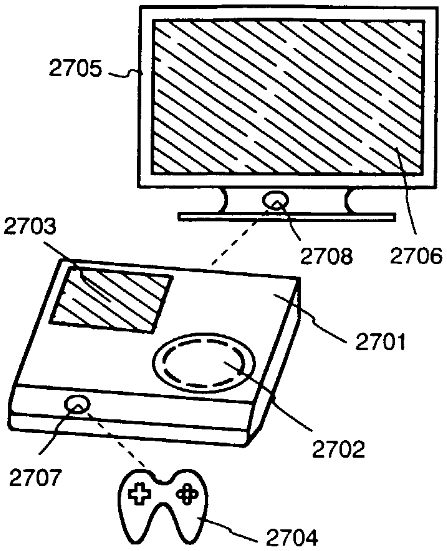


Fig. 21B

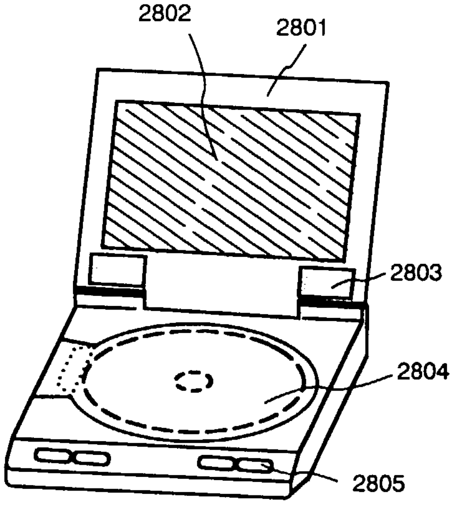


Fig. 21C

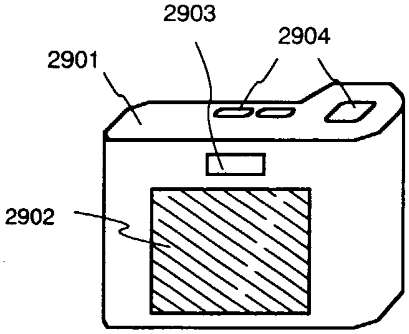


Fig. 21D

Fig. 22A

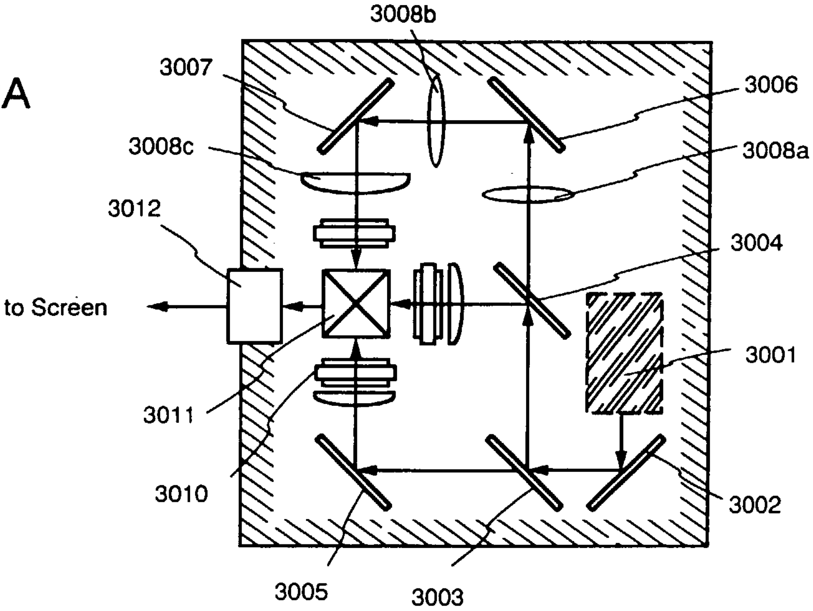
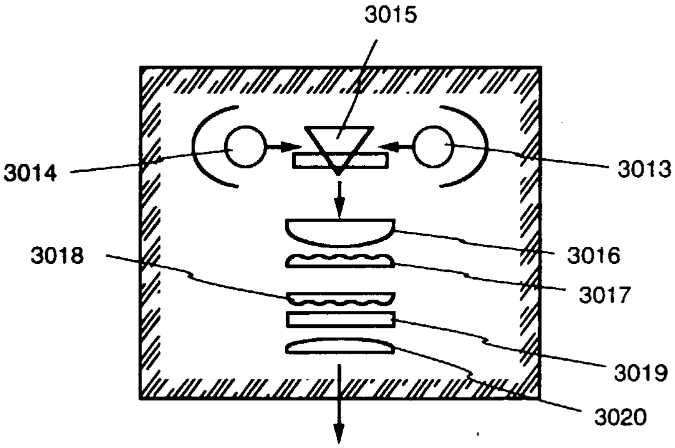


Fig. 22B



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Date Mailed: 04/21/2000

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Applicant(s)

Shunpei Yamazaki, Residence Not Provided;

Continuing Data as Claimed by Applicant

Foreign Applications

If Required, Foreign Filing License Granted 04/20/2000

**

4/24/00

Title

Semiconductor device and method of manufacturing therefor

Preliminary Class

438

Data entry by : MAY, MOLIKI **Team :** OIPE **Date:** 04/21/2000

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THEREFOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device having a circuit comprising a thin film transistor on a substrate having an insulating surface, and a manufacturing method therefor. In particular, the present invention can ideally be used in electro-optical devices, typically liquid crystal display devices in which an active matrix circuit and a driver circuit formed on its periphery, are formed on the same substrate, and in electronic equipment loaded with an electro-optical device. Note that semiconductor device, in this specification, indicates general devices that function by using semiconductor characteristics. Note also that the above stated electro-optical devices, and electronic equipment loaded with the electro-optical device, are included in that category.

2. Description of the Related Art

The development of semiconductor devices having large surface area integrated circuits formed by thin film transistors (hereinafter referred to as TFTs) on a substrate having an insulating surface is advancing. Active matrix type liquid crystal display devices, EL display devices, and contact type image sensors are known as typical examples of such. TFTs are classified by their structure and their method of manufacture. In particular, the electric field effect mobility is high for TFTs (referred to as crystalline, TFTs) in which a semiconductor film having a crystal structure is made into an active layer, so that it is possible to form circuits with a variety of functions.

For example, a pixel section or pixel matrix circuit formed by n-channel TFTs, driver circuits such as a shift register circuit, a level shifter circuit, and a buffer circuit, based on CMOS circuits, and a sampling circuit are formed in each functional block on one substrate in an active matrix type liquid crystal display device. In addition, integrated circuits in a contact type image sensor, such as a sample hold circuit, a shift register circuit, and a multiplexer circuit, are formed using TFTs.

The characteristics of an electric field effect transistor such as a TFT can be considered to be divided into a linear region in which the drain current and the drain voltage increase proportionally, a saturation region in which the drain current is saturated even if the drain voltage increases, and a cut-off region in which ideally current does not flow even if there is an applied drain voltage. The linear region and the saturation region are called the ON region of a TFT, while the cut-off region is called the OFF region in this specification. In addition, for convenience the drain current in the ON region is called the ON current, and the current in the OFF region is called the OFF current.

The operating conditions of the respective circuits are not necessarily identical, so that naturally the characteristics required in the TFT also differ a great deal. In the pixel section, there is a structure formed by an n-channel TFT switching element and an auxiliary storage capacitor, and this is driven by applying a voltage to the liquid crystal. It is necessary to drive the liquid crystal by an alternating current here, and a system called frame inversion driving is employed. Therefore, a required TFT characteristic is the necessity to sufficiently reduce the leakage current. In addition, a high drive voltage is applied to the buffer circuit, so that it is necessary to increase the voltage resistance. Furthermore, it is necessary to sufficiently maintain the ON current in order to increase the current driver performance.

However, there is a problem in that the off current of the crystalline TFT is liable to become large. From the point of reliability, it is still believed that the crystalline TFT fall short of a MOS transistor (a transistor manufactured on a single crystal semiconductor substrate) used in LSIs, etc. For example, a deterioration phenomenon of a drop in the ON current in the crystalline TFT has been observed. The cause of this is the hot carrier effect, and it is thought that the hot carrier generated by the high electric field in the vicinity of the drain causes the degradation phenomenon.

A lightly doped drain (LDD) structure is known in a TFT structure. This structure is formed by a low concentration impurity region between a channel region, and a source region or drain region in which a high concentration of impurities is doped. This low concentration impurity region is called an LDD region. In addition, for the LDD structure, depending upon the positional relationship with the gate electrode, there is an LDD structure that overlaps the gate electrode (hereinafter, this LDD structure is referred to as GOLD (gate-drain overlapped LDD)), and an LDD structure that does not overlap the gate electrode. The high electric field is eased, the hot carrier effect is prevented, and the reliability can be increased with a GOLD structure. For example, there is a GOLD structure in which sidewalls are formed by silicon in Mutsuko Hatano, Hajime Akimoto and Takeshi Sakai, IEDM97 Technical Digest, pp. 523-6, 1997", and compared to TFTs with other structures, it has been confirmed that a very superior reliability can be obtained.

In addition, there is a TFT placed in each of from several tens to several millions of pixels in the pixel section of the active matrix type liquid crystal display device, and a pixel electrode is formed in each of the TFTs. Opposing electrodes are formed on the side of the opposing substrate sandwiching the liquid crystal, forming a kind of capacitor with the liquid crystal as a dielectric. The electric potential applied to each pixel is then controlled by the TFT switching function, and this becomes a structure in which the liquid crystals are driven by controlling the electric charge to the capacitors, controlling the amount of light transmitted and displaying an image.

The capacity of this capacitor gradually decreases due to the leak current, so that this causes the amount of transmitted light to change and the contrast of the image display to be reduced. Capacitor lines are formed conventionally, and a separate capacitor (a storage capacitor) is formed in parallel to the capacitor with the liquid crystal as its dielectric. The storage capacitor works to supplement the capacity lost by the capacitor with the liquid crystal as its dielectric.

However, the required characteristics are not necessarily the same for a TFT as a pixel section switching element and a driver circuit

TFT such as a shift register circuit or a buffer circuit. For example, a large inverse bias voltage (negative for an n-channel TFT) is applied to the gate electrode in the pixel section TFT, but there is basically no operation in which an inverse bias voltage is applied to the driver circuit TFT. In addition, the operation speed of the former may be less than 1/100 that of the latter. Thus it is not preferable to use a similar structure for TFT in which the operating condition and required characteristics differ largely.

Furthermore, compared with an ordinary LDD structure, there is a problem with the GOLD structure in that the OFF current becomes large. In order to prevent an increase in the OFF current, it is possible to make a multi-gate structure in which a plural number of gates are formed between one source and drain pair, but that is insufficient for the GOLD structure TFT. Therefore, it is not necessarily preferable to form all of the TFTs of a large surface area integrated circuit with the same structure. For example, with the n-channel TFT constituting the pixel section, if the OFF current increases, then the power consumption increases and abnormalities in the image display appear, so that it is not desirable to apply the GOLD structure crystalline TFT as is. In addition, there is a problem with the LDD structure that has no overlap with the gate electrode in that the ON current decreases due to an increase in the series resistance. The ON current can be freely designed by the channel width, and for example, it is not always necessary to form the LDD structure that does not overlap the gate electrode in a TFT constituting a buffer circuit.

In addition, if a storage capacitor using capacitor wirings in the pixel section is formed to maintain a sufficient capacity, then the aperture ratio must be sacrificed. In particular, for a small size high definition panel used in a projector type display device, the pixel area for each pixel is also small, , so that the reduction in the aperture ratio due to the capacitor wiring becomes a problem.

SUMMARY OF THE INVENTION

The present invention is a technique for solving this type of problem, and an object of the invention is to realize a crystalline TFT in which reliability equivalent to, or greater than, that of a MOS transistor can be obtained. Another object of the present invention is to increase the reliability of a semiconductor device having a large surface area integrated circuit, in which various types of functional circuits are formed using this type of crystalline TFT. In addition, another object of the present invention is to increase the aperture ratio of an active matrix type liquid crystal display device, in relation to a pixel section TFT and the constitution of a storage capacitor.

In order to solve the above problems, according to one aspect of the present invention, there is provided a semiconductor device having a driver circuit and a pixel section on the same substrate, structured by thin film transistors, characterized in that, considering the operational characteristic required for the thin film transistors in each functional circuit, the driver circuit has: a first thin film transistor having a channel forming region, a third impurity region with one conductivity type forming a GOLD structure, and a first impurity region with one conductivity type forming a source region or a drain region formed on the outside of a gate electrode; a second thin film transistor having a channel forming region, a third impurity region with one conductivity type forming a GOLD structure, a second impurity region with one conductivity type forming an LDD structure formed on the outside of a gate electrode, and a first impurity region with one conductivity type forming a source region or a drain region; a third thin film transistor having a channel forming region, a second impurity region with one conductivity type forming an LDD structure formed on the outside of a gate electrode, and a first impurity region with one conductivity type forming a source region or a drain region; and a fifth thin film transistor having a channel forming region, and a fifth impurity region with the opposite conductivity to one conductivity type, forming a source region or a drain region, and the pixel section has: a fourth thin film transistor having a channel forming region, a fourth impurity region with one conductivity type forming an LDD structure formed on the outside of a gate electrode, and a first impurity region with one conductivity type forming a source region or a drain region.

In addition, another aspect of the present invention is characterized in that a storage capacitor formed in the pixel section is formed by a light shielding film on the fourth thin film transistor through an insulating layer; a dielectric film contacting the light shielding film and a pixel electrode connected to the fourth thin film transistor; and the pixel electrode contacting the dielectric film, and that the storage capacitor is connected to the fourth thin film transistor. The light shielding film is formed from a material with one or plural kinds of elements selected from aluminum, tantalum, and titanium as its main constituent, and it is preferable that the dielectric film be an oxide compound of the light shielding film material. In addition, the dielectric film may be formed from a material selected from silicon nitride, silicon oxide, oxidized silicon nitride, DLC, and polyimide.

In order to solve the above problems, a method of manufacturing a semiconductor device of the present invention is characterized by having: a step of forming plural island shape semiconductor layers on a substrate having an insulating surface; a step of forming a gate insulating film contacting the island shape semiconductor layers; a step of forming gate electrodes contacting the gate insulating film; a step of doping an impurity element with one conductivity type into selected regions of the island shape semiconductor layers, and of forming a first thin film transistor having a first impurity region, and a third impurity region overlapping the gate electrode; a step of doping an impurity element with one conductivity type into selected regions of the island shape semiconductor layers, and of forming a second thin film transistor having a first impurity region, a third impurity region that overlaps the gate electrode, and a second impurity region that does not overlap the gate electrode; a step of doping an impurity element with one conductivity type into selected regions of the island shape semiconductor layers, and of forming a third thin film transistor having a first impurity region, and a second impurity region that does not overlap the gate electrode; a step of doping an impurity element with the opposite conductivity type to one conductivity type into selected regions of the island shape semiconductor layers, and of forming a fifth thin film transistor having a fifth impurity region; and a step of doping an impurity element with one conductivity type into selected regions of the island shape semiconductor layers, and of forming a fourth thin film transistor having a first impurity region, and a fourth impurity region which does not overlap the gate electrode. The first thin film transistor through the fifth thin film transistor are formed on the same substrate, by the same steps, in consideration of the operational characteristics required by each thin film transistors for the various circuit functions.

In addition, according to another aspect of the present invention, it is preferable that a storage capacitor formed in the pixel section is formed by: a step of forming an insulating layer on the fourth thin film transistor; a step of forming a light shielding film on the insulating film; a step of forming a dielectric film contacting the light shielding film; and a step of forming a conductive film contacting the dielectric film. It is preferable that the step of forming the dielectric film contacting the light shielding film be an anodic oxidation process. Therefore, it is preferable that the light shielding film be formed by a material with one or plural kinds of elements selected from aluminum, tantalum, and titanium as its main constituent.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

Figs. 1A to 1C are cross sectional diagrams showing the manufacturing step of a pixel section and a peripheral driver circuit;

Figs. 2A to 2C are cross sectional diagrams showing the manufacturing process of a pixel section and a peripheral driver circuit;

Figs. 3A to 3C are cross sectional diagrams showing the manufacturing process of a pixel section and a peripheral driver circuit;

Fig. 4 is a cross sectional diagram showing the structure of a storage capacitor;

Figs. 5A to 5C are cross sectional diagrams showing the manufacturing process of a storage capacitor;

Figs. 6A to 6D are cross sectional diagrams showing the manufacturing process of a pixel section and a peripheral driver circuit;

Figs. 7A to 7C are cross sectional diagrams showing the manufacturing process of a pixel section and a peripheral driver circuit;

Figs. 8A to 8C are cross sectional diagrams showing the manufacturing process of a pixel section and a peripheral driver circuit;

Fig. 9 is a cross sectional structure diagram of an active matrix type liquid crystal display device;

Fig. 10 is a perspective view of an active matrix type liquid crystal display device;

Figs. 11A and 11B are top views of a pixel section;

Figs. 12A to 12C are cross sectional diagrams showing the structure of a storage capacitor;

Fig. 13 is a circuit block diagram of an active matrix type liquid crystal display device;

Figs. 14A to 14D are cross sectional diagrams showing the structure of a TFT of the present invention;

Figs. 15A to 15C are cross sectional diagrams showing the manufacturing process of a crystalline semiconductor layer;

Figs. 16A and 16E are cross sectional diagrams showing the manufacturing process of a crystalline semiconductor layer;

Figs. 17A to 17E are cross sectional diagrams showing the manufacturing process of a crystalline semiconductor layer;

Figs. 18A to 18F are diagrams showing examples of semiconductor devices;

Figs. 19A to 19C are diagrams showing examples of semiconductor devices;

Figs. 20A to 20D are diagrams showing examples of projectors;

Figs. 21A and 21B are a top view and a cross sectional diagram of an active matrix type EL display device;

Figs. 22A and 22B are a top view and a cross sectional diagram of an active matrix type EL display device;

Fig. 23 is a cross sectional diagram of a pixel section of an active matrix type EL display device;

Figs. 24A and 24B are a top view and a circuit diagram of a pixel section of an active matrix type EL device;

Fig. 25 is a cross sectional diagram of a pixel section of an active matrix type EL display device; and

Figs. 26A to 26C are circuit diagrams of a pixel section of an active matrix type EL display device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[Embodiment mode 1]

The embodiment modes of the present invention are explained using Figs. 1A to 3C. A method of manufacturing a pixel section and driver circuit TFTs formed in the periphery at the same time is explained.

- Process of forming island shape semiconductor layers and gate insulating films

It is preferable to use a non-alkaline glass substrate or a quartz substrate as a substrate 101 in Fig. 1A. In addition, a silicon substrate, and a metallic substrate on which an insulating film is formed on its surface may also be used. A base film 102 is then formed from a silicon oxide film, a silicon nitride film, or an oxidized silicon nitride film by plasma CVD or sputtering to a thickness of between 100 and 400 nm on the surface of the substrate 101 on which the TFTs will be formed. For example, a two layer structure may be used as the base film 102, with a silicon nitride film 102 from 25 to 100 nm, a thickness of 50 nm is used here, and a silicon oxide film 103 from 50 to 300 nm, a thickness of 150 nm is used here. The base film 102 is formed in order to prevent impurity contamination from the substrate, and does not necessarily need to be formed for the case of a quartz substrate being used. An amorphous silicon film is formed next, to a thickness of between 20 and 100 nm on the base film 102, by a known deposition method. Although it depends upon the amount of hydrogen contained in the amorphous silicon film, it is preferable to perform dehydrogenation by heat treatment at between 400 and 500°C for several hours, and it is preferable to perform the crystallization process with the amount of included hydrogen below 5 atom%. Furthermore, the amorphous silicon film may be formed by another manufacturing method such as sputtering or evaporation, but it is preferable to sufficiently reduce the impurity elements of oxygen and nitrogen included in the film. It is possible to form the base film and the amorphous silicon film by the same deposition method here, so that both may be formed in succession. It is possible to prevent contamination of the surface by not once exposing it to the atmosphere after forming the base film, and dispersion in the characteristics of the manufactured TFTs can be reduced. A known laser crystallization technique or thermal crystallization technique may be used for the process of forming a crystalline silicon film from the amorphous silicon film. Further, a crystalline silicon film may be manufactured by a method of thermal crystallization using a catalytic element to promote crystallization of silicon. In addition, a microcrystalline silicon film may be used, and a crystalline silicon film may be directly deposited. Furthermore, a crystalline silicon film may be formed by using a known SOI (silicon on insulator) technique of adhering a single crystal silicon onto a substrate. The unneeded portions of the crystalline silicon film thus formed are removed by etching, forming island shape semiconductor layers 104 to 106. Boron (B) may be doped in advance to a concentration between $1x10^{15}$ and $5x10^{17}$ atoms/cm^3 in the regions of the crystalline silicon film where n-channel TFTs will be formed, in order to control the threshold voltage. A gate insulating film 107 is formed next, having silicon oxide, oxidized silicon nitride, or silicon nitride as its main constituent, covering the island shape semiconductor layers 104 to 106. The gate insulating film 107 may be formed to a thickness of between 10 and 200 nm, preferably from 50 to 150 nm. For example, an oxidized silicon nitride film may be formed to a thickness of 75 nm by plasma CVD with N_2O and SiH_4 as the raw materials, and after that a 115 nm thick gate insulating film may be formed by thermal oxidation at between 800 and 1000°C in a oxygen atmosphere or a mixed atmosphere of oxygen and chlorine. (See Fig. 1A.)

- Formation of second and third impurity regions

In order to form low concentration impurity regions (denoted as a second impurity region and a third impurity region in this invention) that become LDD regions in the n-channel TFT of the CMOS circuit, masks 108 to 111 are formed from resist films over the entire surface of the island shape semiconductor layers 104 and 106, and over the channel forming region of the island shape semiconductor layer 105. A resist mask may be formed at this point in the region that will form peripheral wirings for the island shape semiconductor layers. An impurity element that imparts n-type conductivity is then doped, forming low concentration impurity regions. Phosphorous (P) is doped here by ion doping using phosphine (PH_3). Phosphorous is doped through the gate insulating film 107, into the semiconductor layers below, by this process. It is preferable that the concentration of doped phosphorous be in the range of between $1x10^{16}$ and $1x10^{19}$ atoms/cm^3, and is $1x10^{18}$ atoms/cm^3 here. Thus low concentration impurity regions 112 and 113 are formed where phosphorous is doped in the island shape semiconductor layer 105. Heat treatment is performed afterward in a nitrogen atmosphere at between 400 and 900°C, preferable from 550 to 800°C, for 1 to 12 hours. A process of activating the doped n-type conductivity imparting impurity element is performed by this process. (See Fig. 1B.)

(Forming conductive films for the gate electrodes and the wirings)

A first conductive film 114 is formed to a thickness of 10 to 100 nm from a conductive material with an element selected from tantalum (Ta), titanium (Ti), molybdenum (Mo), and tungsten (W) as its main constituent. It is preferable to use tantalum nitride (TaN) or tungsten nitride (WN) in the first conductive layer. In addition, although not shown in the figures, a silicon film may be formed below the first conductive film to a thickness of approximately 2 to 20 nm. Furthermore, a second conductive film 115 is formed on the first conductive film 114 to a thickness of 100 to 400 nm from a conductive material with an element selected from Ta, Ti, Mo, and W as its main constituent. For example, Ta may be formed to a 200 nm thickness. (See Fig. 1C.)

When using a Ta film as the second conductive film 115, it is possible to form it by sputtering. Ar gas is used as the sputtering gas for the Ta film. In addition, if an appropriate amount of Xe or

Kr is added into the sputtering gas, then the internal stress of the formed film is relaxed and the film can be prevented from peeling. An α phase Ta film has a resistivity of approximately 20 μ cm and can be used in a gate electrode, but a β phase Ta film has a resistivity of approximately 180 μ cm and is unsuitable for use in a gate electrode. However, a TaN film possesses a crystal structure which is close to that of α phase, so that an α phase Ta film can easily be obtained provided that it is formed on top of a TaN film. Therefore, the first conductive film 114 may be formed of a TaN film with a thickness of between 10 and 50 nm. It is preferable that the resistivity of the Ta film be in the range of between 10 and 50 μ cm.

When using a W film as the second conductive film, W is used as a target for sputtering, argon (Ar) gas and nitrogen (N_2) gas are introduced, and the first conductive film 114 is formed by a tungsten nitride (WN) film. The second conductive film 115 is formed of the W film by using sputtering with Ar gas. In addition, it is possible to form the W film by thermal CVD using tungsten hexafluoride (WF_6). Whichever is employed, in order to be used as a gate electrode there is a necessity to reduce the resistance, and it is preferable to make the resistivity of the W film below 20 μ cm. By increasing the grain size of the W film a lowering of resistivity can be done, but in the case where there is a lot of impurity elements such as oxygen throughout the W film, crystallization is inhibited and it becomes high resistance. From this, when sputtering is employed, by forming the W film using a W target with 99.9999% purity, and in addition by providing sufficient forethought so that impurities are not mixed into the gas phase during deposition, a resistivity of between 9 and 20 μ cm can be realized.

- Forming the gate electrode (p-ch), wiring electrode, and fifth impurity region

Resist masks 116 to 119 are formed, and a portion of the first conductive film and the second conductive film is removed by etching, forming a p-channel TFT gate electrode 120, and gate electrodes 122 and 123. An n-channel TFT gate electrode is formed by a later process, so the first conductive film and the second conductive film are left on the entire surface of the semiconductor layers 105 and 106. A process is then performed to dope an impurity element that imparts p-type conductivity into the portion of the semiconductor layer 104 on which the p-channel TFT is formed, with the resist masks 116 to 119 remaining as is as a mask. Boron is doped as the impurity element by ion doping using diborane (B_2H_6). Boron is doped to a concentration of $2x10^{20}$ atoms/cm^3 here. Fifth impurity regions 125 and 126, doped with a high concentration of boron, are then formed as shown in Fig. 2A. In addition, the resist masks 116 to 119 may be used and a portion of the gate insulating film 107 is removed by etching in this process, and after exposing a portion of the island shape semiconductor layer 104, a process of doping an impurity element that imparts p-type conductivity may be performed.

- Formation of gate electrode (n-ch)

Resist masks 127 to 130 are formed, and n-channel TFT gate electrodes 131 and 132 are formed. At this point the gate electrode 131 is formed so as to overlap with a portion of the low concentration impurity regions 112 and 113. (See Fig. 2B.)

- Formation of first impurity region

Resist masks 134 to 136 are formed, and a process of forming first impurity regions that function as a source region or a drain region in the n-channel TFT is performed. The resist mask 136 is formed in a shape that covers the n-channel TFT gate electrode 132. This is in order to form a fourth impurity region that becomes an offset LDD region in the n-channel TFT of the pixel section. An impurity element that imparts n-type conductivity is then doped, forming first impurity regions 139 to 143. An ion doping process is also performed here using phosphine (PH_3). It is preferable to make the phosphorous concentration in this region between $1x10^{19}$ and $1x10^{21}$ atoms/cm^3, and it is set at $1x10^{20}$ atoms/cm^3 here. In addition, phosphorous is doped at the same time into a portion of the regions 125 and 126 of the island shape semiconductor layer 104, into which boron has been doped, forming regions 137 and 138. (See Fig. 2C.)

- Formation of fourth impurity region

A process of doping an impurity element that imparts n-type conductivity is performed in order to form a low concentration impurity region (denoted as fourth impurity region in this invention) that becomes an LDD region in the island shape semiconductor layer 106 of the pixel section n-channel TFT. It is preferable that the concentration of phosphorous doped be the same or lower than that of the second and third impurity regions, and it is set to $2x10^{17}$ atoms/cm^3 here. Low concentration impurity regions 144 to 147 doped with phosphorous are then formed in the island shape semiconductor layers. (See Fig. 3A.)

- Thermal activation process

A first interlayer insulating film 148 is formed on the entire surface of the gate insulating film and the gate electrodes (for cases when a portion of the island shape semiconductor layers 104 to 106 is exposed, on that upper surface as well). The first interlayer insulating film may be formed of a silicon nitride film, a silicon oxide film, or an oxidized silicon nitride film. In addition, a two-layer structure of a silicon nitride film with a silicon oxide film or an oxidized silicon nitride film may also be used (not shown in the figures). Whichever is used, the first interlayer insulating film may be formed so that its thickness is between 500 and 1000 nm. A heat treatment process is performed next in order to activate the impurity elements that impart n-type or p-type conductivity and have been doped at respective concentrations. This process can be performed by thermal annealing using an electric furnace or by rapid thermal annealing (RTA) using a halogen lamp. The activation process is performed by thermal annealing here. Heat treatment is performed in a nitrogen atmosphere at between 300 and 700° C, preferably from 350 to 550° C, and for example is performed at 525° C for two hours. For cases in which the crystalline silicon film is manufactured by a thermal crystallization method using a catalytic element to promote crystallization of the silicon in the crystallization process of the semiconductor layer, a gettering effect in which the catalytic element is segregated in regions doped with phosphorous is obtained at the same time, and the catalytic element can be removed from the channel forming region. In addition, heat treatment is performed in an atmosphere containing between 3 and 100% hydrogen for 1 to 12 hours at between 300 and 450° C, performing a hydrogenation process of the island shape semiconductor layers. A plasma hydrogenation method may be used for this process, and heat treatment may be performed at between 200 and 450° C in the hydrogen atmosphere generated by the plasma. (See Fig. 3B.)

- Formation of source and drain wiring, and interlayer insulating film

Contact holes are next formed in the first interlayer insulating film 148 to reach the source region and the drain region of the respective TFTs. Source wirings 149, 150, and 151, and drain wirings 152 and 153 are then formed. Although not shown in the figures, a three layer structure of a 100 nm Ti film, a 300 nm Al film which includes Ti, and a 150 nm Ti film formed by successive sputtering is used in embodiment mode 1 for the electrodes. A passivation film 154 is then formed on the first interlayer insulating film, the source wirings, the drain wirings, and the respective wiring electrodes. The passivation film 154 is formed to a thickness of 50 to 500 nm by a silicon nitride film, a silicon oxide film, or an oxidized silicon nitride film. If a hydrogenation process is performed next in this state, then a desirable result can be obtained with regard to improving the TFT characteristics. For example, performing heat treatment at 300 to 450° C for 1 to 12 hours in an atmosphere containing between 3 and 100% hydrogen is good, and a similar result can be obtained by using a plasma hydrogenation method or performing heat treatment at 200 to 450° C in a hydrogen atmosphere generated by the plasma. Next, a second interlayer insulating film 155 is formed from an organic resin to approximately 1000 nm. Polyimide, acrylic, and polyimide amide can be used as the organic resin film. The following points can be given as the benefits of using an organic resin film: the ease of film deposition; the parasitic capacity can be reduced because the specific dielectric constant is low; and superior flatness. Note that organic resin films other than those stated above can also be used. A thermal polymerization type polyimide is used here, and after application to the substrate, it is formed through firing at 300° C.

- Formation of storage capacitor and pixel electrode

A light shielding film 156 is formed on the second interlayer insulating film of the pixel section. The light shielding film 156 is a film with an element selected from aluminum (Al), titanium (Ti), and tantalum (Ta) as its main constituent, and is formed to a thickness of 100 to 300 nm. Then with the object of forming a storage capacitor in this section, a dielectric film 157 is formed on the light shielding film 156 with a thickness of between 50 and 200 nm. An oxidized film formed on the surface of the light shielding film 156 by using anodic oxidation may be used for the dielectric film 157. In addition, a silicon oxide film, a silicon nitride film, and an oxidized silicon nitride film, a DLC (diamond like carbon) film, and a polyimide film may also be used. However, the specific dielectric constant of polyimide is between 3 and 4 while the specific dielectric constant of Al oxide is between 7 and 9, for example, so that the latter is extremely suitable for the objective of forming a large capacity with a small surface area.

In concrete, an aluminum oxide is formed by anodic oxidation onto an aluminum film and an electrode of 0.785 mm^2 is formed thereon. As a result of measuring the capacitance, 110 pF at the aluminum oxide film thickness 50 nm and 630 pF at the aluminum oxide film thickness 100nm were obtained. This capacitance value was 2-3 times as much in the case of forming polyimide in the same thickness. Although depending on the pixel size, the storage capacitor disposed in the pixel section of a liquid crystal display device require a capacitance of 100-300 pF. Formation of the storage capacitor by using an aluminum oxide film enabled the area of approximately 1/3 as that required to obtain the same capacitance in a case when polyimide was used.

A contact hole is then formed to reach the drain wiring 153 by an open section 159 formed in the second interlayer insulating film 155 and an open section 158 formed in the passivation film 154, and a pixel electrode 160 is formed. A transparent conductive film may be used for the pixel electrode 160 for the case of a transmission type liquid crystal display device, and a metallic film may be used for the case of a reflection type liquid crystal display device. A transmission type liquid crystal display device is taken here, so that an indium tin oxide (ITO) film is formed here by sputtering to a thickness of 100 nm. The pixel electrode 160 is formed extending through the dielectric film 157 to the light shielding film 156, and a storage capacitor 184 is formed in the region in which the pixel electrode 160 and the light shielding film 156 overlap. (See Fig. 3C.)

An active matrix substrate, in which an n-channel TFT 183 is formed in the pixel section, and a p-channel TFT 181 and an n-channel TFT 182 are formed on the same substrate in the surrounding driver circuit, is thus manufactured by the above processes.

A channel forming region 161, and fifth impurity regions 162 and 163, which function as a source or a drain region, are formed in the p-channel TFT 181 of the driver circuit. The fifth impurity region 162 is then made a source region, and the fifth impurity region 163 becomes a drain region. In addition, a channel forming region 164, and first impurity regions 165 and 166, and third impurity regions 167 and 168 that overlap with the gate electrode through the gate insulating film and function as LDD regions, are formed in the n-channel TFT 182. The first impurity region 165 functions as a source region, and the first impurity region 166 functions as a drain region.

Channel forming regions 169 and 170, first impurity regions 171, 172, and 173, which function as source or drain regions, and fourth impurity regions 174 to 177, which function as LDD regions and do not overlap the gate electrode through the gate insulating film, are formed in the n-channel TFT 183 of the pixel section.

By considering the operating environment of the respective n-channel TFTs of the pixel section and the driver circuit, and differing the length in the longitudinal direction of the channel of the second impurity regions, the third impurity regions, and the fourth impurity regions, which become LDD regions, on the same substrate, the present invention can build-in an optimal shape for the TFTs which structure the respective circuits. The n-channel TFT 182 is suitable for a logic circuit with a drive voltage of approximately 10 V. The length of the LDD region (the third impurity region) that overlaps the gate electrode (L_{ov}) may be made from 0.5 to 3.0 μm, typically 1.5 μm, for a channel length of between 3 and 7 μm. Further, the n-channel TFT 183 of the pixel section is a multi-gate structure, but in order to reverse its polarity and drive it, the fourth impurity regions 174 to 177 that become LDD regions, which do not overlap the gate electrode are formed on both the source side and the drain side. These regions may have a length (L_{off}) from 0.5 to 3.5 μm, typically 2.0 μm.

Thus as above, by optimizing the structure of the TFTs that constitute each circuit in response to the respective specifications of the pixel section and the driver circuits, the present invention can make it possible to raise the operating performance and the reliability of a semiconductor device. Specifically, by respectively differing the design of the LDD regions of the n-channel TFTs in response to each circuit specification, and by appropriately forming LDD regions that overlap the gate electrode, or LDD regions that do not overlap the gate electrode, a TFT structure that places great importance on a countermeasure against deterioration by hot carriers, and a TFT structure that places great importance on a low off current value, can be obtained.

[Embodiment Mode 2]

Another structure for the storage capacitor connected to the n-channel TFT of the pixel section of the active matrix substrate is explained. Fig. 4 shows a cross sectional structure diagram of the pixel section of the active matrix substrate manufactured similar to that of embodiment mode 1.

Base films 402 and 403 are formed on a substrate 401, and a first impurity region and a fourth impurity region are formed in an island shape semiconductor layer 404. A gate electrode 406 is formed on a gate insulating film 405, and a source wiring 408 and a drain wiring 409 are formed on a first interlayer insulating film 407. A light shielding film 412 and a pixel electrode 418 are then formed over a passivation film 410 and a second interlayer insulating film 411.

A storage capacitor 421 connected to an n-channel TFT 420 is formed from the light shielding film 412 formed on the second interlayer insulating film 411, a dielectric film 413 formed on that, and the pixel electrode 418. In addition, a spacer 414, an insulating body, is formed in the region that forms an opening in the second interlayer insulating film, and the pixel electrode 418 is connected to the drain wiring 409 by an opening 415 formed in the passivation film 410, by an opening 416 formed in the second interlayer insulating film 411, and by an opening 417 formed in the spacer 414. By thus forming the spacer 414, shorts can be prevented from being generated between the light shielding film and the pixel electrode. The storage capacitor 421 is formed in the portion in which the light shielding film 412, the dielectric film

413, and the pixel electrode 418 overlap.

[Embodiment mode 3]

Another structure of a storage capacitor connected to the n-channel TFT of the pixel section is shown in Figs. 5A to 5C. Fig. 5A is a pixel section n-channel TFT manufactured similar to that of embodiment mode 1. Base films 502 and 503 are formed on a substrate 501, and a first impurity region and a fourth impurity region are formed in an island shape semiconductor layer 504. A gate electrode 506 is formed on a gate insulating film 505, and a source wiring 508 and a drain wiring 509 are formed on a first interlayer insulating film 507. In addition, a light shielding film 512 and a spacer 513 formed by an organic resin are formed over a passivation film 510 and a second interlayer insulating film. A dielectric film 514 is next formed on the surface of the light shielding film by anodic oxidation, as shown in Fig. 5B. A pixel electrode 518 is connected to the drain wiring 509 by an opening 515 formed in the passivation film 510, by an opening 516 formed in a second interlayer insulating film 511, and by an opening 517 formed in the spacer 513, as shown in Fig. 5C. A storage capacitor 521 is formed in the portion in which the light shielding film 512, the dielectric film 514, and the pixel electrode 518 overlap. Thus shorts can be prevented from being generated between the light shielding film and the pixel electrode by forming the spacer 513, and further, the dielectric film 514 can be prevented from wrapping around the edge portions when being formed on the surface of the light shielding film 512.

[Embodiment 1]

A method of manufacturing a pixel section and its driver circuits on the same substrate is explained in embodiment 1 by refering Figs. 6A to 8C. For convenience, this type of substrate is called an active matrix substrate in this specification. First, an oxidized silicon nitride film 602a is formed to a thickness of between 50 and 500 nm, typically 100 nm, on a substrate 601 as a base film. The oxidized silicon nitride film 602a is manufactured from SiH_4, N_2O, and NH_3, and the concentration of included nitrogen is set to greater than 25 atomic% and less than 50 atomic%. Heat treatment is performed next at 450 to 650°C in a nitrogen atmosphere, making the oxidized silicon nitride film 602a more dense. Further, an oxidized silicon nitride film 602b is formed to a thickness of 100 to 500 nm, typically 200 nm, and a 20 to 80 nm thick amorphous semiconductor film (not shown in the figures) is formed in succession. A crystalline silicon film (not shown in the figures) is formed by a known crystallization method. Portions in which the crystalline silicon film is not necessary are removed by etching, forming island shape crystalline semiconductor films 603 to 606, and a gate insulating film 607 is further formed. The gate insulating film 607 is an oxidized silicon nitride film manufactured from SiH_4 and N_2O, and is formed to between 10 and 200 nm here, preferably from 50 to 150 nm. (See Fig. 6A.)

Resist masks 608 to 611 are next formed covering the entire surface of the island shape semiconductor layers 603 and 606, and covering the channel forming region of the island shape semiconductor layers 604 and 605. An impurity element that imparts n-type conductivity is then doped by ion doping using phosphine (PH_3), forming low impurity concentration regions. Phosphorous is doped through the gate insulating film 607 to the island shape semiconductor layers below by this process, so that the acceleration voltage is set to 65 keV. It is preferable that the concentration of phosphorous doped into the island shape semiconductors be in the range of $1x10^{16}$ to $1x10^{19}$ atoms/cm^3, and is $1x10^{18}$ atoms/cm^3 here. Regions 612 to 615 in which phosphorous is doped are thus formed. (See Fig. 6B.)

A first conductive film 616 is formed by means of sputtering from tantalum nitride (TaN) or tungsten nitride (WN). In addition, although not shown in the figures, a silicon film may be formed below the first conductive film to a thickness of 2 to 20 nm. A third conductive film 617, with a main constituent of aluminum (Al) or copper (Cu), is formed next to a thickness of between 100 and 300 nm. (See Fig. 6C.) In order to make the portion of the wiring from the input-output terminal to the input-output of the driver circuit, the third conductive film is then etched, forming a wiring 618. For example, if Al is used in the third conductive film, it can be etched by a phosphoric acid solution with good selectivity between base TaN film. Further, a second conductive film 619 is formed on the first conductive film 616 and the wiring 618 to a thickness of between 100 to 400 nm from a conductive material with its main constituent selected from Ta, Ti, Mo, and W. For example, Ta may be formed to a 200 nm thickness. (See Fig. 6D.)

Resist masks 620 to 625 are formed next, and a portion of the first conductive film and of the second conductive film are removed by etching, to thereby form a wiring 626 extending from the input-output terminal to the input-output of the driver circuit, a gate electrode 627 of the p-channel TFT, and a gate wiring 630. The etching of the TaN film and the Ta film can be performed with a mixtured gas of CF_4 and O_2. The resist masks 620 to 625 are then left as is, and a process of doping an impurity element that imparts p-type conductivity into the portion of the island shape semiconductor layer 603 on which the p-channel TFT is formed is performed. Boron is doped as the impurity element at this point by ion doping using diborane (B_2H_6). The boron concentration in this region is made $2\text{x}10^{20}$ atoms/cm^3. Thus fifth impurity regions 633 and 634, doped with a high concentration of boron, are formed as shown in Fig. 7A.

The wiring 626 from the input-output terminal to the input-output of the driver circuit is formed so that the circumference of the third conductive layer is covered with the first conductive layer and the second conductive layer.

New resist masks 635 to 640 are formed after removing the resist masks formed in Fig. 7A. This is in order to form the n-channel TFT gate electrodes, and gate electrodes 641 to 643 of the n-channel TFTs are formed by dry etching. The gate electrodes 641 and 642 are formed at this point to overlap a portion of the low concentration impurity regions 612 to 615.

Thus the gate electrodes 627 and 641 to 643 are formed from the first conductive film and the second conductive film.

New resist masks 645 to 649 are then formed. The resist masks

647 and 649 are formed to cover the gate electrodes 642 and 643 of the n-channel TFTs and a portion of the second impurity region. A process of doping an impurity element that imparts n-type conductivity and forming first impurity regions is performed. First impurity regions 650 to 655 are formed in the island shape semiconductor layers forming the n-channel TFTs. (See Fig. 7C.)

A process of doping an impurity element that imparts n-type conductivity is performed in order to form a fourth impurity region of the pixel section n-channel TFT, which becomes an LDD region, in the island shape semiconductor layer 606. It is preferable that the doped phosphorous concentration be the same level as, or less than, that of the second and third impurity regions, and it is set to 2×10^{17} atoms/cm^3 here. Fourth impurity regions 656 to 658 are formed in a self-aligning manner with the gate electrodes as a mask. (See Fig. 8A.)

A first interlayer insulating film 659 is then formed from an oxidized silicon nitride film by plasma CVD using SiH_4, N_2O, and NH_3 as raw materials. It is preferable to form this oxidized silicon nitride film so that it contains between 1 and 30 atomic% hydrogen. Heat treatment is next performed in this state in a nitrogen atmosphere at 400 to 800° C for between 1 and 12 hours, for example at 525° C for 8 hours. The doped impurity elements that impart n-type and p-type conductivities can be activated by this process. A hydrogenation process is performed after heat treatment. The hydrogenation process may be performed in a 3 to 100% hydrogen atmosphere at between 300 and 500° C, preferably from 350 to 450° C, for 2 to 12 hours. The hydrogenation process may be performed with hydrogen generated by the plasma at the substrate temperature between 200 and 500° C, preferably between 300 and 450° C. (See Fig. 8B.)

The first insulating film 659 forms a preset resist mask, and contact holes are formed through an etching process so that the contact holes reach the source regions and the drain regions of the respective TFTs. Source wirings 660, 663, 664, and 666, and drain wirings 661, 662, 665, and 657 are then formed. Although not shown in the figures, in embodiment 1 three layer structure electrodes formed by successively sputtering a 100 nm Ti film, a 300 nm Al film which contains Ti, and a 150 nm Ti film are used for these electrodes.

A passivation film 670 is then formed on top. The passivation film 670 may be an oxidized silicon nitride film formed from SiH_4, N_2O, and NH_3 by plasma CVD, or a silicon nitride film manufactured from SiH_4, N_2, and NH_3. A hydrogenation process is performed first, preceding the film formation, through plasma hydrogenation by introducing N_2O, N_2, NH_3, etc. The hydrogen generated in the gas phase by the plasma is supplied throughout the first interlayer insulating film, and provided that the substrate is heated to between 200 and 400° C, the hydrogen also diffuses to the lower layers and the semiconductor layers can be hydrogenated. There are no particular limits on the manufacturing conditions of the passivation film, but it is preferable that the film be dense. Further, a hydrogenation process may be performed after forming the passivation film by heat treatment in an atmosphere containing hydrogen or nitrogen for 1 to 12 hours at between 300 and 550° C.

A second interlayer insulating film 671 is formed next from an organic resin with a thickness of 1000 nm. Polyimide, acrylic, and polyimide amide can be used as the organic resin film. The following points can be given as the benefits of using an organic resin film: the ease of film deposition; the parasitic capacity can be reduced because the specific dielectric constant is low; and superior flatness. Note that organic resin films other than those stated above can also be used. A thermal polymerization type polyimide is used here, and after application to the substrate, it is formed by means of firing at 300° C.

If an insulating film 644 is formed on the second interlayer insulating film to a thickness of 5 to 50 nm from an oxidized silicon nitride film, silicon oxide film, etc., then the adhesion of a light shielding film formed on top of this can be raised. In addition, if the surface of the second interlayer insulating film, formed by an organic resin, is improved by processing with a CF_4 plasma, then the adhesion of films formed on top of this can be raised. An Al film is then formed by sputtering or vacuum evaporation and etched, forming a light shielding film 672. An oxide film of 50 to 200 nm formed on the surface of the light shielding film 672 is formed by anodic oxidation. In anodic oxidation, first a tartaric acid ethylene glycol solution with a sufficiently low alkaline ion concentration is prepared. The concentration of tartaric acid is between 0.1 and 10%, preferably 3%, and 1 to 20% ammonia in water is added to this, regulating the pH to 7 ± 0.5. A platinum electrode that becomes a cathode is formed in this solution, and the substrate on which the light shielding film 672 is formed is immersed in the solution. A direct current is set so that it is fixed at 2 mA, with the light shielding film 672 as an anode.

The voltage between the cathode and the anode in the solution changes with time in accordance with the growth of the oxide film, but the voltage is regulated so that the current is constant. When the voltage becomes 150 V, it is taken as fixed, and is maintained until the current is 0.1 mA. Thus an oxidized Al film 673 can be formed to a thickness of 50 to 200 nm on the surface of the light shielding film 672. Note that the values shown here related to the anodic oxidation method are only one example, and that the optimal values will naturally change with the size of the elements being manufactured, etc. A contact hole to reach the drain wiring 667 is then formed by the open sections formed in the insulating film 644, the second interlayer insulating film 671, and the passivation film 670, and a pixel electrode 676 is formed. A transparent conductive film may be used for the pixel electrode 676 for the case of a transmission type liquid crystal display device, and a metallic film may be used for the case of a reflection type liquid crystal display device. An indium tin oxide (ITO) film is formed to a thickness of 100 nm by sputtering because a transmission type liquid crystal display device is made here. The pixel electrode 676 is formed extending over the light shielding film 672 through the Al oxide film 673, and a storage capacitor 700 is formed in the region in which the pixel electrode 676 overlaps the light shielding film 672. Thus an active matrix substrate, in which a pixel section and driver circuit TFTs formed in the periphery are formed on the same substrate. (See Fig. 8C.)

A p-channel TFT 701 is formed in a self-aligning manner, and n-channel TFTs 702 to 704 are formed in a non-self-aligning manner.

A channel forming region 677 and fifth impurity regions 678 and 679 are formed in the p-channel TFT 701 of the driver circuit. The fifth impurity region 678 becomes as a source region, and the fifth impurity region 679 becomes a drain region. On the other hand, a channel forming region 680, a first impurity region 681 that becomes a source region, a first impurity region 682 that becomes a drain region, and third impurity regions 683 and 684 that become LDD regions and overlap the gate electrode through the gate insulating film, are formed in the n-channel TFT 702. This n-channel TFT is suitable for a shift register circuit or a buffer circuit. In the ne-channel TFT 703, a channel forming region 685, a first impurity region 686 that becomes a source region, a first impurity region 687 that becomes a drain region, third impurity regions 688a and 689a that become LDD regions and overlap the gate electrode through the gate insulating film, and second impurity regions 688b and 689b that become LDD regions and do not overlap the gate electrode, are formed. This kind of n-channel TFT is suitable for a sampling circuit. Channel forming regions 690 and 691, first impurity regions 692 and 696, and fourth impurity regions 693 to 695 that become LDD regions and do not overlap the gate electrode through the gate insulating film, are formed in the n-channel TFT 704 of the pixel section.

Thus as above, by optimizing the structure of the TFTs that constitute each circuit in response to the respective specifications of the pixel section and the driver circuits, the present invention can make it possible to raise the operating performance and the reliability of a semiconductor device. For example, an LDD region

(GOLD) is formed and which overlaps the gate electrode in the n-channel TFT 702 of the driver circuit. By forming this type of LDD region, fluctuation of properties due to the kink effect or the hot electron effect can be prevented, and this is suitable for a shift register, and especially for a buffer circuit. In the n-channel TFT 703, the LDD regions (GOLD) 688a and 689a are formed which overlap the gate electrode through the gate insulating film, while the LDD regions 688b and 689b are formed so as not to overlap the gate electrode, so that this is effective in the objective of reducing the off current value and preventing deterioration of the TFT due to the hot carrier effect. In the n-channel TFT of the pixel section, only LDD regions 693 to 695, which do not overlap the gate electrode, are formed, so it is effective in mainly reducing the off current value, making the switching operation reliable, along with reducing the power consumption.

[Embodiment 2]

A process of manufacturing an active matrix type liquid crystal display device from an active matrix substrate is explained in embodiment 2. As shown in Fig. 9, an alignment film 901 is formed to the state of Fig. 8C. Polyimide resin is often used in an alignment film of an ordinary liquid crystal display element. A transparent electrode 903 and an alignment film 904 are formed in an opposing side substrate 902. After formation, a rubbing process is performed to align the alignment films in parallel so that the liquid crystal molecules will possess a certain fixed pre-tilt angle. Then, the active matrix substrate on which the pixel section and the driver circuit are formed, and the opposing substrate are joined together through a sealing material or spacers (both not shown in the figures) in accordance with a known cell assembly process. A liquid crystal material 905 is next injected between both substrates, and this is completely sealed by a sealant (not shown in the figures). In addition to a TN liquid crystal, a thresholdless antiferroelectric liquid crystal, an antiferroelectric liquid crystal, etc., can be applied as the liquid crystal material. Thus the active matrix type liquid crystal display device shown in Fig. 9 is completed.

Next, the structure of this active matrix type liquid crystal display device is explained using the perspective view of Fig. 10 and the top views of Figs. 11A and 11B. Note that in order to correspond with the cross sectional structure diagrams of Figs. 6A to 8C, common reference numerals are also used in Fig. 10 and Figs. 11A and 11B. The active matrix substrate is structured by a pixel section 1001, a scanning (gate) line driver circuit 1002, and a signal (source) line driver circuit 1003 formed on the glass substrate 601. The n-channel TFT 704 is formed in the pixel section, and the driver circuits formed in the periphery are basically structured with CMOS circuits. The scanning (gate) line driver circuit 1002 and the signal (source) line driver circuit 1003 are connected to the pixel section 1001 by the gate wiring 643 and the source wiring 666, respectively. In addition, the wirings 626 and 668 are formed from an external input-output terminal 1034, connected to an FPC 1031, to the input-output terminal of the driver circuits.

Figs. 11A and 11B are top views showing a portion of the pixel section 1001. Fig. 11A is a top view showing a superposition of a semiconductor layer, a gate electrode, and a source wiring, and Fig. 11B is a top view showing the superposition of the light shielding films and the pixel electrodes formed on top. The gate electrode 643, through the gate insulating film (not shown in the figures), intersects the semiconductor layer 606 below. Although not shown in the figures, the source region, the drain region, and the fourth impurity region are formed in the semiconductor layer 606. In addition, the light shielding film 672, the dielectric film (not shown in the figures), and the pixel electrodes 676 formed for each pixel, are formed on the pixel TFTs, and the storage capacitor 700 is formed in the region where the light shielding film 672 and the pixel electrode 676 overlap through the dielectric film. It is possible to reduce the surface area to form a necessary capacitor by using a dielectric film formed in the capacitor section by oxidizing the surface of the Al film forming the light shielding film. Further, by making the light shielding film formed on the n-channel TFT of the pixel section into one electrode of the storage capacitor as in embodiment 2, the aperture ratio of the image display section of the active matrix type liquid crystal display device can be increased. Additionally, the cross sectional structure along the A-A′ shown in Figs. 11A and 11B corresponds to the cross sectional deagrams along the A-A′ of the pixel section shown in Figs. 8A to 8C.

[Embodiment 3]

Another example is shown in Figs. 12A to 12C of the constitution of the connection method for the storage capacitor formed in the pixel section TFT. Figs. 12A to 12C show cross sectional structure diagrams of the pixel section of an active matrix substrate manufactured similar to that of embodiment mode 1. Base films 1202 and 1203 are formed on a substrate 1201, and a first impurity region and a fourth impurity region are formed in an island shape semiconductor layer 1204. A gate electrode 1206 is formed on a gate insulating film 1205, and a source wiring 1208 and a drain wiring 1209 are formed on a first interlayer insulating film 1207. In addition, a light shielding film 1213 is formed on a passivation film 1211 and a second interlayer insulating film 1212.

In Fig. 12A, a storage capacitor 1240 connected to an n-channel TFT is formed from the light shielding film 1213 formed on the second interlayer insulating film 1212, a dielectric film 1214 formed on that, and a pixel electrode 1215. The pixel electrode 1215, which is one of the storage capacitor 1240 electrodes, is connected to the drain wiring 1209 by an opening 1260 formed in the passivation film 1211 and the second interlayer insulating film 1212. In addition, the light shielding film, which is the other electrode, is connected to a wiring electrode 1210 formed on the first interlayer insulating film 1207 by an opening 1261 formed in the passivation film 1211 and the second interlayer insulating film 1212. Further, in Fig. 12B, it is possible to electrostatically combine a wiring 1216, formed from the same material as the pixel electrode 1215, and the light shielding film 1213 through the dielectric film 1214 by a connection section 1251, and it is possible to connect to the wiring electrode 1210 formed on the first interlayer insulating film 1207 by the opening 1261 formed in the passivation film 1211 and the second interlayer insulting film 1212.

In addition, in Fig. 12B it is possible to electrostatically combine the light shielding film 1213 with a common electrode 1220, through the dielectric film 1214, the alignment film 1217, a liquid crystal 1218, and an allignment film 1219 on the opposing substrate side.

[Embodiment 4]

Fig. 13 shows an example of the circuit structure of the active matrix substrate shown in embodiment 1. The active matrix substrate of embodiment 4 has a source signal line side driver circuit 1301, a gate signal line side driver circuit (A) 1307, a gate signal line side driver circuit (B) 1311, a pre-charge circuit 1312, and a pixel section 1306. The source signal line side driver circuit 1301 is provided with a shift register circuit 1302, a level shifter circuit 1303, a buffer circuit 1304, and a sampling circuit 1305. In addition, the gate signal line side driver circuit (A) 1307 is provided with a shift register circuit 1308, a level shifter circuit 1309, and a buffer circuit 1310. The gate signal line side driver circuit (B) 1311 has a similar structure.

To show one example of the driver voltages for the respective circuits here, it is between 10 and 16 V for the shift register circuits 1302 and 1308, while in the level shifter circuits 1303 and 1309, the buffer circuits 1304 and 1310, the sampling circuit 1305, and the pixel section 1306, the driver voltages are from 14 to 16 V. The amplitude of the voltage applied to the sampling circuit 1305 and the pixel section 1306 is a voltage in which the polarity is normally inverted, and mutually applied. Considering the n-channel TFT driver voltage, it is easy to differ the lengths of the second impurity regions that become LDD regions on the same substrate, and optimal shapes can be built-in for the TFTs that structure the respective circuits with the present invention.

Fig. 14A shows an example of the structure of a shift register circuit TFT. An n-channel TFT of the shift register circuit is a single gate, and third impurity regions (LDD regions) 205 and 206 are formed which overlap the gate electrode. The length of this region in the longitudinal direction of the channel may be made between 0.5 and 3 μm for a channel length of 3 to 7 μm. This LDD structure is effective as a countermeasure against hot carrier degradation, and is suitable for a shift register circuit in which the off region characteristics are not very important.

Fig. 14B shows an example of the structure of a level shifter circuit and a buffer circuit TFT. An n-channel TFT for these circuits has a double gate structure, but of course a single gate structure can also be used with no problem. This n-channel TFT also has a structure in which the third impurity regions (LDD regions) 205 and 206 are formed which overlap the gate electrode. By forming this type of LDD region, the high electric field region near the drain can be eased, and fluctuations of characteristics due to the kink effect and the hot electron effect can be prevented. As a result, the reliability of a buffer circuit can be increased.

Fig. 14C shows an example of the structure of a sampling circuit TFT. The n-channel TFT of this circuit is a single gate, and second impurity regions that become LDD regions and overlap the gate electrode are formed on both the source side and the drain side. The length of the LDD regions 205 and 206 which do not overlap the gate electrode may be formed in the range of 0.5 to 3.0 μm, and both are preferably made of equal length. The objective of lowering the off current value, and the objective of preventing degradation of the TFT due to the hot carrier effect, can both be achieved at the same time by these LDD regions.

Fig. 14D is a structure suitable to a driver circuit operated at high speed by a driver voltage of approximately 1.5 to 5 V. Third impurity regions that overlap the gate electrode are not formed in a drain region 208 of the n-channel TFT, and this becomes a structure that prevents reduction of the operational frequency due to a parasitic capacity.

[Embodiment 5]

A method of manufacturing a semiconductor layer that can be applied to the present invention is explained in embodiment 5. A glass substrate, a ceramic substrate, a quartz substrate, etc., can be used as a substrate 1501 in Figs. 15A to 15C. In addition, a silicon substrate with an insulating film such as a silicon oxide film or a silicon nitride film formed on the surface, and a metallic substrate, typically stainless steel, may also be used. When a glass substrate is used, it is desirable to heat it in advance at a temperature below the softening point. For example, if a Corning Co. #1737 substrate is used, it may be heat treated at 500 to 650° C, preferably between 595 and 645° C, for 1 to 24 hours.

A base film is then formed on the main surface of the substrate 1501. There are no special limitations on the base film material, but an oxidized silicon nitride film 1502 is formed. It is also possible to form this by a single layer or a plural number of layers selected from a silicon nitride film, a silicon oxide film, an oxidized silicon nitride film, and a tantalum oxide film. When an oxidized silicon nitride film is then used, it may be formed with a thickness of between 20 and 100 nm, typically 50 nm. In addition, an oxidized silicon nitride is formed to a thickness of 50-500nm, typically 50-200nm, on a silicon nitride film of 10-100nm. An amorphous semiconductor layer 1503 is then formed on top. This may be any amorphous semiconductor formed by deposition by plasma CVD, reduced pressure CVD, sputtering, etc., and silicon (Si), germanium (Ge), a silicon and germanium alloy, silicon carbide are available, and in addition compound semiconductor materials such as gallium arsenide can be used. The semiconductor layer is formed between 10 and 100 nm in thickness, typically 50 nm. Furthermore, it is possible to form the base film 1501 and the amorphous semiconductor layer 1503 successively by plasma CVD or sputtering. By not exposing the surface to the atmosphere after forming the respective layers, the surface can be prevented from being contaminated. (See Fig. 15A.)

A crystallization process is performed next. A known laser crystallization technique or thermal crystallization technique may be used for the process of crystallizing the amorphous semiconductor layer. Furthermore, hydrogen is contained in the film at a ratio of 10 to 40 atomic% in an amorphous semiconductor layer formed by plasma CVD, and before performing crystallization, it is desirable to perform heat treatment at 400 to 500° C and desorb the hydrogen from the film so that the amount of contained hydrogen is below 5 atomic %. (See Fig. 15B.) An island shape crystalline semiconductor layer 1505 is then formed from a crystalline semiconductor layer 1504, and a gate insulating film 1505 is formed. A material such as silicon nitride film, silicon oxide film, and oxidized silicon nitride film may be used in the gate insulating film 1505. The thickness of the gate insulating film 1505 may be formed between 10 and 1000 nm, preferably from 50 to 400 nm. If further processing is performed in accordance with embodiment 1, then the semiconductor device of the present invention can be formed. (See Fig. 15C.)

A base film 1602 is formed from an oxidized silicon nitride film on the main surface of a substrate 1601 in Figs. 16A to 16E, and an amorphous semiconductor layer 1603 is formed on that surface similar to that of Figs. 15A to 15C. The amorphous semiconductor layer may be formed with a thickness of between 10 and 200 nm, preferably from 30 to 100 nm. In addition, an aqueous solution containing 10 ppm by weight of a catalytic element is applied by spin coating, forming a catalytic element containing layer 1604 on the entire surface of the amorphous semiconductor layer 1603. In addition to nickel (Ni), the catalytic elements that can be used here are germanium (Ge), iron (Fe), palladium (Pd), tin (Sn), lead (Pb), cobalt (Co), platinum (Pt), copper (Cu), and gold (Au). The internal stress of the amorphous semiconductor layer is not uniformly determined by the manufacturing conditions. However, it is necessary to perform heat treatment at between 400 and 600° C, desorbing hydrogen from the film, before the crystallization process.

(See Fig. 16A.) Heat treatment is then performed at 500 to 600° C for 4 to 12 hours, for example at 550° C for 8 hours, forming a crystalline semiconductor layer 1605. (See Fig. 16B.)

A gettering process to remove the catalytic element used in the crystallization process from the crystalline semiconductor film is performed next. The concentration of the catalytic element in the crystalline semiconductor film can be reduced below 1×10^{17} atoms/cm^3, preferably below 1×10^{16} atoms/cm^3 by this gettering process. A mask insulating film 1606 is first formed on the surface of the crystalline semiconductor layer 1605 to a thickness of 150 nm, and an open section 1607 is formed by patterning, forming an exposed region of the crystalline semiconductor layer. A phosphorous doping process is then performed, forming a phosphorous containing region 1608 in the crystalline semiconductor layer. (See Fig. 16C.) If heat treatment is performed in a nitrogen atmosphere at 550 to 800° C for 5 to 24 hours in this state, for example at 600° C for 12 hours, then the phosphorous containing region 1608 works as a gettering site, and the catalytic element remaining in the crystalline semiconductor layer 1605 can be segregated in the phosphorous containing region 1608. (See Fig. 16D.) By then removing the mask insulating film 1606 and the phosphorous containing region 1608 by etching, a crystalline semiconductor layer in which the concentration of the catalytic element used in the crystallization process is reduced to below 1×10^{17} atoms/cm^3 can be obtained. A gate insulating film 1610 is then formed adhering to an island shape semiconductor layer 1609. (See Fig. 16E.)

On the other hand, a base film 1702 and an amorphous semiconductor layer 1703 are formed in order on a substrate 1701 in Figs. 17A to 17E, and a mask insulating film 1704 is formed on the surface of the amorphous semiconductor layer 1703. The mask insulating film is made a 150 mm thick, in this case. Further, the mask insulating film 1704 is patterned, selectively forming an open section 1705, and an aqueous solution containing 10 ppm by weight of a catalytic element is applied next. Thus a catalytic element-containing layer 1706 is formed. The catalytic element-containing layer 1706 contacted the amorphous semiconductor layer 1703 only through the open section 1705. (See Fig. 17A.) Heat treatment is performed next at between 500 and 650° C for 4 to 24 hours, for example at 570° C for 14 hours, forming a crystalline semiconductor layer 1707. The region of the amorphous semiconductor layer contacting the catalytic element crystallizes first in this crystallization process, and then crystallization proceeds from there in the horizontal direction. The crystalline semiconductor layer 1707 thus formed has a gathering of cylindrical shape or needle shape crystals. Looking at each of the crystals macroscopically, they are grown with a specific directionality, so there is an advantage in that the crystals line up. (See Fig. 17B.)

A process is performed next to remove the catalytic element used in the crystallization process from the crystalline semiconductor film, similar to that of Figs. 16A to 16E. A phosphorous doping process is performed on the substrate in the same state as in Fig. 17B, forming a phosphorous containing region 1709 in the crystalline semiconductor layer. The amount of contained phosphorous in this region is between $1x10^{19}$ and $1x10^{21}$ atoms/cm^3. (See Fig. 17C.) If heat treatment is performed in a nitrogen atmosphere at 550 to 800° C for 5 to 24 hours in this state, for example at 600° C for 12 hours, then the phosphorous containing region 1709 works as a gettering site, and the catalytic element remaining in the crystalline semiconductor layer 1707 can be segregated in the phosphorous containing region 1709. (See Fig. 17D.)

By then removing the mask insulating film 1704 and the phosphorous containing region 1709 by etching, an island shape crystalline semiconductor layer 1710 is formed. A gate insulating film 1711 is then formed adhering to the crystalline semiconductor layer 1710. The gate insulating film 1711 is formed from a single layer or a plural number of layers selected from silicon oxide and oxidized silicon nitride. It may be formed with a thickness of 10 to 100 nm, preferably from 50 to 80 nm. Heat treatment is then performed in an atmosphere containing a halogen (typically chlorine) and oxygen, for example, at 950° C for 30 minutes. Note that it is good if the heat treatment temperature is selected in the range of 700 to 1100° C, and it is good if the processing time is selected between 10 minutes and 8 hours. As a result, a thermal oxidation film is formed at the interface of the island shape semiconductor layer 1710 and the gate insulating film 1711, and a good interface with a low interface level density can be formed. (See Fig. 17E.)

[Embodiment 6]

Semiconductor devices, in which an active matrix type display device is incorporated in accordance with the TFT circuits of the present invention, are explained by referring Figs. 18A to 20D in embodiment

6.

The following can be given as examples of this type of semiconductor devices: portable information terminals (such as electronic notebook mobile computers and portable telephones); video cameras; still cameras; personal computers; and televisions. Some examples of these are shown in Figs. 18A to 18F.

Fig. 18A is a portable telephone, and is composed of a main body 9001, a voice output section 9002, a voice input section 9003, a display device 9004, operation switches 9005, and an antenna 9006. The present invention can be applied to the voice output section 9002, to the voice input section 9003, and to the display device 9004 provided with an active matrix substrate.

Fig. 18B is a video camera, and is composed of a main body 9101, a display device 9102, a voice input section 9103, operation switches 9104, a battery 9105, and an image receiving section 9106. The present invention can be applied to the voice input section 9103, and to the display device 9102 provided with an active matrix substrate, and to the image receiving section 9106.

Fig. 18C is a mobile computer, and is composed of a main body 9201, a camera section 9202, an image receiving section 9203, operation switches 9204, and a display device 9205. The present invention can be applied to the image receiving section 9203 and to the display device 9205 provided with an active matrix substrate.

Fig. 18D is a head mount display, and is composed of a main body 9301, display devices 9302, and arm sections 9303. The present invention can be applied to the display device 9302. In addition, although not shown, the present invention can be used for other signal control circuits.

Fig. 18E is a rear type projector, and is composed of a main body 9401, a light source 9402, a display device 9403, a polarization beam splitter 9404, reflectors 9405 and 9406, and a screen 9407. The present invention can be applied to the display device 9403.

Fig. 18F is a portable book, and is composed of a main body 9501, display devices 9502 and 9503, a recording medium 9504, operation switches 9505, and an antenna 9506, and is for displaying data recorded on a mini-disc (MD) or DVD, or data received by antenna. The display devices 9502 and 9503 are direct viewing type display devices, and the present invention is applicable to them.

Fig. 19A is a personal computer, and is composed of a main body 2401, an image input section 2402, a display device 2403, and a keyboard 2404.

Fig 19B is a player that uses a recording medium on which a program is recorded (hereinafter referred to as a recording medium), and is composed of a main body 2413, a display device 2414, a speaker section 2415, a recording medium 2416, and operation switches 2417. Note that music appreciation, film appreciation, games, and the use of the Internet can be performed with this device using a DVD (digital versatile disk), a CD, etc., as a recording medium. The present invention can be applied to the display device 2414, and to other signal control circuits.

Fig. 19C is a digital camera, and is composed of a main body 2418, a display device 2419, a viewfinder 2420, operation switches 2421, and an image receiving section (not shown in the figure). The present invention can be applied to the display device 2419 and to other signal control circuits.

Fig. 20A is a front type projector, and is composed of a projector device 2601 and a screen 2602. The present invention can be applied to the projector device 2601 and to other signal control circuits.

Fig. 20B is a rear type projector, and is composed of a main body 2701, a projector device 2702, a mirror 2703, and a screen 2704. The present invention can be applied to the projector device 2702 (it is especially effective for 50 to 100 inch cases), and to other signal control circuits.

Note that Fig. 20C is a drawing showing one example of the structure of the projector devices 2601 and 2702 from Figs. 20A and 20B. The projector devices 2601 and 2702 comprises an optical light source system 2801, mirrors 2802 and 2805 to 2807, dichroic mirrors 2803 and 2804, optical lenses 2808 and 2809, a prism 2811, a display device 2810, and an optical projection system 2812. The optical projection system 2812 is composed of an optical system provided with a projection lens. Embodiment 6 shows an example in which the liquid crystal display device 2810 is triple stage using three lenses, but there are no special limits and a single stage is acceptable, for example. Further, the operator may set optical systems such as optical lenses, film having polarizing function, film to regulate the phase difference, IR films, etc., suitably within the optical path shown by an arrow in

Fig. 20C.

In addition, Fig. 20D shows one example of the structure of the optical light source system 2801 from Fig. 20C. In embodiment 6, the optical light source system 2801 is composed of light sources 2813 and 2814, a compound prism 2815, collimator lenses 2816 and 2820, lens arrays 2817 and 2818, and a polarizing conversion element 2819. Note that the optical light source system shown in Fig. 20D uses two light sources, but three, four, or more light sources, may be used. Of course a single light source is acceptable. Further, the operator may place optical lenses, film having polarizing function, film to regulate the phase difference, IR films, etc., suitably in the optical light source system.

In addition, although not shown in the figures, it is possible to apply the present invention to image sensors and EL type display devices. Thus the applicable range of the present invention is extremely wide, and it is possible to apply the present invention to electronic equipment in all fields.

Furthermore, although not shown in the figures, it is possible to apply the present invention to the display sections of car navigation systems, image sensors, and personal computers. Thus the applicable range of the present invention is extremely wide, and it is possible to apply the present invention to electronic equipment in all fields.

[Embodiment 7]

An explanation of the example of the manufacture of an active matrix type EL (electro-luminescence) display device using the present invention is given in embodiment 7.

Fig. 21A is a top view of an EL display device using the present invention. In Fig. 21A, reference numeral 4010 denotes a substrate, 4011 denotes a pixel section, 4012 denotes a source side driver circuit, and 4013 denotes a gate side driver circuit. Both drive circuits lead to an FPC 4017 through wirings 4014 to 4016, and thus connect to external equipment.

A cover 6000, a sealing material (also called a housing material) 7000, and a sealant (a second sealing material) 7001 are formed so as to surround at least the pixel section, and preferably both the pixel section and the driver circuits at this point.

Fig. 21B is the cross sectional structure of the EL display device of embodiment 8. A driver circuit TFT (a CMOS circuit combining an n-channel TFT and a p-channel TFT is shown here) 4022 and a pixel section TFT 4023 (the only TFT that controls the current to the EL element is shown here.) are formed on the substrate 4010 and a base film 4021.

The present invention can be used for the driver circuit TFT 4022 and for the pixel section TFT 4023.

After completing the driver circuit TFT 4022 and the pixel section TFT 4023 using the present invention, a pixel electrode 4027 is formed by a transparent conductive film, on an interlayer insulating film (a flattening film) 4026 made of resin material, in order to electrically connect to the drain of the pixel section TFT 4023. When the pixel electrode 4027 is formed by a transparent conductive film, the p-channel TFT is preferably used for the pixel section TFT. An indium oxide and tin oxide compound (called ITO), or an indium oxide and zinc oxide compound can be used as the transparent conductive film. Then, after forming the pixel electrode 4027, an insulating film 4028 is formed, and an open section is formed on the pixel electrode 4027.

An EL layer 4029 is formed next. Any known EL materials (hole injection layer, hole transport layer, illumination layer, electron transport layer, electron injection layer) may be freely combined and used in a laminate structure or a single layer structure. A known technique may be used to determine the structure type. Further, there are low molecular materials and high molecular materials (polymers) as EL materials. An evaporation method is used for low molecular materials, but it is possible to use an easy method such as spin coating, printing, or injecting for high molecular materials.

The EL layer is formed in embodiment 7 by an evaporation method using a shadow mask. By using a shadow mask and forming a luminescence layer that can emit different wavelengths of light for each pixel (red light emitting layer, green light emitting layer, and blue light emitting layer), color display is possible. Any other form may be used, such as combining color changing layers (CCM) with color filters, and combining white light emitting layers with color filters. Of course a single color emitting EL display device is also possible.

After forming the EL layer 4029, a cathode 4030 is formed on top. It is preferable to remove as much as possible of the moisture and oxygen existing in the interface between the cathode 4030 and the EL layer 4029. Therefore, it is necessary to form the EL layer 4029 and the cathode 4030 inside a vacuum by successive film deposition, or to form the EL layer 4029 in an inert atmosphere and then form the cathode 4030 without exposure to the atmosphere. It is possible to perform the above film deposition in embodiment 7 by using a multi-chamber system (cluster tool system) deposition device.

Note that a laminate structure of a LiF (lithium fluoride) film and an Al (aluminum) film is used for the cathode 4030 in embodiment 7. Specifically, a 1 nm thick LiF (lithium fluoride) film is formed on the EL layer 4029 by evaporation, and a 300 nm thick aluminum film is formed on top of that. Of course an MgAg electrode, a known cathode material, may be used. Then the cathode 4030 is connected to the wiring 4016 in the region denoted with the reference numeral 4031. The wiring 4016 is a power supply line in order to apply a preset voltage to the cathode 4030, and is connected to the FPC 4017 through a conductive paste material 4032.

The region denoted by reference numeral 4031 electrically connects the cathode 4030 and the wiring 4016, so it is necessary to form contact holes in the interlayer insulating film 4026 and the insulating film 4028. The contact holes may be formed during etching of the interlayer insulating film 4026 (when forming the pixel electrode contact hole) and during etching of the insulating film 4028 (when forming the open section before forming the EL layer). Further, etching may proceed in one shot all the way to the interlayer insulating film 4026 when etching the insulating film 4028. In this case the contact holes can have a good shape provided that the interlayer insulating film 4026 and the insulating film 4028 are the same resin material.

A passivation film 6003, a filler 6004, and a cover 6000 are formed, covering the surface of the EL element thus formed.

In addition, a sealing material is formed on the inside of the cover 6000 and the substrate 4010, so as to surround the EL element section, and the sealant 7001 (the second sealing material) is formed on the outside of the sealing material 7000.

At this point the filler 6004 also functions as an adhesive in order to bond the cover 6000. PVC (polyvinyl chloride), epoxy resin, silicone resin, PVB (polyvinyl butyral), or EVA (ethylene vinyl acetate) can be used as the filler 6004. If a drying agent is formed on the inside of the filler 6004, a moisture absorption effect can be maintained, so this is preferable.

Further, spacers may be included within the filler 6004. The spacers may be of a powdered substance such as BaO, etc., giving the spacers themselves the ability to absorb moisture.

When using spacers, the passivation film 6003 can relieve the spacer pressure. Further, a resin film, etc., can be formed separately from the passivation film 6003 to relieve the spacer pressure.

In addition, a glass plate, an aluminum plate, a stainless steel plate, an FRP (fiberglass-reinforced plastic) plate, a PVF (polyvinyl fluoride) film, a Mylar film, a polyester film, or an acrylic film can be used as the cover 6000. Note that if PVB or EVA is used as the filler 6004, it is preferable to use a sheet with a structure in which several tens of μm of aluminum foil is sandwiched by a PVF film or a Mylar film.

However, depending upon the light emission direction from the EL element (the light radiation direction), it is necessary for the cover 6000 to have light transmitting characteristics.

In addition, the wiring 4016 is electrically connected to the FPC 4017 through the opening among the sealing material 7000, the sealant 7001 and the substrate 4010. Note that an explanation of the wiring 4016 has been made, and the wirings 4014 and 4015 are also connected electrically to the FPC 4017 by similarly passing underneath the sealing material 7000 the sealant 7001.

Figs. 22A and 22B are used in embodiment 7 to explain an example of the manufacture of an EL display device with a different form. Reference numerals that are the same as in Figs. 21A and 21B indicate the same sections, and therefore their explanation is omitted.

Fig. 22A is a top view of the EL display device of embodiment 9, and a cross sectional diagram taken along the line of A-A′ in Fig. 22A is shown in Fig. 22B.

Processing is performed similar to that shown in Figs. 21A and 21B, through the formation of the passivation film 6003 covering the surface of the EL element.

In addition, the filler 6004 is formed, covering the EL element. The filler 6004 also functions as an adhesive in order to bond to the cover 6000. PVC (polyvinyl chloride), epoxy resin, silicone resin, PVB (polyvinyl butyral), or EVA (ethylene vinyl acetate) can be used as the filler 6004. If a drying agent is formed on the inside of the filler 6004, a moisture absorption effect can be maintained, so this is preferable.

Further, spacers may be included within the filler 6004. The spacers may be of a powdered substance such as BaO, etc., giving the spacers themselves the ability to absorb moisture.

When using spacers, the passivation film 6003 can relieve the spacer pressure. Further, a resin film, etc., can be formed separately from the passivation film 6003 to relieve the spacer pressure.

In addition, a glass plate, an aluminum plate, a stainless steel plate, an FRP (fiberglass-reinforced plastic) plate, a PVF (polyvinyl fluoride) film, a Mylar film, a polyester film, or an acrylic film can be used as the cover 6000. Note that if PVB or EVA is used as the filler 6004, it is preferable to use a sheet with a structure in which several tens of μm of aluminum foil is sandwiched by a PVF film or a Mylar film.

However, depending upon the light emission direction from the EL element (the light radiation direction), it is necessary for the cover 6000 to have light transmitting characteristics.

A frame 6001 is attached so as to cover the side face (the exposed face) of the filler 6004 after bonding the cover 6000 using the filler 6004. The frame 6001 is bonded by a sealing material (functioning as an adhesive) 6002. It is preferable to use a light curing resin as the sealing material 6002 at this point, but if the heat resistance characteristics of the EL layer permit, then a thermal curing resin may also be used. Note that it is preferable that the sealing material 6002 be a material that is as impermeable as possible to water and oxygen. Further, a drying agent may be added on the inside of the sealing material 6002.

In addition, the wiring 4016 is electrically connected to the

FPC 4017 through the opening between the sealing material 6002 and the substrate 4010. Note that an explanation of the wiring 4016 has been made, and the wirings 4014 and 4015 are also connected electrically to the FPC 4017 by similarly passing underneath the sealing material 6002.

A detailed cross sectional structure of a pixel section is shown in Fig. 23, a upper surface structure is shown in Fig. 24A, and a circuit diagram is shown in Fig. 24B for the EL display device. Common reference numerals are used in Figs. 23, 24A, and 24B, so they may be mutually referenced.

In Fig. 23, a switching TFT 3002 is formed on a substrate 3001 using an n-channel TFT formed by using the present invention. (Refer to embodiments 1 to 7.) A double gate structure is used in embodiment 7, but there are no large differences in structure and manufacturing processes, so that explanation is omitted. However, by using a double gate structure, in essence the structure is two TFTs in series, which has the advantage that the off current value can be lowered. Note that although embodiment 7 has a double gate structure, a single gate structure may also be used, as may a triple gate structure or a multiple gate structure having a larger number of gates.

In addition, a current control TFT 3003 is formed using an n-channel TFT of the present invention. At this point a drain wiring 3035 of the switching TFT 3002 is electrically connected to a gate electrode 3037 of the current control TFT by a wiring 3036. Further, the wiring denoted by reference numeral 3038 is a gate wiring that electrically connects gate electrodes 3039a and 3039b on the switching

TFT 3002.

The fact that the current control TFT 3003 has the structure of the present invention has an extremely important meaning at this point. A current control TFT is an element for controlling the amount of current flowing in an EL element, and there is much current flow, so it is an element in which there is a great danger of degradation due to heat or due to hot carriers. Therefore, the structure of the present invention, in which a GOLD region (second impurity region) is formed to overlap a gate electrode through a gate insulating, is extremely effective on the drain side of the current control TFT.

Additionally, a single gate structure is shown in the figures for the current control TFT 3003 in embodiment 7, but a multiple-gate structure, with a plural number of TFTs connected in series, may also be used. Further, a structure so as to perform heat radiation with a high efficiency, in which a plural number of TFTs are connected in parallel, in essence dividing the channel forming region into a plural number of channel forming regions, may also be used. This type of structure is an effective countermeasure to heat degradation.

As shown in Fig. 24A, the wiring that becomes the gate electrode 3037 of the current control TFT 3000 overlaps a drain wiring 3040 on the current control TFT 3003, through an insulating film in the region shown by reference numeral 3004. At this point a capacitor is formed in the region shown by reference numeral 3004. The capacitor 3004 functions as a capacitor in order to store the voltage applied to the gate on the current control TFT 3003. Note that the drain wiring 3040 is connected to a current supply line (power supply line) 3006, and a fixed voltage is always applied.

A first passivation film 3041 is formed over the switching TFT 3002 and the current control TFT 3003, and a flattening film 3042 is formed on top of that by an insulating resin film. It is very important to flatten the step due to the TFTs using the flattening film 3042. An EL layer formed later is extremely thin, so that there are cases that cause the luminescence to be defective due to the existence of the step. Therefore, to form the EL layer with as level a surface as possible, it is preferable to perform flattening before forming a pixel electrode.

The reference numeral 3043 denotes a pixel electrode (EL element cathode) from a conductive film with high reflectivity, and is electrically connected to the drain of the current control TFT 3003. In this case it is preferable to use an n-channel TFT as the current control TFT. It is preferable to use a low resistance conductive film, such as an aluminum alloy film, a copper alloy film, or a silver alloy film, etc., or a laminate of such films. Of course, a laminate structure with other conductive films may be used.

Furthermore, a luminescence layer 3045 is formed in the middle of the groove (corresponding to the pixel) formed by banks 3044a and 3044b formed by insulating films (preferably resins). Note that only one pixel is shown in the figures here, but the luminescence layer may be divided to correspond to each of the colors R (red), G (green), and B (blue). A π-conjugate polymer material is used as an organic EL material that is the luminescence layer. Polyparaphenylene vinylenes (PPVs), polyvinyl carbazoles (PVCs), and polyfluoranes can be given as typical polymer materials.

Note that there are several types of PPV organic EL materials, and materials described in Shenk, H., Becker, H., Gelsen, O., Kluge, E., Kreuder, W., and Spreitzer, H., Polymers for Light Emitting Diodes, Euro Display Proceedings, 1999, p. 33-7, and in Japanese Patent Application Laid-Open No. Hei 10-92576, for example, may be used.

As specific luminescence layers, cyano-polyphenylene vinylene may be used as a red light emitting luminescence layer, polyphenylene vinylene may be used as a blue light radiating luminescence layer, and polyphenylene vinylene or polyalkylphenylene may be used as a blue light radiating luminescence layer. The film thicknesses may be between 30 and 150 nm (preferably between 40 and 100 nm).

However, the above example is one example of the organic EL materials that can be used as luminescence layers, and it is not necessary to limit use to these materials. An EL layer (a layer for luminescence and for performing carrier motion for luminescence) may be formed by freely combining luminescence layers, charge transport layers, or charge injection layers.

For example, an example using polymer materials as luminescence layers is shown in embodiment 7, but low molecular organic EL materials may also be used. Further, it is possible to use inorganic materials such as silicon carbide, etc., as charge transport layers and charge injection layers. Known materials can be used for these organic EL materials and inorganic materials.

A laminate structure EL layer, in which a hole injection layer

3046 from PEDOT (polythiophene) or PAni (polyaniline) is formed on the luminescence layer 3045, is used in embodiment 7. An anode 3047 is then formed on the hole-injection layer 3046 from a transparent conductive film. The light generated by the luminescence layer 3045 is radiated toward the upper surface (toward the top of the TFT) in the case of embodiment 7, so the anode must have light transmitting characteristics. An indium oxide and tin oxide compound, or an indium oxide and zinc oxide compound can be used for the transparent conductive film. However, because it is formed after forming the low heat resistance luminescence layer and hole injection layer, it is preferable to use a material that can be deposited at as low a temperature as possible.

At the point where the anode 3047 is formed, an EL element 3005 is completed. Note that what is called the EL element 3005 here indicates the capacitor formed by the pixel electrode (cathode) 3043, the luminescence layer 3045, the hole-injection layer 3046, and the anode 3047. As shown in Fig. 24A, the pixel electrode 3043 nearly matches the area of the pixel, so the entire pixel functions as an EL element. Therefore, the luminescence usage efficiency is very high, and a bright image display is possible.

A second passivation film 3048 is then formed in addition on the anode 3047 in embodiment 7. It is preferable to use a silicon nitride film or an oxidized silicon nitride film as the second passivation film 3048. The purpose of this is the isolation of the EL element and the outside, and has meaning in preventing degradation due to the oxidation of the organic EL material, and in controlling gaseous emitted from the organic EL material. Thus the reliability of an EL display device can be raised.

Thus the EL display panel of the present invention 7 has a pixel section from pixels structured as in Fig. 23, and has a switching TFT with sufficiently low off current value, and a current control TFT with strong hot carrier injection. Therefore, an EL display panel that has high reliability, and in which good image display is possible, can be obtained.

Note that it is possible to implement the constitution of Fig. 23 by freely combining it with the constitutions of embodiment mode 1 and embodiments 1 to 4. Note that it is effective to use the EL display device of embodiment 7 as the display section of the electronic equipment of embodiment 6.

Next, a structure in which the structure of the EL element 3005 is inverted is explained as another constitution of the pixel section. Fig. 25 is used in the explanation. Note that the only points that differ from the structure of Fig. 23 are the EL element section and the current control TFT, so other explanations are omitted.

The p-channel TFT of the present invention is used for the current control TFT 3103 in Fig. 25. Embodiment mode 1 and embodiments 1 to 4 may be referred to for the manufacturing process.

A transparent conductive film is used as a pixel electrode (anode) 3050 in Fig. 25. Specifically, an indium oxide and zinc oxide compound conductive film is used. Of course, an indium oxide and tin oxide compound conductive film may also be used.

Then, after forming banks 3051a and 3051b from insulating films, a luminescence layer 3052 is formed from polyvinyl carbazole by solution coating. An electron injection layer 3053 is formed on top from potassium acetylacetonate (denoted acacK), and a cathode 3054 is formed from an aluminum alloy. In this case the cathode 3054 also functions as a passivation film. Thus an EL element 3101 is formed.

The light generated by the luminescence layer 3052 is radiated toward the substrate on which the TFT is formed, as shown by the arrows.

Note that it is possible to implement the constitution of Fig. 25 by freely combining it with the constitutions of embodiment mode 1 and embodiments 1 to 4. In addition, it is effective to use the EL display panel of embodiment 7 as the display section of the electronic equipment of embodiment 6.

An example of a case of a pixel with a different structure from that of the circuit diagram of Fig. 24B is shown in Figs. 26A to 26C. Note that in embodiment 7, reference numeral 3201 denotes a source wiring of a switching TFT 3202, 3203 denotes a gate wiring of the switching TFT 3202, 3204 denotes a current control TFT, 3205 denotes a capacitor, 3206 and 3208 denote current supply lines, and 3207 denotes an EL element.

Fig. 26A is an example of a case in which the current supply line 3206 is shared between two pixels. Namely, this is characterized in that two pixels are formed having linear symmetry around the current supply line 3206. In this case the number of power supply lines can be reduced, so the pixel section can be made higher definition.

Fig. 26B is an example of a case in which the current supply line 3208 is formed parallel to the gate wiring 3203. Note that Fig. 26B has a structure in which the current supply line 3208 and the gate wiring 3203 are formed so as not to overlap, but if both are wirings formed on different layers, then they can be formed to overlap through an insulating film. In this case, the area used exclusively by the current supply line 3208 and the gate wiring 3203 can be shared, so the pixel section can be made higher definition.

Furthermore, Fig. 26C is characterized in that the current supply line 3208 is formed parallel to gate wirings 3203a, 3203b, similar to the structure of Fig. 26B, and in addition, two pixels are formed to have linear symmetry around the current supply line 3208. It is also effective to form the current supply line 3208 to overlap one gate wiring 3203a or 3203b. In this case the number of power supply lines can be reduced, so the pixel section can be made higher definition.

Note that it is possible to implement the constitution of the circuit shown in Figs. 26A to 26C by freely combining with the constitutions of embodiment mode 1 and embodiments 1 to 4. In addition, it is effective to use an EL display device having the pixel structure of embodiment 7 as the display section of the electronic equipment of embodiment 6.

A structure in which a capacitor 3004 is formed in order to store the voltage applied to the current control TFT 3003 gate is used in Figs. 24A and 24B, but it is possible to omit the capacitor 3004. An n-channel TFT of the present invention as shown in embodiments 1 to 7 is used as the current control TFT 3003, so it has a GOLD region (second impurity region) formed so as to overlap the gate electrode through a gate insulating film. A parasitic capacitor, generally called a gate capacitor, is formed in the overlapping region, and embodiment 7 is characterized in that the parasitic capacitor is actively used as a substitute for the capacitor 3004.

The capacitance of the parasitic capacitor changes in accordance with the area of the overlap between the gate electrode and the GOLD region, so the length of the GOLD region in the overlapping region determines the capacitance.

Furthermore, it is possible to similarly omit the capacitor 3205 in the structures of Figs. 26A, 26B, and 26C.

Note that it is possible to implement this kind of constitution by freely combining it with the constitutions of embodiment mode 1 and embodiments 1 to 4. In addition, it is effective to use an EL display device having the pixel structure of embodiment 7 as the display section of the electronic equipment of embodiment 6.

[Embodiment 8]

Fig. 27 is a result of bias-temperature (B-T) examination to show an example of characteristic of n-channel TFT fabricated according to the description of Embodiment 1. The TFT structure shown in Fig. 27 has a channel length 8μm, L_{ov}=2.5μm and L_{off} is not disposed. In the B-T examination, bias of 20V was inputted to the gate electrode and that was kept for an hour. Then the bias was broken, and heat treatment was carried out for an hour. Fig. 27 shows the result by characteristic of gate voltage (VG) versus drain current (ID) in cases of drain voltage

(Vd) 1V and 5V. Due to the structure having LDD region that overlap the gate electrode, deterioration by hot carrier effect was prevented and further difference in the characteristic due to the bias stress was not observed. Also, by forming the base film in double layered structure comprising an oxidized silicon nitride (100nm) made of SiH_4, NH_3 and N_2O and an oxidized silicon nitride (200nm) made of SiH_4 and N_2O, avoiding an effect from a movable ion included in the substrate became possible, and difference in threshold voltage was not observed in the B-T examination.

Figs. 28A and 28B show dynamic characteristic (source voltage 10V) of a ring oscillator fabricated by using such TFTs. The ring oscillator has 19 stages. Fig. 28A shows a difference in oscillation frequency by channel length when $L_{ov}=2\mu m$, with a parameter of activation condition of the doped impurity element. The oscillation frequency decreases with the increase in channel length however it is not dependent upon activation condition. When a LDD structure overlapping with a gate electrode is disposed, decrease in operation frequency by increase in parasitic capacitor of that section should be feared. However, it turned out that there is no practical problem because oscillation of frequency at 8-12 MHz was available although dependence on L_{ov} length was observed upon differentiating the value of L_{ov} for 1-3 μm with channel length 6 μm, as shown in Fig. 28B.

As such, a TFT having oxidized silicon nitride as a base film and an LDD structure overlapping a gate electrode has a good resistance against stress due to bias or heat, and there is no deterioration by hot carrier effect. Further, because it is possible to operate them by high frequency, they are especially superior for forming a shift register circuit or a buffer circuit of the driver circuit.

In accordance with the present invention, a third impurity region that overlaps a gate electrode, and a second impurity region and a fourth impurity region which do not overlap the gate electrode, are formed as the LDD regions between a channel forming region and a drain region of an n-channel TFT, and N-channel TFTs with optimized structures corresponding to the different operating characteristics can be formed on the same substrate. For example, taking a CMOS circuit which is formed on an active matrix substrate as a base, n-channel TFTs in which a third impurity region is formed which overlaps a gate electrode, can be formed for the surrounding driver circuits, and an n-channel TFT of a pixel section with a structure in which a fourth impurity region is formed which does not overlap a gate electrode, can be made.

A storage capacitor formed in the pixel section is formed of a light shielding film, a dielectric film formed on the light shielding film, and a pixel electrode. Al is especially used in the light shielding film, and the dielectric film is formed by anodic oxidation process. By using an Al oxide film, it is possible to reduce the surface area in order to form the capacity required for an image display. In addition, by using the light shielding film formed on the pixel TFT as one electrode of the storage capacitor, the aperture ratio of the image display section of an active matrix type liquid crystal display device can be increased.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising a driver circuit and a pixel section comprising thin film transistors over a substrate, wherein:

a) said driver circuit includes:

a first thin film transistor comprising:

a channel forming region and a third impurity region having a conductivity type, formed on the inside of a gate electrode; and

a first impurity region having said conductivity type which forms a source region or a drain region, formed on the outside of the gate electrode; and

a fifth thin film transistor comprising:

a channel forming region, and a fifth impurity region which forms a source region or a drain region having inverse conductivity type to said conductivity type; and

b) said pixel section comprises:

a fourth thin film transistor comprising:

a channel forming region formed on the inside of a gate electrode; and

a fourth impurity region having said conductivity type, and a first impurity region having said conductivity type which forms a source region or a drain region, formed on the outside of the gate electrode.

2. A semiconductor device according to claim 1, wherein:

an impurity element having said conductivity type is included in the third impurity region and in the fourth impurity region; and

a concentration of the impurity element included in said fourth impurity region is less than a concentration of the impurity element included in said third impurity region.

3. A semiconductor device according to claim 1, wherein:

said pixel section comprises:

a light shielding film formed on said fourth thin film transistor interposing an insulating layer therebetween;

a pixel electrode connected to said fourth thin film transistor; and

a storage capacitor comprising said light shielding film, said insulating layer contacting said light shielding film, and the pixel electrode contacting the insulating layer,

wherein said storage capacitor is connected to said fourth thin film transistor.

4. A semiconductor device according to claim 3, wherein:

said light shielding film comprises an element selected from a group consisting of aluminum, tantalum, and titanium; and

said insulating layer comprises an oxide of said element of the light shielding film.

5. A semiconductor device according to claim 3, wherein said insulating layer comprises a material selected from silicon nitride, silicon oxide, oxidized silicon nitride, diamond-like carbon (DLC), and polyimide.

6. A semiconductor device according to claim 3, wherein:

said insulating layer comprises an inorganic insulating film and an organic insulating film; and

said light shielding film is formed contacting the organic insulating film.

7. A semiconductor device according to claim 3, wherein:

said insulating layer comrises an inorganic insulating film and an organic insulating film; and

said light shielding film is formed contacting the inorganic insulating film.

8. A semiconductor device according to claim 1 wherein said semiconductor device is one selected from a group consisting of: a portable telephone, a video camera, a mobile computer, a head mount display, a projector, a portable book, a digital camera, a car navigation system, and a personal computer.

9. A semiconductor device comprising a driver circuit and a pixel section comprising thin film transistors over a substrate, wherein:

a) said driver circuit comprises:

a first thin film transistor comprising:

a channel forming region and a third impurity region having a conductivity type, formed on the inside of a gate electrode; and

a first impurity region having said conductivity type which forms a source region or a drain region, formed on the outside of the gate electrode;

a second thin film transistor comprising:

a channel forming region and a third impurity region having said conductivity type, formed on the inside of a gate electrode; and

a second impurity region having said conductivity type, and a first impurity region having said conductivity type which forms a source region or a drain region, formed on the outside of the gate electrode; and

a fifth thin film transistor comprising:

a channel forming region, and a fifth impurity region which forms a source region or a drain region having an inverse conductivity type to said conductivity type; and

b) said pixel section comprises:

a fourth thin film transistor having:

a channel forming region formed on the inside of a gate electrode; and

a fourth impurity region having said conductivity type, and a first impurity region which forms a source region or a drain region having said conductivity type, formed on the outside of the gate electrode.

10. A semiconductor device according to claim 2, wherein:

an impurity element having said conductivity type is included in the third impurity region and in the fourth impurity region; and

a concentration of the impurity element included in said fourth impurity region is less than a concentration of the impurity element included in said third impurity region.

11. A semiconductor device according to claim 9, wherein:

an impurity element having said conductivity type is included in the second impurity region and in the third impurity region; and

a concentration of the impurity element included in said second impurity region is the same as a concentration of the impurity element included in said third impurity region.

12. A semiconductor device according to claim 9, wherein said pixel section further comprises:

a light shielding film formed on said fourth thin film transistor interposing an insulating layer therebetween;

a pixel electrode connected to said fourth thin film transistor; and

a storage capacitor comprising said light shielding film, said insulating layer contacting said light shielding film, and the pixel electrode contacting the insulating layer,

wherein said storage capacitor is connected to said fourth thin film transistor.

13. A semiconductor device according to claim 12, wherein:

said light shielding film comprises an element selected from a group consisting of aluminum, tantalum, and titanium; and

said insulating layer comprises an oxide of said element of the light shielding film.

14. A semiconductor device according to claim 12, wherein said insulating layer comprises a material selected from silicon nitride, silicon oxide, oxidized silicon nitride, diamond-like carbon (DLC), and polyimide.

15. A semiconductor device according to claim 12, wherein:

said insulating layer comprises an inorganic insulating film and an organic insulating film; and

said light shielding film is formed contacting the organic insulating film.

16. A semiconductor device according to claim 12, wherein:

said insulating layer comrises an inorganic insulating film and an organic insulating film; and

said light shielding film is formed contacting the inorganic insulating film.

17. A semiconductor device according to claim 9 wherein said semiconductor device is one selected from a group consisting of: a portable telephone, a video camera, a mobile computer, a head mount display, a projector, a portable book, a digital camera, a car navigation system, and a personal computer.

18. A semiconductor device comprising a driver circuit and a pixel section comprising thin film transistors over a substrate, wherein:

a) said driver circuit comprises:

a first thin film transistor comprising:

a channel forming region and a third impurity region having a conductivity type, formed on the inside of a gate electrode;

and

a first impurity region having said conductivity type which forms a source region or a drain region, formed on the outside of the gate electrode;

a third thin film transistor comprising:

a channel forming region formed on the inside of a gate electrode; and

a second impurity region having said conductivity type, and a first impurity region having said conductivity type which forms a source region or a drain region, formed on the outside of the gate electrode; and

a fifth thin film transistor comprising:

a channel forming region, and a fifth impurity region which forms a source region or a drain region having an inverse conductivity type to said conductivity type; and

b) said pixel section comprises:

a fourth thin film transistor comprising:

a channel forming region formed on the inside of a gate electrode; and

a fourth impurity region having said conductivity type, and a first impurity region which forms a source region or a drain region having said conductivity type, formed on the outside of the gate electrode.

19. A semiconductor device according to claim 18, wherein:

an impurity element having said conductivity type is included in the third impurity region and in the fourth impurity region; and

a concentration of the impurity element included in said fourth impurity region is less than a concentration of the impurity element included in said third impurity region.

20. A semiconductor device according to claim 18, wherein:

an impurity element having said conductivity type is included in the second impurity region and in the third impurity region; and

a concentration of the impurity element included in said second impurity region is the same as a concentration of the impurity element included in said third impurity region.

21. A semiconductor device according to claim 18, wherein said pixel section further comprises:

a light shielding film formed on said fourth thin film transistor interposing an insulating layer therebetween;

a pixel electrode connected to said fourth thin film transistor; and

a storage capacitor comprising said light shielding film, said insulating layer contacting said light shielding film, and the pixel electrode contacting the insulating layer,

wherein said storage capacitor is connected to said fourth thin film transistor.

22. A semiconductor device according to claim 21, wherein:

said light shielding film comprises an element selected from a group consisting of aluminum, tantalum, and titanium; and

said insulating layer comprises an oxide of said element of the light shielding film.

23. A semiconductor device according to claim 21, wherein said insulating layer comprises a material selected from silicon nitride, silicon oxide, oxidized silicon nitride, diamond-like carbon (DLC), and polyimide.

24. A semiconductor device according to claim 21, wherein:

said insulating layer comprises an inorganic insulating film and an organic insulating film; and

said light shielding film is formed contacting the organic insulating film.

25. A semiconductor device according to claim 21, wherein:

said insulating layer comrises an inorganic insulating film and an organic insulating film; and

said light shielding film is formed contacting the inorganic insulating film.

26. A semiconductor device according to claim 18 wherein said semiconductor device is one selected from a group consisting of: a portable telephone, a video camera, a mobile computer, a head mount display, a projector, a portable book, a digital camera, a car navigation system, and a personal computer.

27. A semiconductor device comprising a driver circuit and a pixel section comprising thin film transistors over a substrate, wherein:

a) said driver circuit comprises:

a first thin film transistor comprising:

a channel forming region and a third impurity region having a conductivity type, formed on the inside of a gate electrode; and

a first impurity region having said conductivity type which forms a source region or a drain region, formed on the outside of the gate electrode;

a second thin film transistor comprising:

a channel forming region and the third impurity region having said conductivity type, formed on the inside of a gate electrode; and

a second impurity region having said conductivity type, and a first impurity region which forms a source region or a drain region having said conductivity type, formed on the outside of the gate electrode;

a third thin film transistor comprising:

a channel forming region formed on the inside of a gate electrode; and

a second impurity region having said conductivity type, and a first impurity region which forms a source region or a drain region having said conductivity type, formed on the outside of the gate electrode; and

a fifth thin film transistor comprising:

a channel forming region, and a fifth impurity region which forms a source region or a drain region having an inverse conductivity type to said conductivity type; and

b) said pixel section comprises:

a fourth thin film transistor comprising:

a channel forming region formed on the inside of a gate electrode; and

a fourth impurity region having said conductivity type, and a first impurity region which forms a source region or a drain region having said conductivity type, formed on the outside of the gate electrode.

28. A semiconductor device according to claim 27, wherein:

an impurity element having said conductivity type is included in the third impurity region and in the fourth impurity region; and

a concentration of the impurity element included in said fourth impurity region is less than a concentration of the impurity element included in said third impurity region.

29. A semiconductor device according to claim 27, wherein:

an impurity element having said conductivity type is included in the second impurity region and in the third impurity region; and

a concentration of the impurity element included in said second impurity region is the same as a concentration of the impurity element included in said third impurity region.

30. A semiconductor device according to claim 27, wherein said pixel section further comprises:

a light shielding film formed on said fourth thin film transistor interposing an insulating layer therebetween;

a pixel electrode connected to said fourth thin film transistor; and

a storage capacitor comprising said light shielding film, said insulating layer contacting said light shielding film, and the pixel electrode contacting the insulating layer,

wherein said storage capacitor is connected to said fourth thin film transistor.

31. A semiconductor device according to claim 30, wherein:

said light shielding film comprises an element selected from a group consisting of aluminum, tantalum, and titanium; and

said insulating layer comprises an oxide of said element of the light shielding film.

32. A semiconductor device according to claim 30, wherein said insulating layer comprises a material selected from silicon nitride, silicon oxide, oxidized silicon nitride, diamond-like carbon (DLC), and polyimide.

33. A semiconductor device according to claim 30, wherein:

said insulating layer comprises an inorganic insulating film and an organic insulating film; and

said light shielding film is formed contacting the organic insulating film.

34. A semiconductor device according to claim 30, wherein:

said insulating layer comrises an inorganic insulating film and an organic insulating film; and

said light shielding film is formed contacting the inorganic insulating film.

35. A semiconductor device according to claim 27 wherein said semiconductor device is one selected from a group consisting of: a portable telephone, a video camera, a mobile computer, a head mount display, a projector, a portable book, a digital camera, a car navigation system, and a personal computer.

36. A semiconductor device having a panel comprising a pixel section and a driver circuit formed over a substrate, wherein:

a) said pixel section comprises a thin film transistor comprising:

a semiconductor layer formed over an insulating surface of said substrate;

a gate insulating film on said semiconductor layer and a gate electrode over said gate insulating film;

a channel forming region formed in said semiconductor layer;

a source region and a drain region formed in said semiconductor layer; and

a lightly doped drain (LDD) region, formed in said semiconductor layer to exclude the region underneath said gate electrode, and

b) said driver circuit comprises:

a first thin film transistor comprising:

a first semiconductor layer formed over an insulating surface of said substrate;

a gate insulating film on said first semiconductor layer and a first gate electrode over said gate insulating film;

a first channel forming region formed in said semiconductor layer;

a first source region and a first drain region formed in said first semiconductor layer; and

a first lightly doped drain (LDD) region, formed in said first semiconductor layer provided in a portion underneath said first gate electrode, and

a second thin film transistor comprising:

a second semiconductor layer formed over an insulating surface of said substrate;

a gate insulating film on said second semiconductor layer and a second gate electrode over said gate insulating film;

a second channel forming region formed in said second semiconductor layer;

a second source region and a second drain region formed in said second semiconductor layer; and

a second lightly doped drain (LDD) region, formed in said second semiconductor layer to exclude the region underneath said second gate electrode: and

a third thin film transistor comprising:

a third semiconductor layer formed over an insulating surface of said substrate;

a gate insulating film on said third semiconductor layer and a third gate electrode over said gate insulating film;

a third channel forming region formed in said third semiconductor layer;

a third source region and a third drain region formed in said third semiconductor layer;

a third lightly doped drain (LDD) region formed in said third semiconductor layer provided in a portion underneath said third gate electrode, and

a fourth lightly doped drain (LDD) region, formed in said third semiconductor layer to exclude the region underneath said third gate electrode.

37. A semiconductor device according to claim 36, wherein:

an impurity element having said conductivity type is included in the third impurity region and in the fourth impurity region; and

a concentration of the impurity element included in said fourth impurity region is less than a concentration of the impurity element included in said third impurity region.

38. A semiconductor device according to claim 36, wherein:

an impurity element having said conductivity type is included in the second impurity region and in the third impurity region; and

a concentration of the impurity element included in said second impurity region is the same as a concentration of the impurity element included in said third impurity region.

39. A semiconductor device according to claim 36, wherein said pixel section further comprises:

a light shielding film formed on said fourth thin film transistor interposing an insulating layer therebetween;

a pixel electrode connected to said fourth thin film transistor; and

a storage capacitor comprising said light shielding film, said insulating layer contacting said light shielding film, and the pixel electrode contacting the insulating layer,

wherein said storage capacitor is connected to said fourth thin film transistor.

40. A semiconductor device according to claim 39, wherein:

said light shielding film comprises an element selected from a group consisting of aluminum, tantalum, and titanium; and

said insulating layer comprises an oxide of said element of the light shielding film.

41. A semiconductor device according to claim 39, wherein said insulating layer comprises a material selected from silicon nitride, silicon oxide, oxidized silicon nitride, diamond-like carbon (DLC), and polyimide.

42. A semiconductor device according to claim 39, wherein:

said insulating layer comprises an inorganic insulating film and an organic insulating film; and

said light shielding film is formed contacting the organic insulating film.

43. A semiconductor device according to claim 39, wherein:

said insulating layer comrises an inorganic insulating film and an organic insulating film; and

said light shielding film is formed contacting the inorganic insulating film.

44. A semiconductor device according to claim 39 wherein said semiconductor device is one selected from a group consisting of: a portable telephone, a video camera, a mobile computer, a head mount display, a projector, a portable book, a digital camera, a car navigation system, and a personal computer.

45. A method of manufacturing a semiconductor device, comprising:

a step of forming a plural number of island semiconductor layers over a substrate having an insulating surface;

a step of forming a gate insulating layer contacting said island semiconductor layers;

a step of forming gate electrodes contacting said gate insulating layer;

a step of forming a first thin film transistor having a first impurity region, and a third impurity region which overlaps said gate electrode, by doping an impurity element with one conductivity type into selected regions of said island shape semiconductor layers;

a step of forming a fifth thin film transistor having a fifth impurity region, by doping an impurity element with inverse conductivity type into selected regions of said island shape semiconductor layers; and a step of forming a fourth thin film transistor having a first impurity region and a fourth impurity region, by doping an impurity element with one conductivity type into selected regions of said island shape semiconductor layers.

46. A method of manufacturing a semiconductor device according to claim 45, wherein:

the same impurity element with one conductivity type is doped into said third impurity region and into said fourth impurity region; and

a concentration of the impurity element included in said fourth impurity region is doped to less than said concentration of the impurity element included in said third impurity region.

47. A method of manufacturing a semiconductor device according to claim 45, wherein:

the same impurity element with one conductivity type is doped into said second impurity region and into said third impurity region; and

a concentration of the impurity element included in said second impurity region is doped to the same as said concentration of the impurity element included in said third impurity region.

48. A method of manufacturing a semiconductor device according to claim 45, wherein:

a storage capacitor is formed by:

a step of forming an insulating layer on said fourth thin film transistor;

a step of forming a light shielding film on said insulating layer;

a step of forming a dielectric film contacting said light shielding film; and

a step of forming a conductive film contacting said dielectric film.

49. A method of manufacturing a semiconductor device according to claim 48, wherein said step of forming the dielectric film contacting the light shielding film is an anodic oxidation process.

50. A method of manufacturing a semiconductor device according to claim 48, wherein said light shielding film is formed from a material selected from a group consisting of aluminum, tantalum, and titanium.

51. A method of manufacturing a semiconductor device according to claim 48, wherein:

said insulating layer is formed from an inorganic insulating layer and an organic insulating layer; and

said light shielding film is formed contacting the organic insulating layer.

52. A method of manufacturing a semiconductor device according to claim 48, wherein:

said insulating layer is formed from an inorganic insulating layer and an organic insulating layer; and

said light shielding film is formed contacting the inorganic insulating layer.

53. A method of manufacturing a semiconductor device according to claim

45, wherein said semiconductor device is an electronic device selected from a group consisting of portable telephone, a video camera, a mobile computer, a head mount display, a projector, a portable book, a digital camera, a car navigation system, and a personal computer.

54. A method of manufacturing a semiconductor device, comprising:

a step of forming a plural number of island semiconductor layers over a substrate having an insulating surface;

a step of forming a gate insulating layer contacting said island semiconductor layers;

a step of forming gate electrodes contacting said gate insulating layer;

a step of forming a first thin film transistor having a first impurity region, and a third impurity region which overlaps said gate electrode, by doping an impurity element with one conductivity type into selected regions of said island shape semiconductor layers;

a step of forming a second thin film transistor having a first impurity region, a third impurity region which overlaps said gate electrode, and a second impurity region which does not overlap said gate electrode, by doping an impurity element with one conductivity type into selected regions of said island shape semiconductor layers;

a step of forming a fifth thin film transistor having a fifth impurity region, by doping an impurity element with inverse conductivity type into selected regions of said island shape semiconductor layers; and

a step of forming a fourth thin film transistor having a first impurity region and a fourth impurity region, by doping an impurity element with one conductivity type into selected regions of said island shape semiconductor layers.

55. A method of manufacturing a semiconductor device according to claim 54, wherein:

the same impurity element with one conductivity type is doped into said third impurity region and into said fourth impurity region; and

a concentration of the impurity element included in said fourth impurity region is doped to less than said concentration of the impurity element included in said third impurity region.

56. A method of manufacturing a semiconductor device according to claim 54, wherein:

the same impurity element with one conductivity type is doped into said second impurity region and into said third impurity region; and

a concentration of the impurity element included in said second impurity region is doped to the same as said concentration of the impurity element included in said third impurity region.

57. A method of manufacturing a semiconductor device according to claim 54, wherein:

a storage capacitor is formed by:

a step of forming an insulating layer on said fourth thin film transistor;

a step of forming a light shielding film on said insulating layer;

a step of forming a dielectric film contacting said light shielding film; and

a step of forming a conductive film contacting said dielectric film.

58. A method of manufacturing a semiconductor device according to claim 57, wherein said step of forming the dielectric film contacting the light shielding film is an anodic oxidation process.

59. A method of manufacturing a semiconductor device according to claim 57, wherein said light shielding film is formed from a material selected from a group consisting of aluminum, tantalum, and titanium.

60. A method of manufacturing a semiconductor device according to claim 57, wherein:

said insulating layer is formed from an inorganic insulating layer and an organic insulating layer; and

said light shielding film is formed contacting the organic insulating layer.

61. A method of manufacturing a semiconductor device according to claim 57, wherein:

said insulating layer is formed from an inorganic insulating layer and an organic insulating layer; and

said light shielding film is formed contacting the inorganic insulating layer.

62. A method of manufacturing a semiconductor device according to claim

54, wherein said semiconductor device is an electronic device selected from a group consisting of portable telephone, a video camera, a mobile computer, a head mount display, a projector, a portable book, a digital camera, a car navigation system, and a personal computer.

63. A method of manufacturing a semiconductor device, comprising:

a step of forming a plural number of island semiconductor layers over a substrate having an insulating surface;

a step of forming gate insulating films contacting said island semiconductor layers;

a step of forming gate electrodes contacting said gate insulating films;

a step of forming a first thin film transistor having a first impurity region, and a third impurity region which overlaps said gate electrodes, by doping an impurity element with one conductivity type into selected regions of said island shape semiconductor layers;

a step of forming a third thin film transistor having a first impurity region, and a second impurity region which does not overlap said gate electrode, by doping an impurity element with one type conductivity into selected regions of said island shape semiconductor layers;

a step of forming a fifth thin film transistor having a fifth impurity region, by doping an impurity element with inverse conductivity type into selected regions of said island shape semiconductor layers; and

a step of forming a fourth thin film transistor having a first impurity region and a fourth impurity region, by doping an impurity element with one conductivity type into selected regions of said island shape semiconductor layers.

64. A method of manufacturing a semiconductor device according to claim 63, wherein:

the same impurity element with one conductivity type is doped into said third impurity region and into said fourth impurity region; and

a concentration of the impurity element included in said fourth impurity region is doped to less than said concentration of the impurity element included in said third impurity region.

65. A method of manufacturing a semiconductor device according to claim 63, wherein:

the same impurity element with one conductivity type is doped into said second impurity region and into said third impurity region; and

a concentration of the impurity element included in said second impurity region is doped to the same as said concentration of the impurity element included in said third impurity region.

66. A method of manufacturing a semiconductor device according to claim 63, wherein:

a storage capacitor is formed by:

a step of forming an insulating layer on said fourth thin film transistor;

a step of forming a light shielding film on said insulating layer;

a step of forming a dielectric film contacting said light shielding film; and

a step of forming a conductive film contacting said dielectric film.

67. A method of manufacturing a semiconductor device according to claim 66, wherein said step of forming the dielectric film contacting the light shielding film is an anodic oxidation process.

68. A method of manufacturing a semiconductor device according to claim 66, wherein said light shielding film is formed from a material selected from a group consisting of aluminum, tantalum, and titanium.

69. A method of manufacturing a semiconductor device according to claim 66, wherein:

said insulating layer is formed from an inorganic insulating layer and an organic insulating layer; and

said light shielding film is formed contacting the organic insulating layer.

70. A method of manufacturing a semiconductor device according to claim 66, wherein:

said insulating layer is formed from an inorganic insulating layer and an organic insulating layer; and

said light shielding film is formed contacting the inorganic insulating layer.

71. A method of manufacturing a semiconductor device according to claim

63, wherein said semiconductor device is an electronic device selected from a group consisting of portable telephone, a video camera, a mobile computer, a head mount display, a projector, a portable book, a digital camera, a car navigation system, and a personal computer.

72. A method of manufacturing a semiconductor device, comprising:

a step of forming a plural number of island shape semiconductor layers on a substrate having an insulating surface;

a step of forming gate insulating films contacting said island shape semiconductor layers;

a step of forming gate electrodes contacting said gate insulating films;

a step of forming a first thin film transistor having a first impurity region, and a third impurity region which overlaps said gate electrodes, by doping an impurity element with one conductivity type into selected regions of said island shape semiconductor layers;

a step of forming a second thin film transistor having a first impurity region, a third impurity region which overlaps said gate electrode, and a second impurity region which does not overlap said gate electrode, by doping an impurity element with one conductivity type into selected regions of said island shape semiconductor layers;

a step of forming a third thin film transistor having a first impurity region, and a second impurity region which does not overlap said gate electrode, by doping an impurity element with one conductivity type into selected regions of said island shape semiconductor layers;

a step of forming a fifth thin film transistor having a fifth impurity region, by doping an impurity element with inverse conductivity type into selected regions of said island shape semiconductor layers; and

a step of forming a fourth thin film transistor having a first impurity region and a fourth impurity region, by doping an impurity element with one conductivity type into selected regions of said island shape semiconductor layers.

73. A method of manufacturing a semiconductor device according to claim 72, wherein:

the same impurity element with one conductivity type is doped into said third impurity region and into said fourth impurity region; and

a concentration of the impurity element included in said fourth impurity region is doped to less than said concentration of the impurity element included in said third impurity region.

74. A method of manufacturing a semiconductor device according to claim 72, wherein:

the same impurity element with one conductivity type is doped into said second impurity region and into said third impurity region; and

a concentration of the impurity element included in said second impurity region is doped to the same as said concentration of the impurity element included in said third impurity region.

75. A method of manufacturing a semiconductor device according to claim 72, wherein:

a storage capacitor is formed by:

a step of forming an insulating layer on said fourth thin film transistor;

a step of forming a light shielding film on said insulating layer;

a step of forming a dielectric film contacting said light shielding film; and

a step of forming a conductive film contacting said dielectric film.

76. A method of manufacturing a semiconductor device according to claim 75 wherein said step of forming the dielectric film contacting the light shielding film is an anodic oxidation process.

77. A method of manufacturing a semiconductor device according to claim 75, wherein said light shielding film is formed from a material selected from a group consisting of aluminum, tantalum, and titanium.

78. A method of manufacturing a semiconductor device according to claim 75, wherein:

said insulating layer is formed from an inorganic insulating layer and an organic insulating layer; and

said light shielding film is formed contacting the organic insulating layer.

79. A method of manufacturing a semiconductor device according to claim 75, wherein:

said insulating layer is formed from an inorganic insulating layer and an organic insulating layer; and said light shielding film is formed contacting the inorganic insulating layer.

80. A method of manufacturing a semiconductor device according to claim 72, wherein said semiconductor device is an electronic device selected from a group consisting of portable telephone, a video camera, a mobile computer, a head mount display, a projector, a portable book, a digital camera, a car navigation system, and a personal computer.

81. A semiconductor device according to claim 1 wherein said semiconductor device comprises an electro-luminescence display panel.

82. A semiconductor device according to claim 9 wherein said semiconductor device comprises an electro-luminescence display panel.

83. A semiconductor device according to claim 18 wherein said semiconductor device comprises an electro-luminescence display panel.

84. A semiconductor device according to claim 27 wherein said semiconductor device comprises an electro-luminescence display panel.

85. A semiconductor device according to claim 36 wherein said semiconductor device comprises an electro-luminescence display panel.

ABSTRACT OF THE DISCLOSURE

In an active matrix type liquid crystal display device, in which functional circuits such as a shift register circuit and a buffer circuit are incorporated on the same substrate, an optimal TFT structure is provided along with the aperture ratio of a pixel matrix circuit is increased. There is a structure in which an n-channel TFT, with a third impurity region which overlaps a gate electrode, is formed in a buffer circuit, etc., and an n-channel TFT, in which a fourth impurity region which does not overlap the gate electrode, is formed in a pixel matrix circuit. A storage capacitor formed in the pixel matrix circuit is formed by a light shielding film, a dielectric film formed on the light shielding film, and a pixel electrode. Al is especially used in the light shielding film, and the dielectric film is formed anodic oxidation process, using an Al oxide film.

Fig. 1A

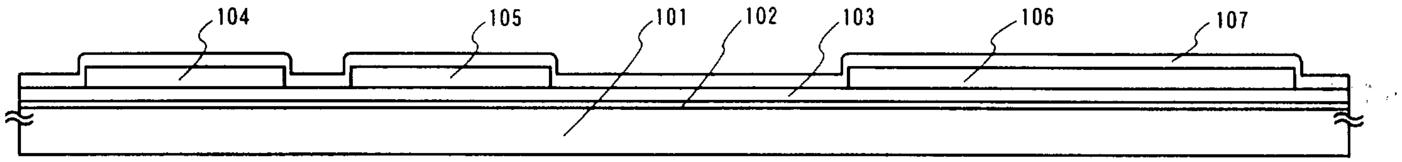


Fig. 1B

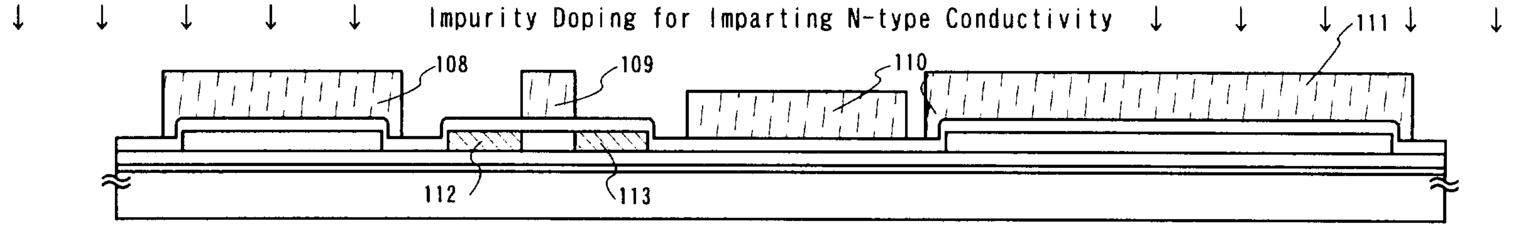


Fig. 1C

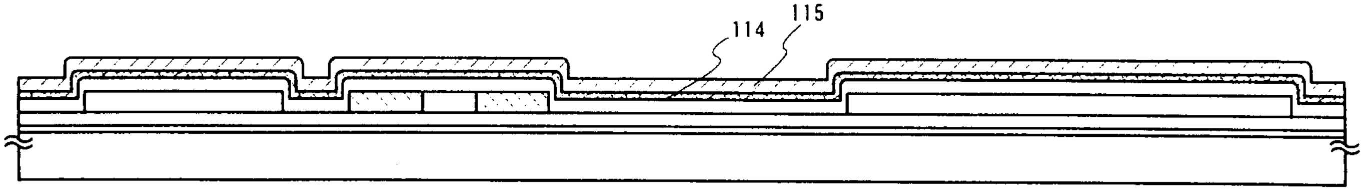


Fig. 2A

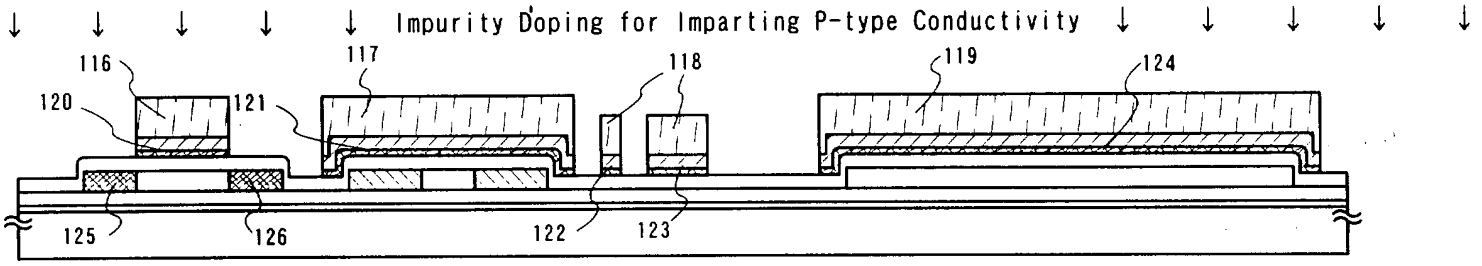


Fig. 2B

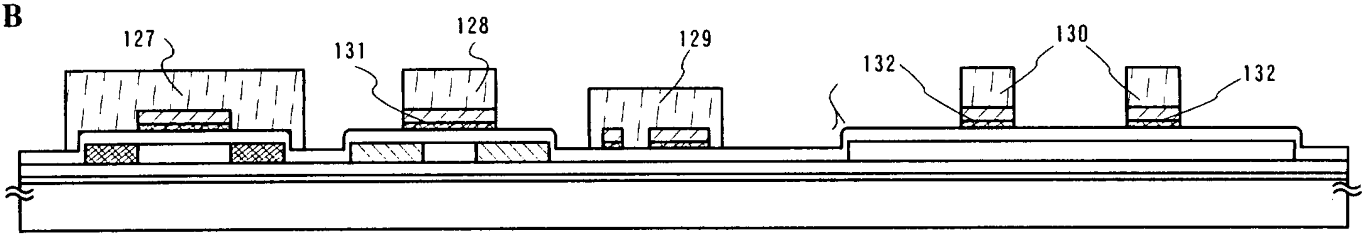


Fig. 2C

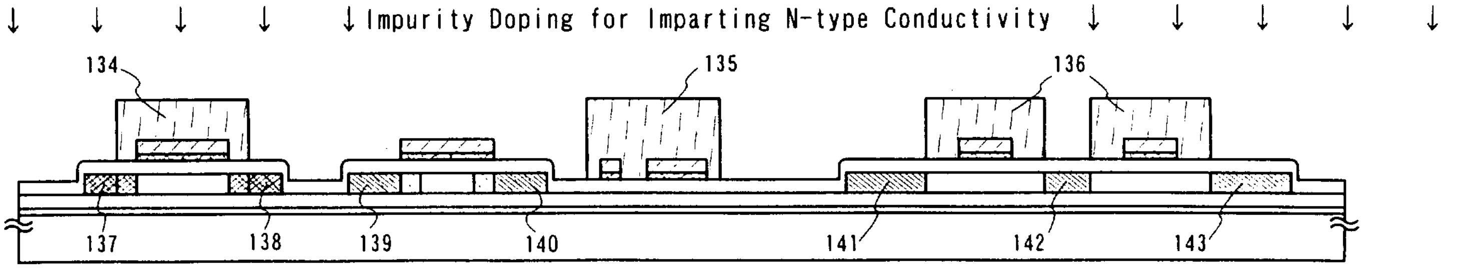


Fig. 3A

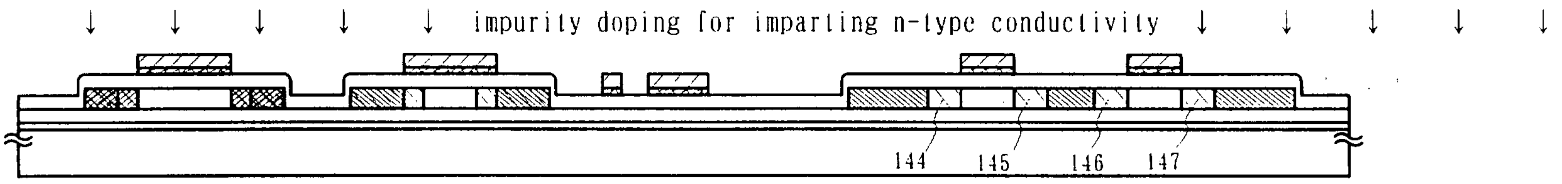


Fig. 3B

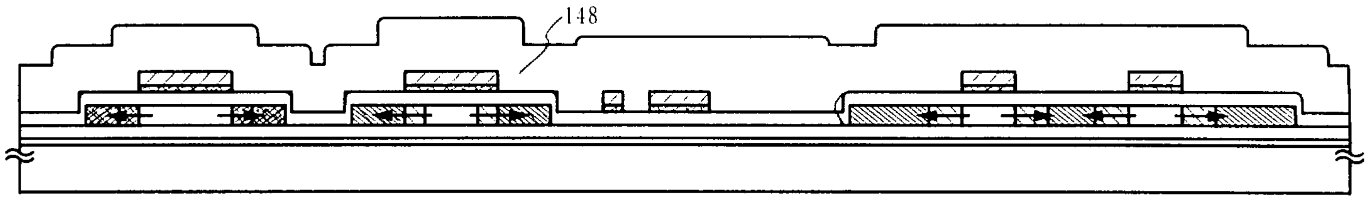


Fig. 3C

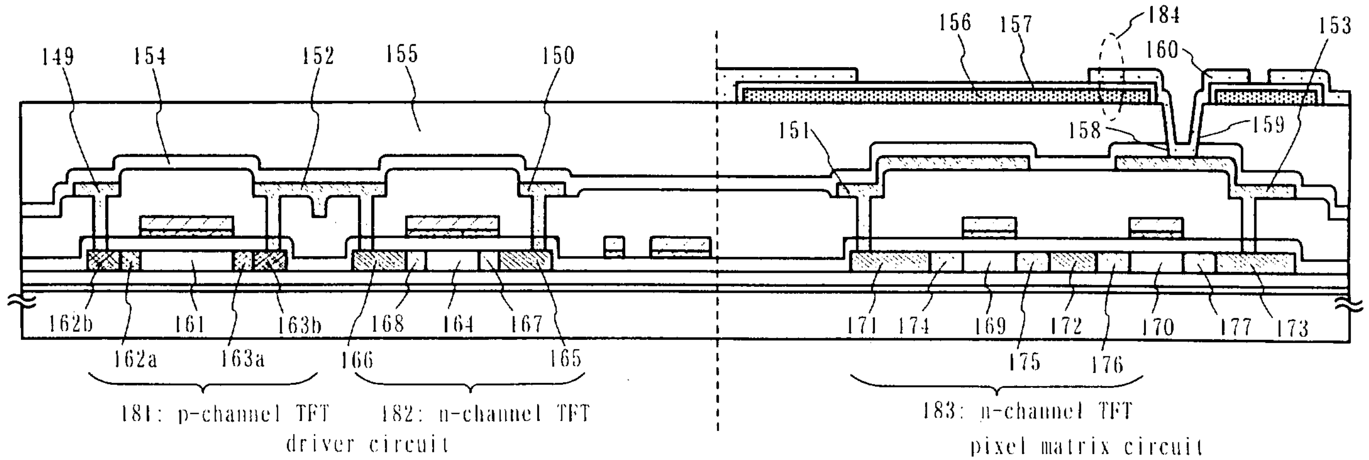
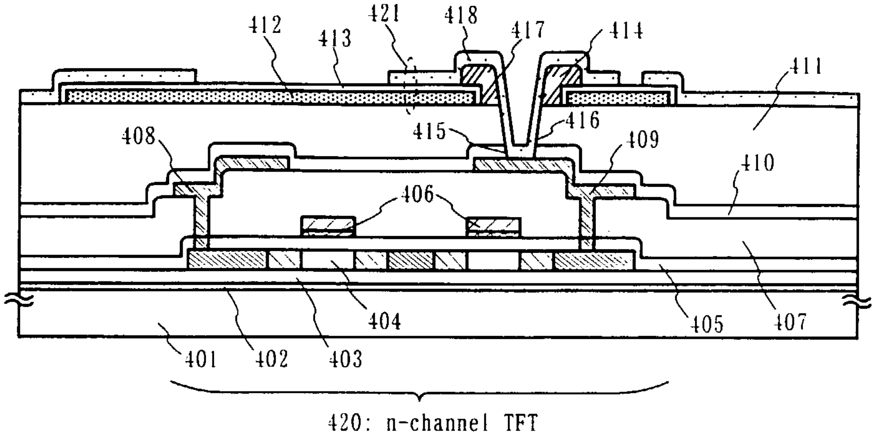


Fig. 4



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420: n-channel TFT

Fig. 5A

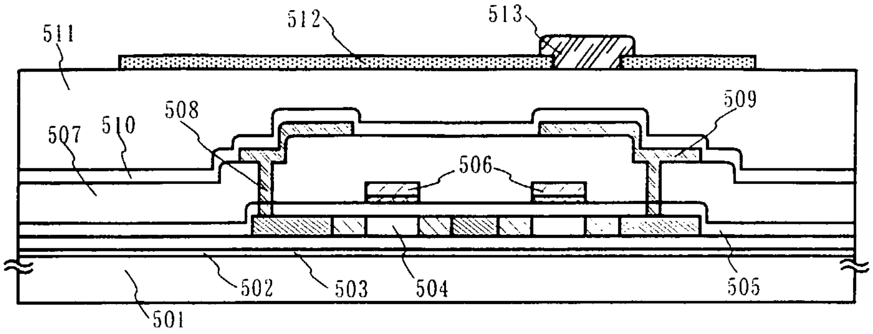


Fig. 5B

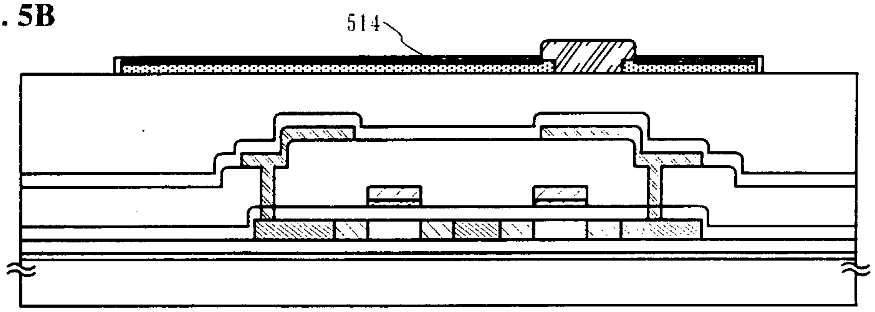


Fig. 5C

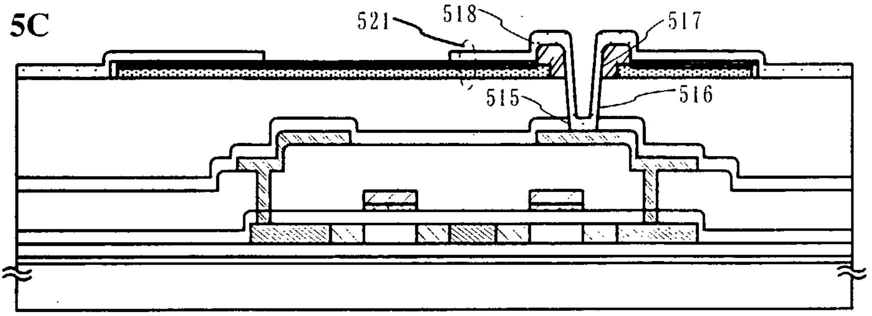


Fig. 6A

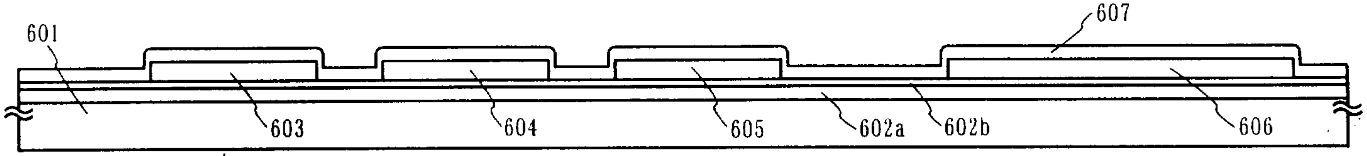


Fig. 6B

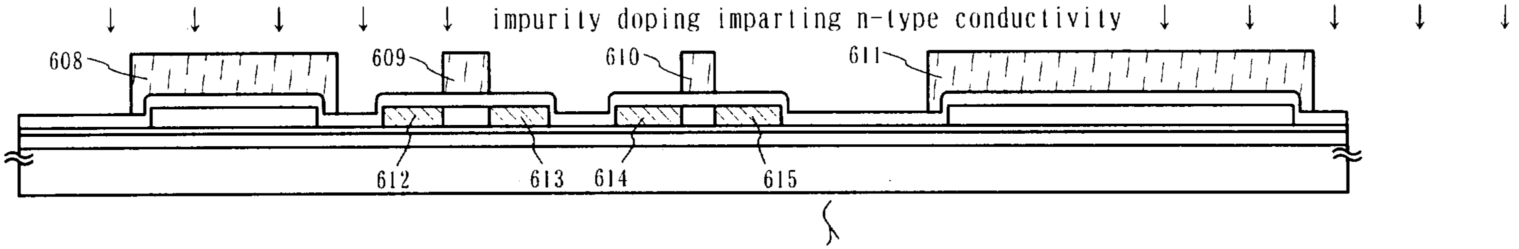


Fig. 6C

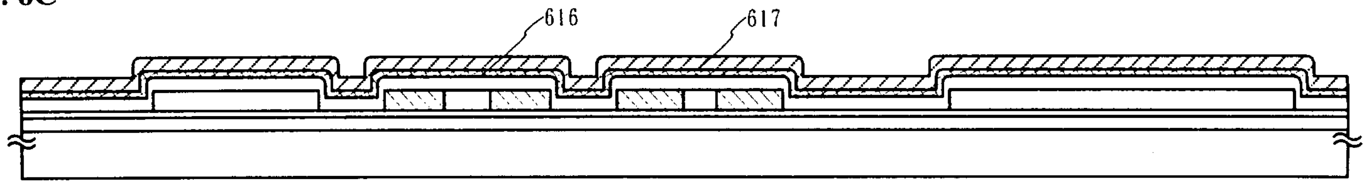


Fig. 6D

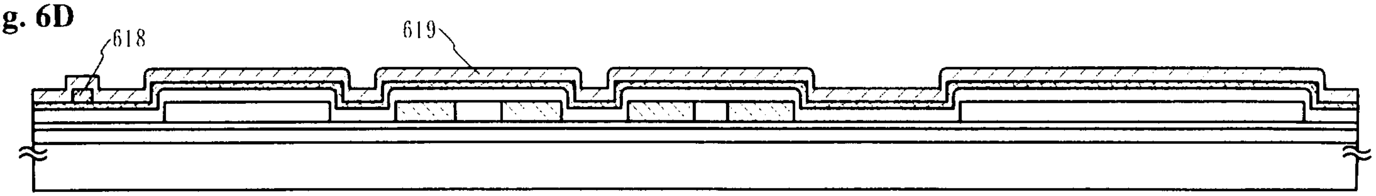


Fig. 7A

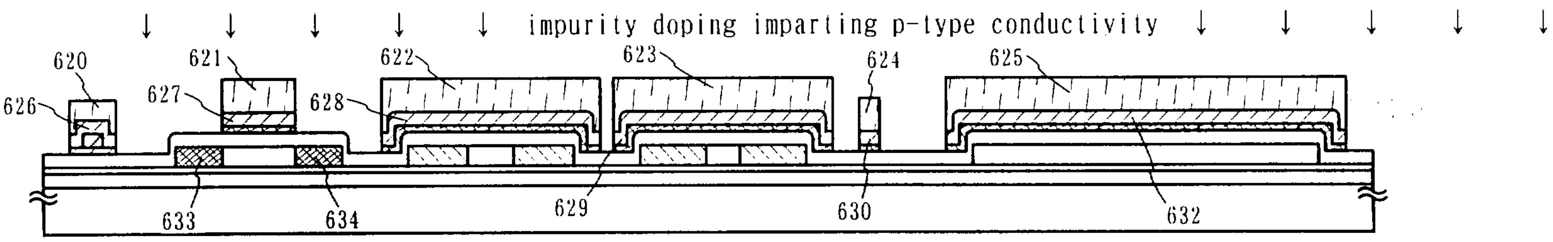


Fig. 7B

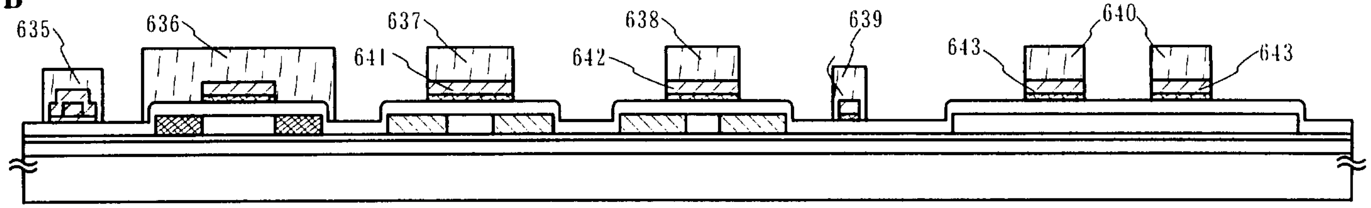


Fig. 7C

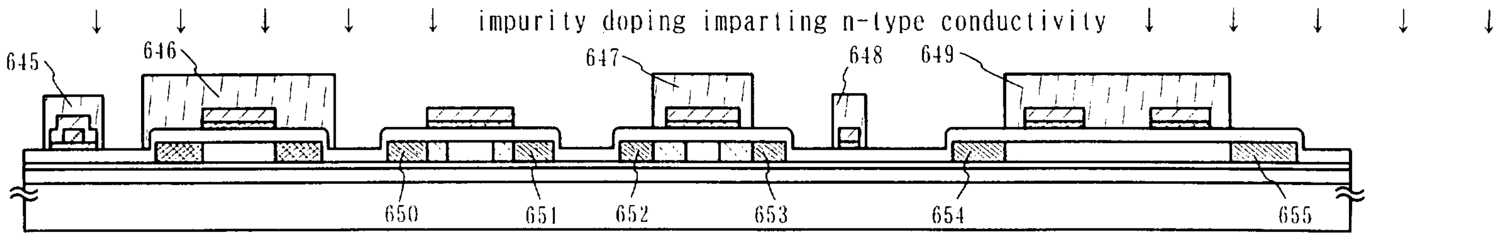


Fig. 8A

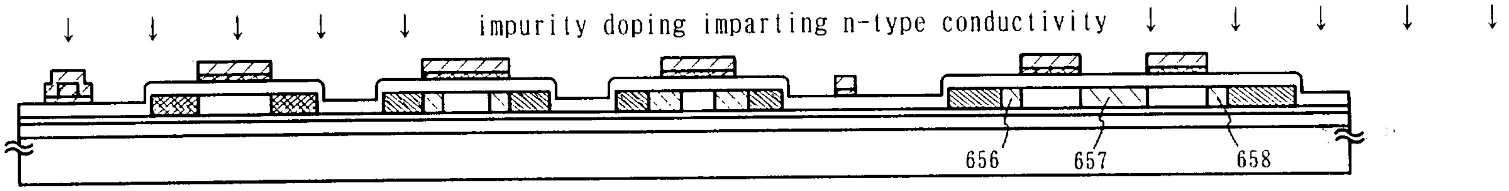


Fig. 8B

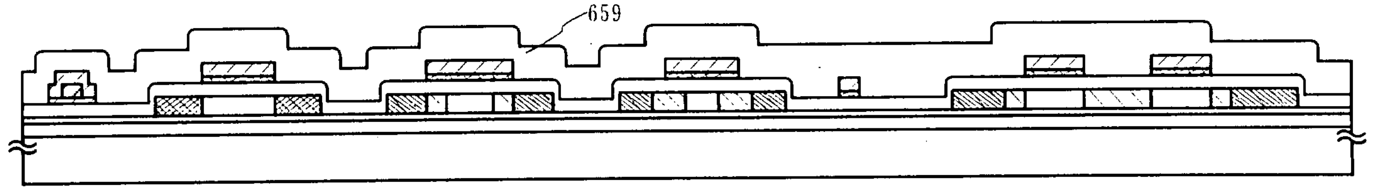


Fig. 8C

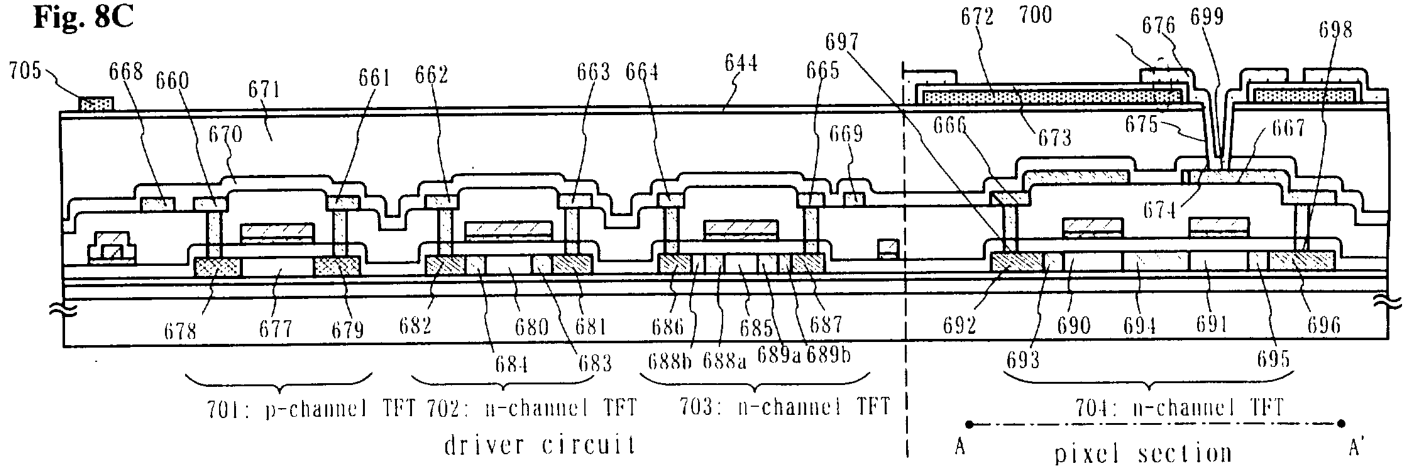
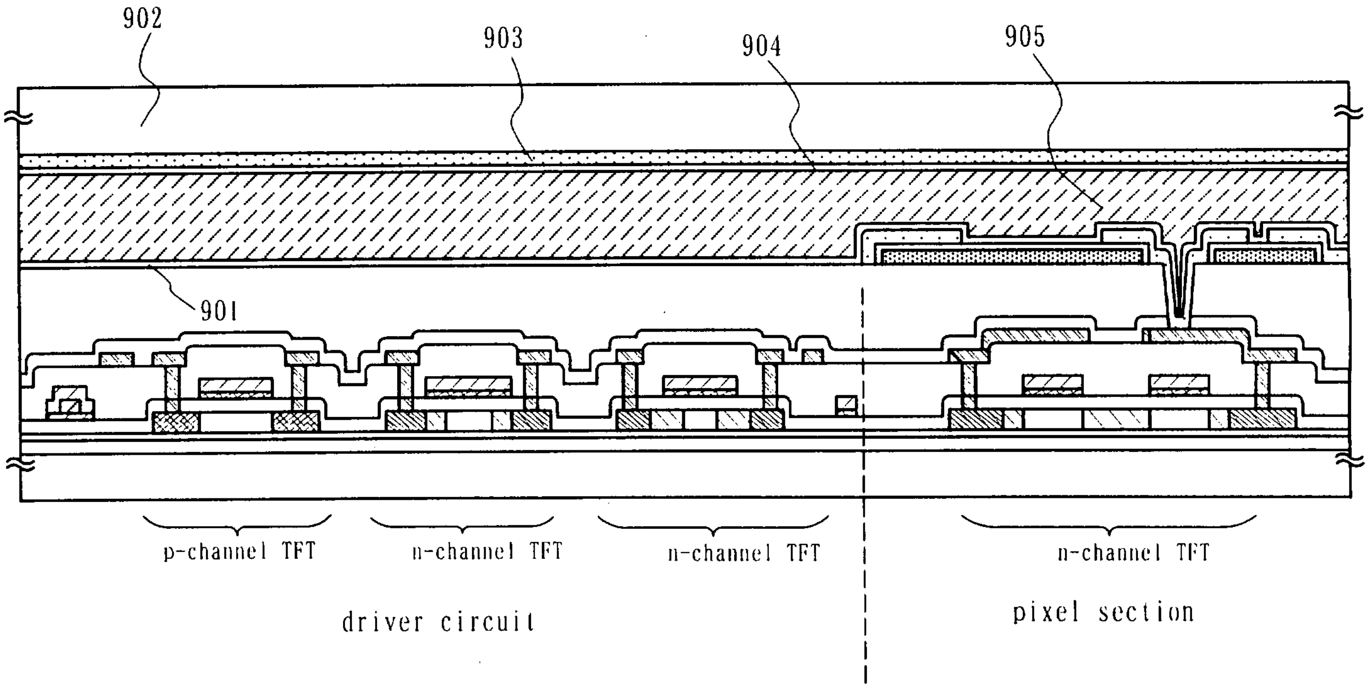


Fig. 9


902
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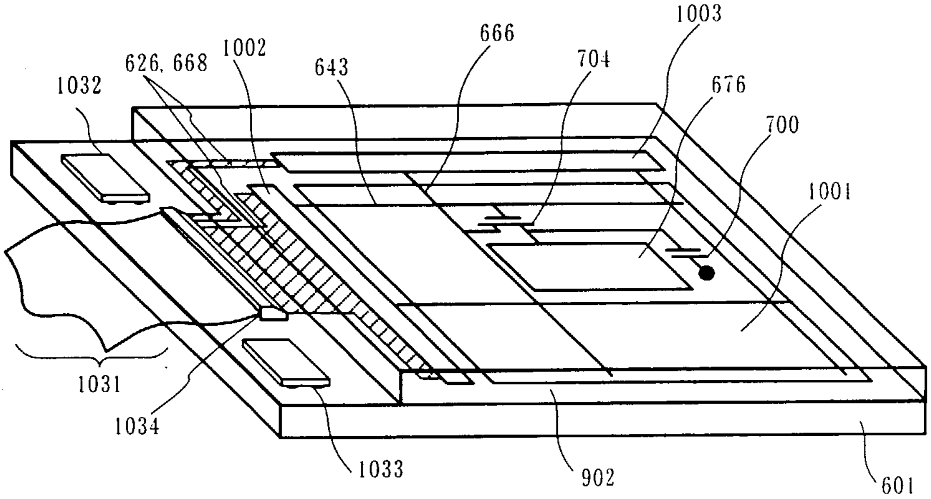
p-channel TFT
n-channel TFT
n-channel TFT
n-channel TFT
driver circuit
pixel section

Fig. 10



1032
626, 668
1002
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601

Fig. 11A

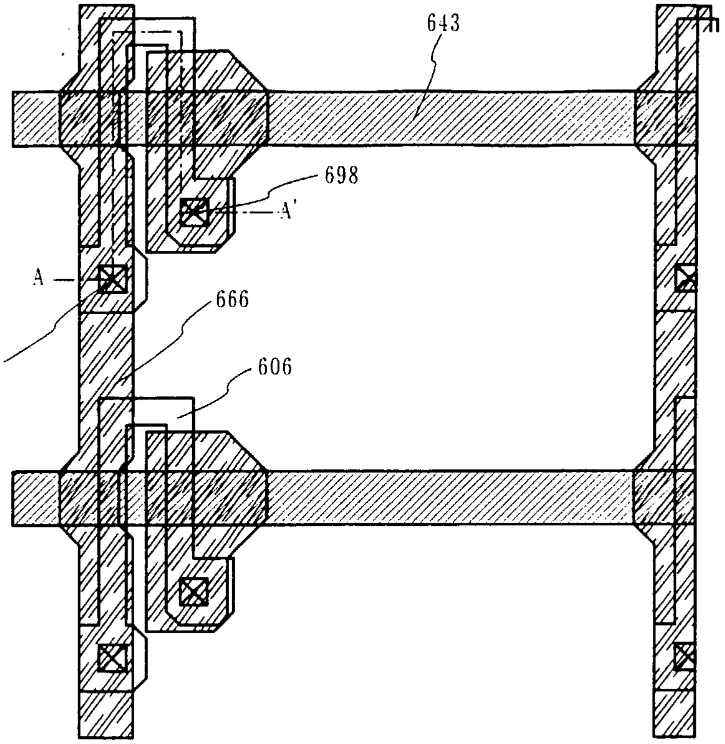


Fig. 11B

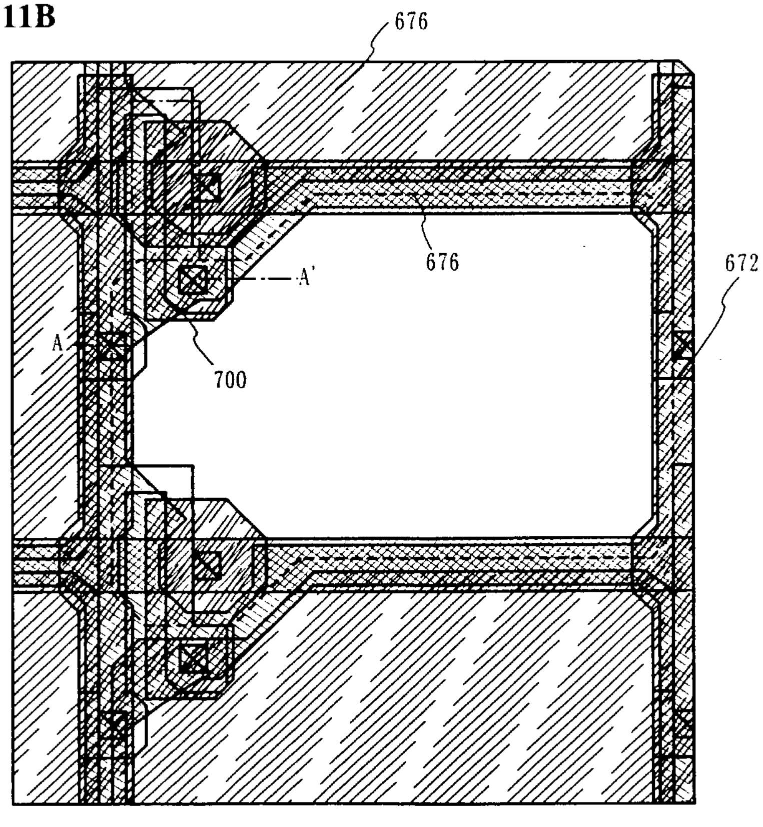


Fig. 12A

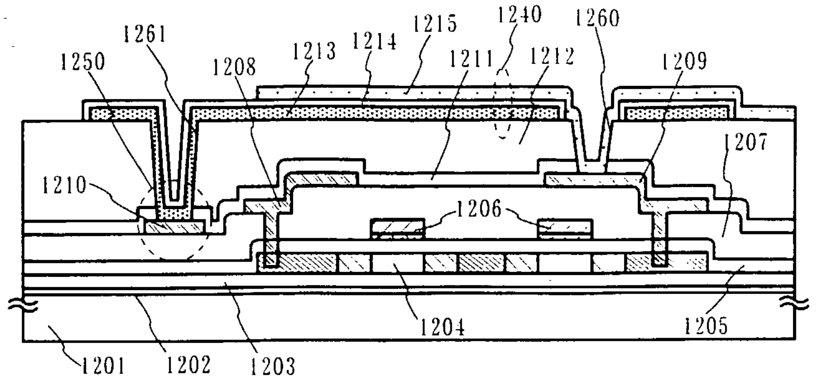


Fig. 12B

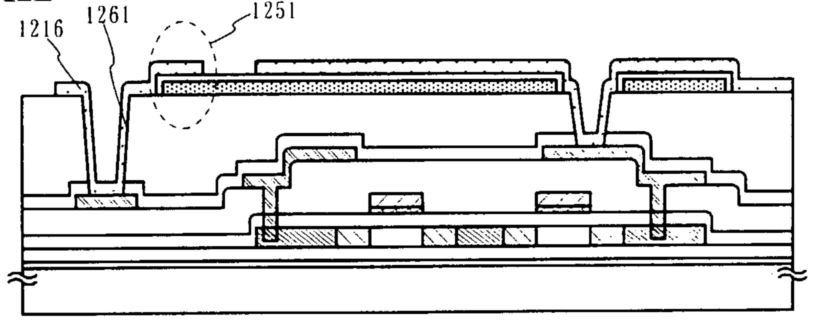


Fig. 12C

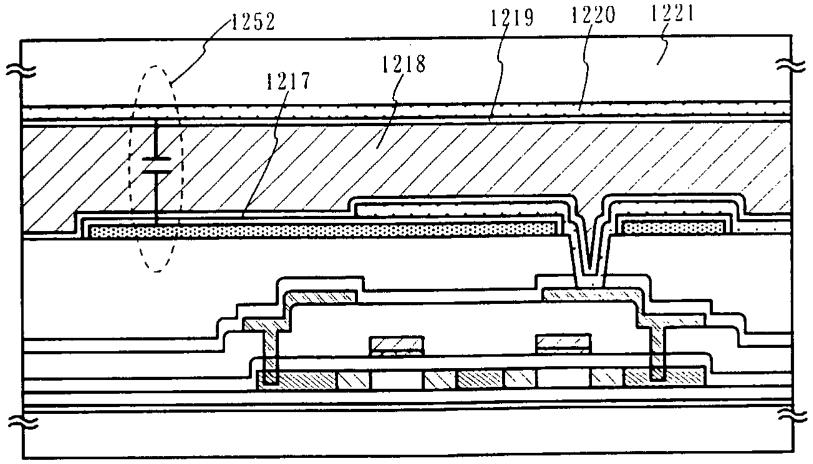


Fig. 13

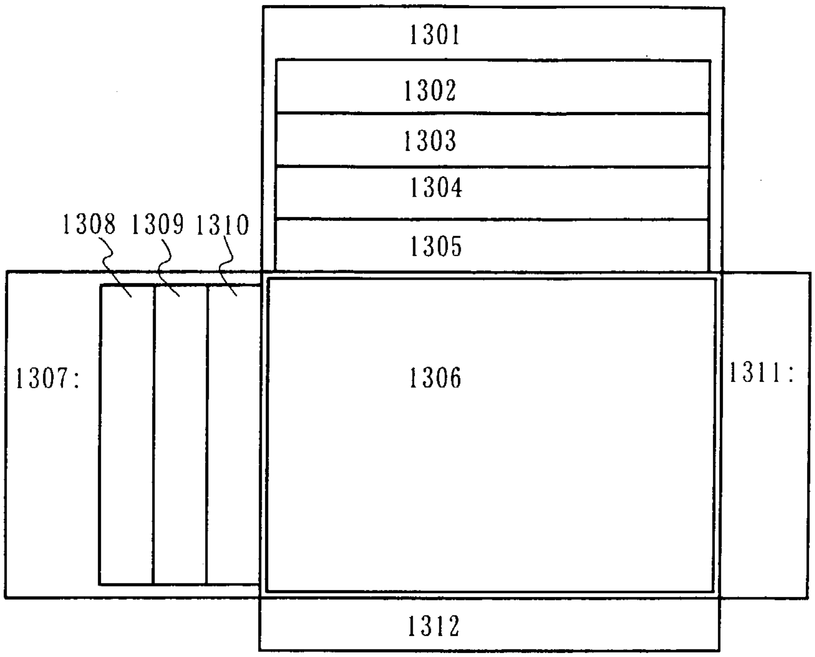


Fig. 14A

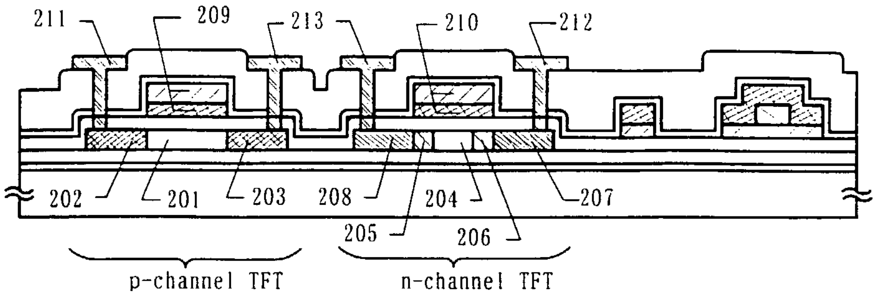


Fig. 14B

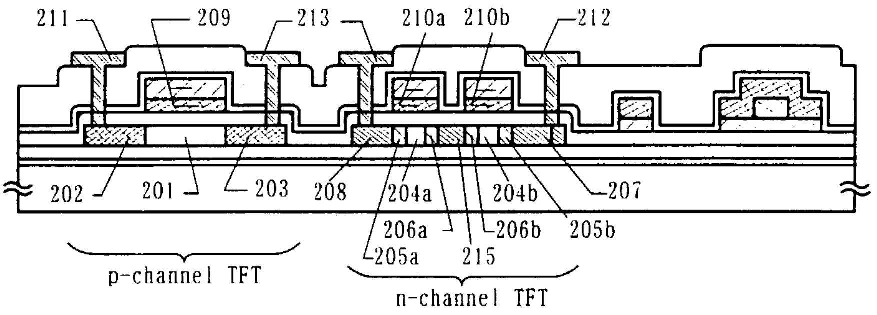


Fig. 14C

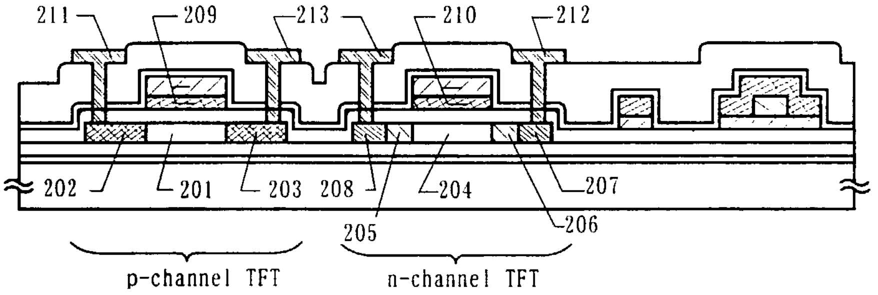


Fig. 14D

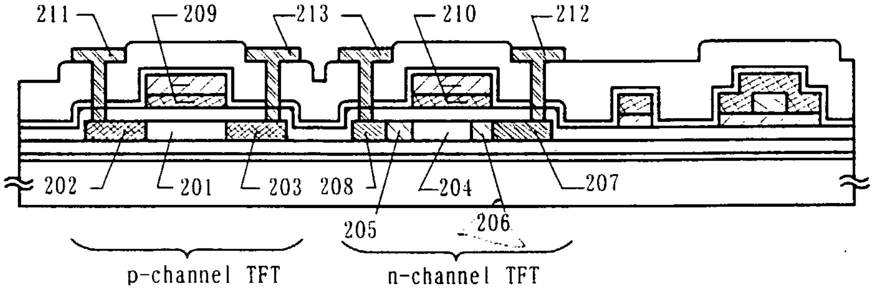
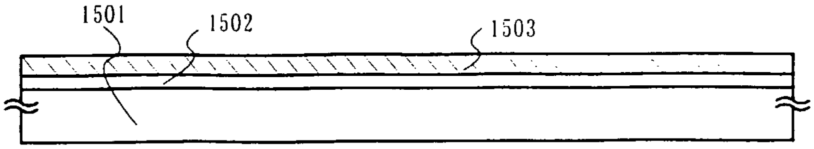


Fig. 15A



Fig, 15B

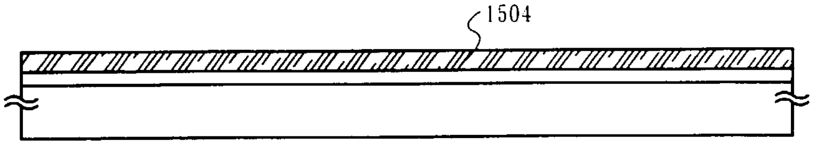


Fig. 15C

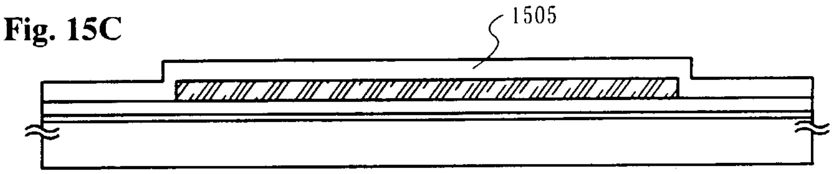


Fig. 16A

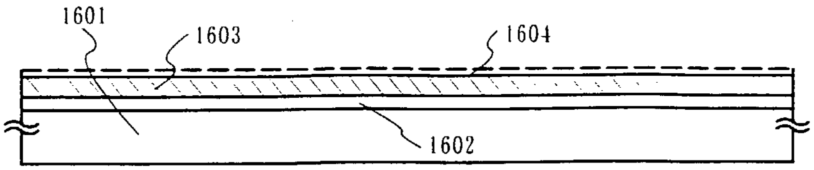


Fig. 16B

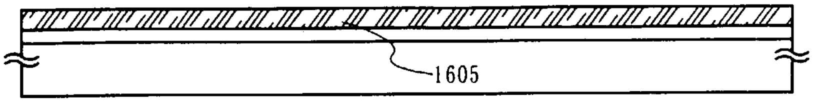


Fig. 16C

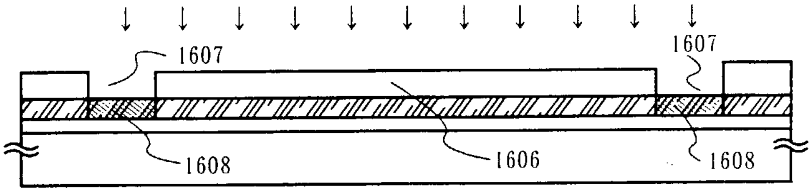


Fig. 16D

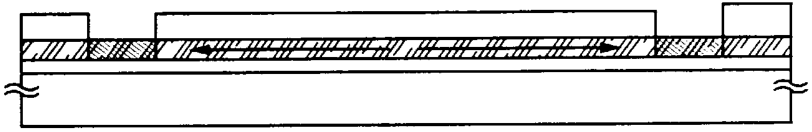


Fig. 16E

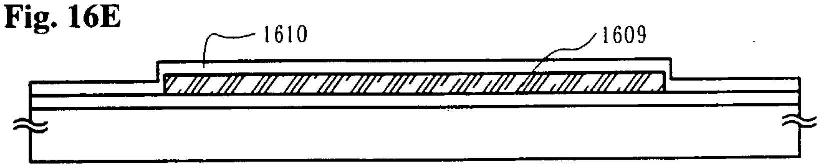


Fig. 17A

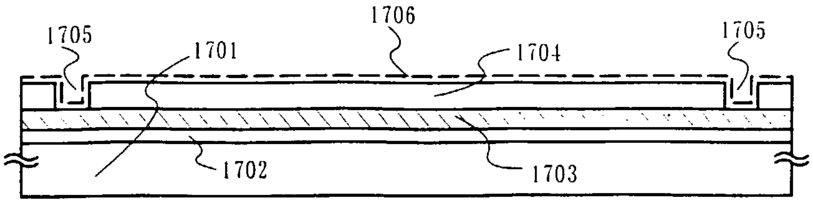


Fig. 17B

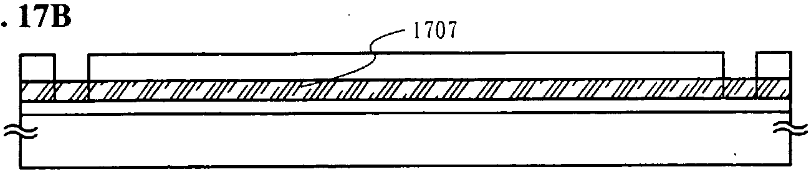


Fig. 17C

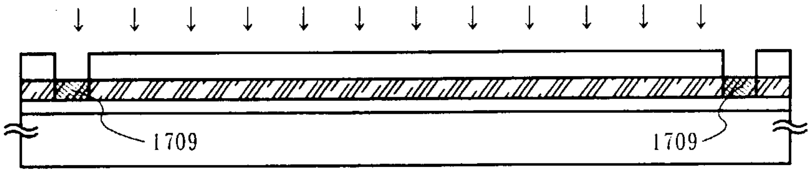


Fig. 17D

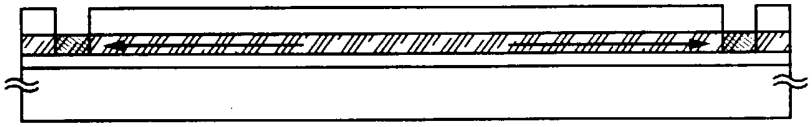


Fig. 17E

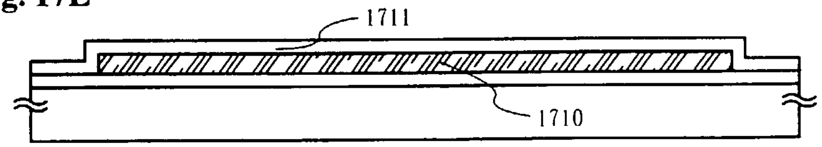


Fig. 18A

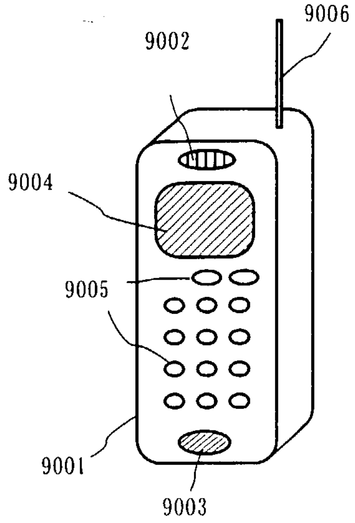


Fig. 18B

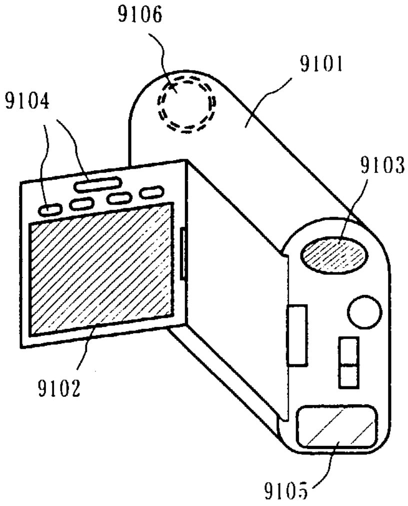


Fig. 18C

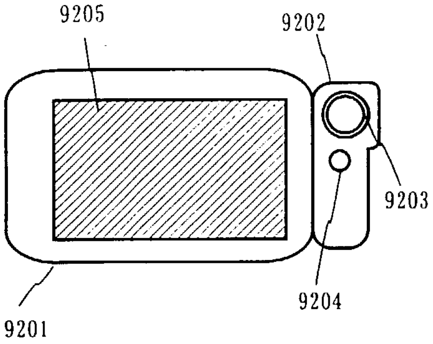


Fig. 18D

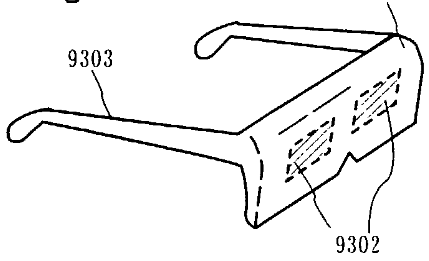


Fig. 18E

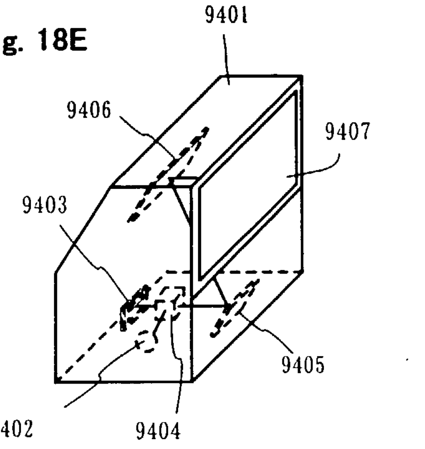
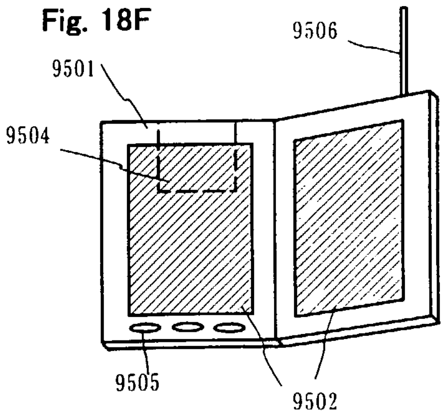


Fig. 18F



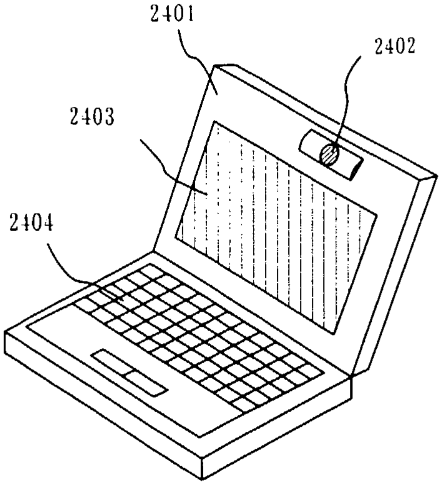


Fig. 19A

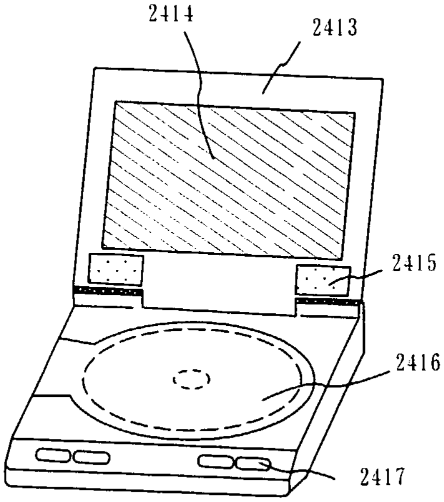


Fig. 19B

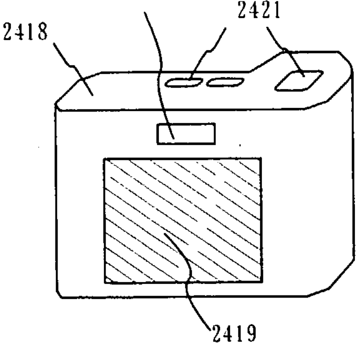


Fig. 19C

Fig. 20A

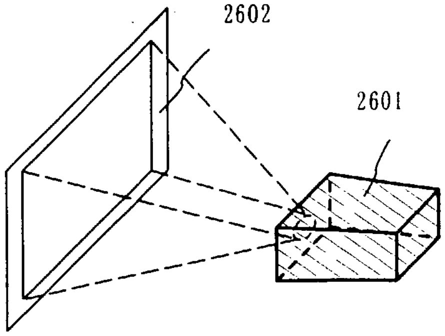


Fig. 20B

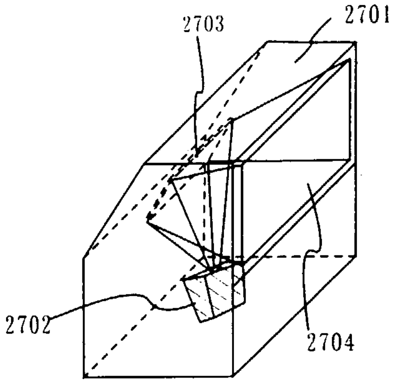


Fig. 20C

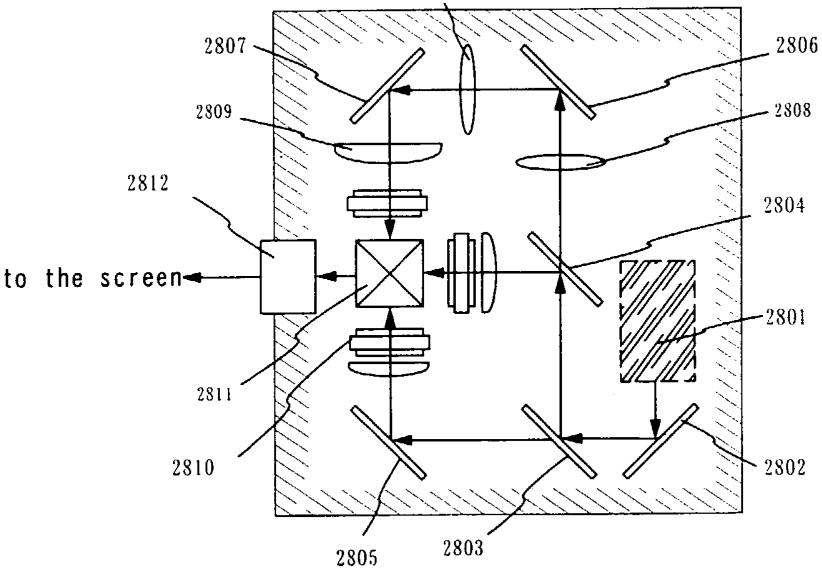


Fig. 20D

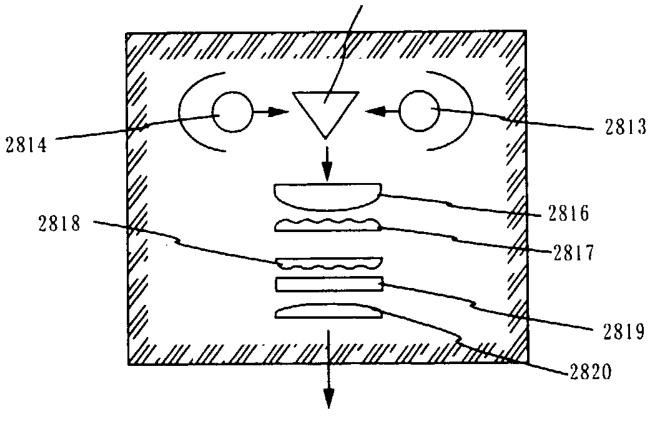


Fig. 21A

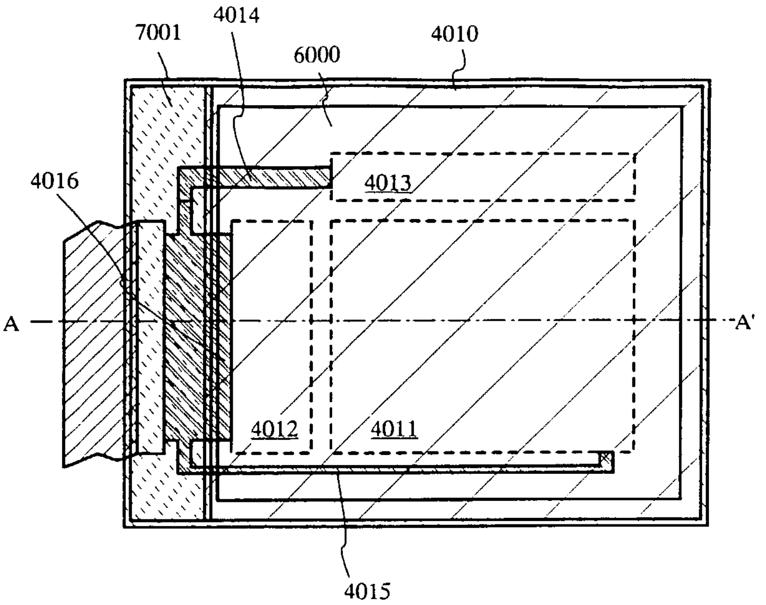


Fig. 21B

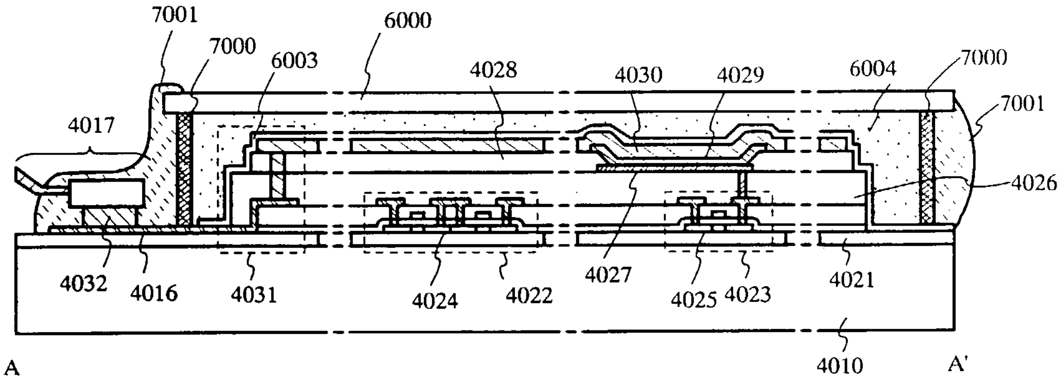


Fig. 22A

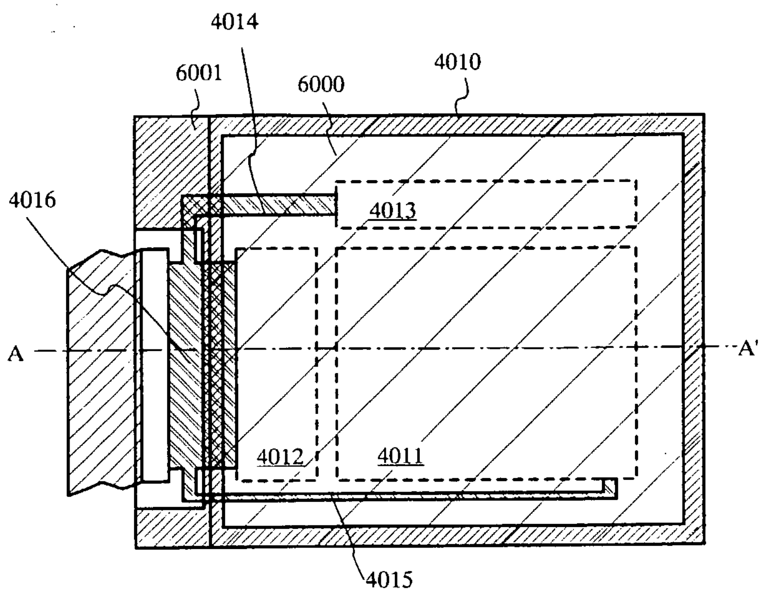


Fig. 22B

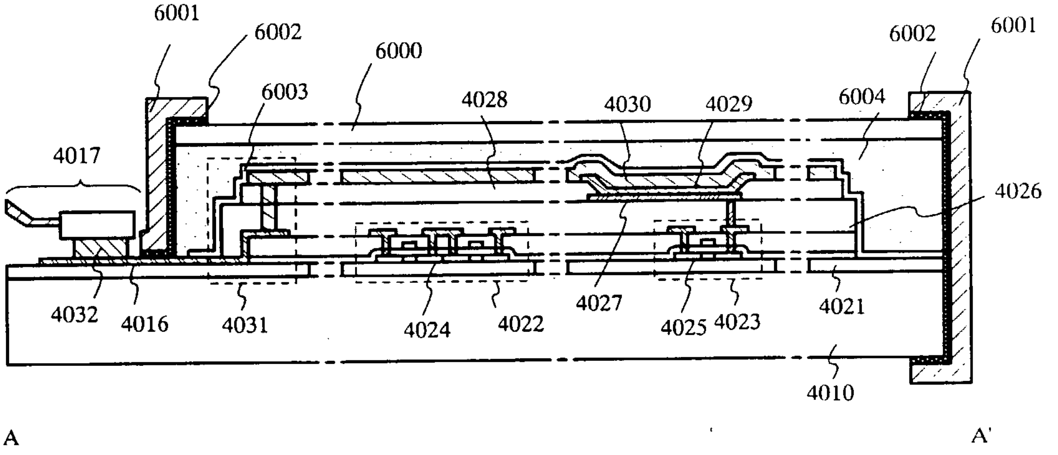
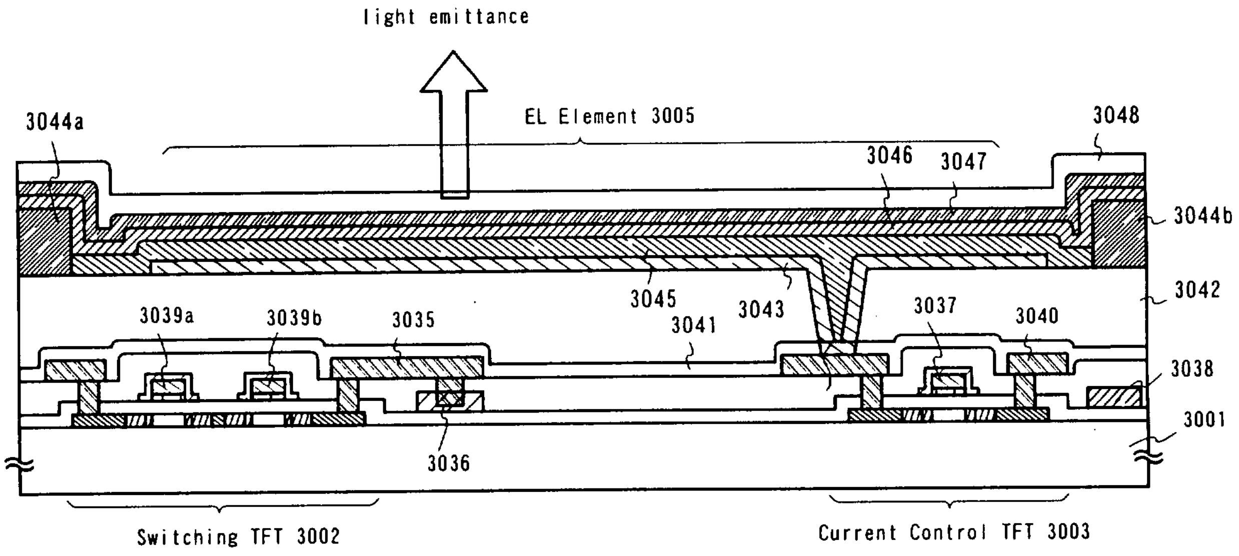


Fig. 23


light emittance
3044a
EL Element 3005
3048
3046
3047
3044b
3042
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3039b
3035
3037
3040
3038
3001
3036
Switching TFT 3002
Current Control TFT 3003

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Date Mailed: 06/21/2000

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Continuing Data as Claimed by Applicant

Foreign Applications

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If Required, Foreign Filing License Granted 05/02/2000

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Title

Semiconductor device and fabrication method thereof

Preliminary Class

257

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SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a semiconductor device having a circuit comprising thin film transistors (hereinafter referred to as "TFTs") on a substrate having an insulation surface, and to a fabrication method of such a semiconductor device. More specifically, the present invention relates to electro-optical apparatuses (called also "electronic appliances") typified by a liquid crystal display device including a pixel unit (pixel matrix circuit) and driving circuits (driver circuits) disposed around the pixel unit and formed on the same substrate and an EL (Electro-Luminescence) display device, and electrical appliances (called also "electronic appliances") having the electro-optical apparatus mounted thereto.

The term "semiconductor device" used in this specification represents generally those apparatuses which function by utilizing semiconductor characteristics, and includes also the electro-optical apparatuses and electrical appliances using the electro-optical apparatus described above.

2. Description of the Related Art

Development of a semiconductor device having a large area integrated circuit, that comprises TFTs formed on a substrate having an insulation surface, has been made progressively. An active matrix type liquid crystal display device, an EL display device and a close adhesion type image sensor are typical of such semiconductor devices. Particularly because TFTs using a polycrystalline silicon film (typically, a poly-Si film) as an active layer (the TFT will be hereinafter referred to as "poly-silicon TFT") have high field mobility, they can form a variety of functional circuits.

In the active matrix type liquid crystal display device, for example, an integrated circuit that includes a pixel unit for displaying images for each functional block, a shift register circuit, a level shifter circuit, a buffer circuit, a sampling circuit, and so forth, each being based on a CMOS circuit, is formed on one substrate. In the case of the close adhesion type image sensor, an integrated circuit such as a sample-and-hold circuit, a shift register circuit, a multiplexer circuit, and so forth, is formed by using the TFTs.

These driving circuits (which are also called "peripheral driving circuits") do not always have the same operating condition. Therefore, the characteristics required for the TFTs are naturally different to certain extents. The pixel unit comprises a pixel TFT functioning as a switching device and an auxiliary holding capacitance, and a voltage is applied to a liquid crystal to drive it. Here, an alternating current must be applied to drive the liquid crystal, and a system called "frame inversion driving" has gained a wide application. Therefore, one of the required characteristics of the TFT is that an OFF current value (a drain current value flowing through the TFT when it is in the OFF operation) must be sufficiently lowered. Because a high driving voltage is applied to the buffer circuit, the TFT must have a high withstand voltage such that it does not undergo breakdown even when a high voltage is applied. In order to improve the current driving capacity, it is necessary to sufficiently secure the ON current value (the drain current value flowing through the TFT when it is in the ON operation).

However, the poly-silicon TFT involves the problem that its OFF current is likely to become high. Degradation such as the drop of the ON current value is observed in the poly-silicon TFT in the same way as in MOS transistors used for ICs, or the like. It is believed that the main cause is hot carrier injection, and the hot carriers generated by a high field in the proximity of the drain presumably invite this degradation.

An LDD (Lightly Doped Drain) structure is known as a structure of the TFT for lowering the OFF current value. This structure forms an impurity region having a low concentration between a channel formation region and a source or drain region to which an impurity is doped in a high concentration. The low concentration impurity region is called the "LDD region".

A so-called "GOLD (Gate-drain Overlapped LDD) structure" is also known as a structure for preventing deterioration of the ON current value by hot carrier injection. Since the LDD region is so arranged as to overlap with a gate wiring through a gate insulation film in this structure, this structure is effective for preventing hot carrier injection in the proximity of the drain and for improving reliability. For example, Mutsuko Hatano, Hajime Akimoto and Takeshi Sakai, "IEDM97 Technical Digest", pp.523-526, 1997, discloses a GOLD structure using side walls formed from silicon. It has been confirmed that this structure provides by far higher reliability than the TFTs having other structures.

In an active matrix type liquid crystal display device, a TFT is disposed for each of dozens to millions of pixels and a pixel electrode is disposed for each TFT. An opposing electrode is provided on an opposing substrate side sandwiching a liquid crystal, and forms a kind of capacitors using the liquid crystal as a dielectric. The voltage to be applied to each pixel is controlled by the switching function of the TFT. As the charge to this capacitor is controlled, the liquid crystal is driven, and an image is displayed by controlling the quantity of transmitting rays of light.

However, the accumulated capacity of this capacitor decreases gradually due to a leakage current resulting from the OFF current, or the like. Consequently, the quantity of transmitting rays of light changes, thereby lowering the contrast of image display. Therefore, it has been customary to dispose a capacitance wiring, and to arrange another capacitor (called a "holding capacitance") in parallel with the capacitor using the liquid crystal as the dielectric in order to supplement the capacitance lost by the capacitor using the liquid crystal as the dielectric.

Nonetheless, the required characteristics of the pixel TFT of the pixel unit are not always the same as the required characteristics of the TFT (hereinafter called the "driving TFT") of a logic circuit (called also the "driving circuit") such as the shift register circuit and the buffer circuit. For example, a large reverse bias voltage (a negative voltage in n-channel TFT) is applied to the gate wiring in the pixel TFT, but the TFT of the driving circuit is not fundamentally driven by the application of the reverse bias voltage. The operation speed of the former may be lower than 1/100 of the latter.

The GOLD structure has a high effect for preventing the degradation of the ON current value, it is true, but is not free from the problem that the OFF current value becomes greater than the ordinary LDD structures. Therefore, the GOLD structure cannot be said as an entirely preferable structure for the pixel TFT, in particular. On the contrary, the ordinary LDD structures have a high effect for restricting the OFF current value, but is not resistant to hot carrier injection, as is well known in the art.

For these reasons, it is not always preferred to constitute all the TFTs by the same construction in the semiconductor devices having a plurality of integrated circuits such as the active matrix type liquid crystal display device.

When a sufficient capacitance is secured by forming a holding capacitance using the capacitance wiring in the pixel unit as represented by the prior art example described above, an aperture ratio (a ratio of an area capable of image display to an area of one pixel) must be sacrificed. Particularly in the case of a small high precision panel used for a projector type display device, the area per pixel is so small that the drop of the aperture ratio by the capacitance wiring becomes a serious problem.

SUMMARY OF THE INVENTION

In order to solve the problems described above, the present invention aims at improving operation performance and reliability of a semiconductor device by optimizing the structures of the TFT used for each circuit of the semiconductor device in accordance with the function of each circuit.

It is another object of the present invention to provide a structure for lowering the area of a holding capacitance provided to each pixel and for improving an aperture ratio in a semiconductor device having a pixel unit.

To accomplish the objects described above, the present invention employs the following constructions. In a semiconductor device including a pixel unit and a driving circuit on the same substrate, the present invention provides a semiconductor device wherein an LDD region of an n-channel TFT forming the driving circuit described above is formed in such a fashion that a part or the whole part thereof overlaps with a gate wiring of the n-channel TFT while sandwiching a gate insulation film between them, and an LDD region of a pixel TFT that forms the pixel unit is formed in such a fashion as not to overlap with a gate wiring of the pixel TFT while sandwiching a gate insulation film.

In addition to the construction described above, the holding capacitance of the pixel unit may comprise a shading film arranged on a resin film, an oxide of the shading film and a pixel electrode. According to this arrangement, the holding capacitance can be formed with an extremely small area and consequently, the aperture ratio of the pixel can be improved.

Another detailed construction according to the present invention is as follows. In a semiconductor device including a pixel unit and a driving circuit on the same substrate, this driving circuit includes a first n-channel TFT formed in such a fashion that the whole part of its LDD region overlaps with a gate wiring while sandwiching a gate insulation film between them, and a second n-channel TFT formed in such a fashion that a part of its LDD region overlaps with a gate wiring while sandwiching a gate insulation film between them, and the pixel unit includes a pixel TFT formed in such a fashion that an LDD region does not overlap with a gate wiring while sandwiching a gate insulation film between them. Needless to say, a holding capacitance of the pixel unit may comprise a shading film disposed on an organic resin film, an oxide of the shading film and a pixel electrode.

In the construction described above, the LDD region of the n-channel TFT forming the driving circuit may contain an element belonging to the Group 15 of the Periodic Table in a concentration higher by 2 to 10 times that of the LDD region of the pixel TFT. The LDD region of the first n-channel TFT may be formed between a channel formation region and a drain region, and the LDD regions of the second n-channel TFT may be so formed as to sandwich the channel formation region between them.

As to a method of fabricating a semiconductor device, the present invention employs the following construction. In a method of fabricating a semiconductor device including a pixel unit and a driving circuit on the same substrate, the method according to the present invention comprises the steps of forming a channel formation region, a source region, a drain region and an LDD region between the drain region and the channel formation region, in an active layer of a first n-channel TFT that forms the driving circuit; forming a channel formation region, a source region, a drain region, an LDD region between the source region and the channel formation region and an LDD region between the drain region and the channel formation region, in an active layer of a second n-channel TFT that forms the driving circuit; forming a channel formation region, a source region and a drain region in an active layer of a p-channel TFT that forms the driving circuit; and forming a channel formation region, a source region, a drain region and an LDD region between the drain region and the channel formation region, in an active layer of a pixel TFT that forms the pixel unit; wherein the LDD region of the first n-channel TFT is formed in such a fashion that the whole part thereof overlaps with the gate wiring of the first n-channel TFT while sandwiching the gate insulation film between them, the LDD region of the second n-channel TFT is formed in such a fashion that a part thereof overlaps with the gate wiring of the first n-channel TFT while sandwiching the gate insulation film between them, and the LDD region of the pixel TFT is so arranged as not to overlap with the gate wiring of the pixel TFT while sandwiching the gate insulation film between them.

As to the fabrication method, the present invention employs the following another construction. In a method of fabricating a semiconductor device including a pixel unit and a driving circuit on the same substrate, the method of the present invention comprises a first step of forming an active layer on a substrate; a second step of forming a gate insulation film in contact with the active layer; a third step of adding an element belonging to the Group 15 of the Periodic Table to an active layer of an n-channel TFT forming the driving circuit, and forming an n^-

region; a fourth step of forming a conductive film on the gate insulation film; a fifth step of patterning the conductive film and forming a gate wiring of a p-channel TFT; a sixth step of adding an element belonging to the Group 13 of the Periodic Table in self-alignment to the active layer of the p-channel TFT with the gate wiring of the p-channel TFT as a mask, and forming a p^{++} region; a seventh step of patterning the conductive film that is not patterned in the fifth step, and forming a gate wiring of the n-channel TFT; an eighth step of adding an element belonging to the Group 15 of the Periodic Table to the active layer of the n-channel TFT, and forming an n^{+} region; and a ninth step of adding an element belonging to the Group 15 of the Periodic Table in self-alignment with the gate wirings of the n- channel TFT and the p-channel TFT as the masks, and forming an n^{--} region.

In a method of fabricating a semiconductor device including a pixel unit and a driving circuit on the same substrate, a further detailed construction of the method of the present invention comprises a first step of a first step of forming an active layer on a substrate; a second step of forming a gate insulation film in contact with the active layer; a third step of adding an element belonging to the Group 15 of the Periodic Table to an active layer of an n-channel TFT forming the driving circuit, and forming an n^{-} region; a fourth step of forming a conductive film on the gate insulation film; a fifth step of patterning the conductive film and forming a gate wiring of a p-channel TFT; a sixth step of adding an element belonging to the Group 13 of the Periodic Table in self-alignment to the active layer of the p-channel TFT with the gate wiring of the p-channel TFT as a mask, and forming a p^{++} region; a seventh step of patterning the conductive film, that is not patterned in the fifth step, and forming a gate wiring of the n-channel TFT; an eighth step of adding an element belonging to the Group 15 of the Periodic Table to the active layer of the n-channel TFT, and forming an n^+ region; and a ninth step of adding an element belonging to the Group 15 of the Periodic Table in self-alignment with the gate wirings of the n-channel TFT and the p-channel TFT as the masks, and forming an n^{--} region.

In the construction described above, the sequence of the process steps for forming the p^{++} region, the n^+ region or the n^{--} region may be changed appropriately. Whichever sequence may be employed, the basic function of the TFT formed finally does not change and the effects of the present invention are not spoiled in any way.

BRIEF DECRIPTION OF THE DRAWINGS

FIGs. 1A to 1C are schematic sectional views showing a fabrication process of a pixel unit and a driving circuit;

FIGs. 2A to 2C are schematic sectional views showing a fabrication process of a pixel unit and a driving circuit;

FIGs. 3A to 3C are schematic sectional views showing a fabrication process of a pixel unit and a driving circuit;

FIG. 4 is schematic sectional view showing a structure of a holding capacitance;

FIGs. 5A to 5C are schematic sectional views showing a fabrication process of a holding capacitance;

FIGs. 6A to 6D are schematic sectional views showing a fabrication process of a pixel unit and a driving circuit;

FIGs. 7A to 7C are schematic sectional views showing a fabrication process of a pixel unit and a driving circuit;

FIGs. 8A to 8C are schematic sectional views showing a fabrication process of a pixel unit and a driving circuit;

FIG. 9 is a sectional structural view showing an active matrix type liquid crystal display device;

FIG. 10 is a perspective view of an active matrix type liquid crystal display device;

FIGs. 11A and 11B are top views of a pixel unit;

FIGs. 12A and 12B are sectional views showing a structure of a holding capacitance;

FIG. 13 is a block circuit diagram of an active matrix type liquid crystal display device;

FIGs. 14A to 14E are sectional views showing a fabrication process of a crystalline semiconductor film;

FIGs. 15A to 15E are sectional views showing a fabrication process of a crystalline semiconductor film;

FIGs. 16A to 16C are schematic sectional views showing a fabrication process of a pixel unit and a driving circuit;

FIGs. 17A and 17B are a sectional view and a top view of a pixel unit;

FIGs. 18A to 18C are schematic sectional views showing a fabrication process of a pixel unit and a driving circuit;

FIGs. 19A to 19C are schematic sectional views showing a fabrication process of a pixel unit and a driving circuit;

FIGs. 20A to 20C are schematic sectional views showing a fabrication process of a pixel unit and a driving circuit;

FIGs. 21A to 21D are schematic sectional views showing a pixel unit and a driving circuit;

FIGs. 22A to 22C are schematic sectional views showing a fabrication process of a pixel unit and a driving circuit;

FIG. 23 is a schematic sectional view showing a structure of a pixel unit and a driving circuit;

FIG. 24 is a circuit diagram showing the construction of an active matrix type EL display device;

FIGs. 25A and 25B are a top view and a sectional view showing the construction of an EL display device;

FIG. 26 is a schematic sectional view showing a sectional structure of an EL display device;

FIGs. 27A and 27B are a schematic view and a wiring diagram showing a top structure of a pixel unit of an EL display device;

FIG. 28 is a schematic sectional view showing a sectional structure of an EL display device;

FIGs. 29A to 29C are circuit diagrams showing the circuit construction of a pixel unit of an EL display device;

FIGs. 30A to 30F are perspective views showing an example of electrical appliances;

FIGs. 31A to 31D are perspective views showing an example of electrical appliances; and

FIGs. 32A and 32B are schematic views showing the construction of an optical engine.

FIG. 33 is a graph showing ID-VG curves and μ_{FE} of an n-channel TFT.

FIG. 34 is a graph showing the relation between degradation rate of the μ_{FE} and the Lov region length of the n-channel TFT.

FIGs. 35A and 35B are graphs showing time dependent change of current consumption and the lowest operation voltage.

FIG. 36 is a graph showing ID-VG curves and μ_{FE} of an n-channel TFT.

FIG. 37 is a graph showing the relation between degradation rate of the μ_{FE} and the Lov region length of the n-channel TFT.

FIGs. 38A and 38B are graphs showing time dependent change of current consumption and the lowest operation voltage.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, preferred embodiments of the present invention will be explained in detail with reference to Examples thereof.

[Example 1]

The first example will be explained with reference to FIGs. 1A to 1C, 2A to 2C and 3A to 3C. A method of simultaneously fabricating TFT of a pixel unit and TFT of a driving circuit disposed around the pixel unit will be explained.

FIG. 1A shows the formation step of active layers and a gate insulation film.

In FIG. 1A, a substrate 101 is preferably made of a glass substrate, a quartz substrate or a plastic substrate (inclusive of a plastic film). A silicon substrate or a metal substrate having an insulation film on the surface thereof can be used, too.

An underlying film 102 that comprises a silicon-containing insulation film (the term "insulation film" generically represents a silicon oxide film, a silicon nitride film and a silicon nitride oxide film in this specification) is formed by a plasma CVD process or a sputtering process to a thickness of 100 to 400 nm on the surface of the substrate 101 on which the TFTs are to be fabricated. The term "silicon nitride oxide film" used in this specification represents an insulation film expressed by the general formula SiO_xN_y (where $0 < x$ and $y < 1$) and containing silicon, oxygen and nitrogen in a predetermined proportion.

In this example, the underlying film 102 has a two-layered structure consisting of a silicon nitride film 102 that has a thickness within the range of 25 to 100 nm and is hereby 50 nm and a silicon oxide film 103 that has a thickness within the range of 50 to 300 nm and is hereby 150 nm. The underlying film 102 is disposed so as to prevent contamination of impurities from the substrate, and need not always be disposed when the quartz substrate is used.

Next, an amorphous silicon film having a thickness of 20 to 100 nm is formed on the underlying film 102 by a known film formation method. The amorphous silicon film is preferably subjected to a dehydrogenation treatment preferably at 400 to 550° C for several hours, though the treatment temperature and time vary depending on the hydrogen content. A crystallization step is preferably carried out after the hydrogen content is lowered to not greater than 5 atomic%. Though the amorphous silicon film may be formed by other fabrication methods such as sputtering and vacuum deposition, impurity elements contained in the film such as oxygen and nitrogen are preferably lowered sufficiently. Because the underlying film and the amorphous silicon film can be formed by the same film formation method, they may be formed hereby continuously. When the underlying film is prevented from being exposed once to the atmospheric air after its formation, surface contamination can be prevented, and variance of characteristics of the resulting TFT can be reduced.

A process step of forming the crystalline silicon film from the amorphous silicon film may use a known laser crystallization technology or thermal crystallization technology. The crystalline silicon film may be formed by the thermal crystallization method using a catalytic element that promotes crystallization of silicon. Besides the amorphous silicon film, a micro-crystalline silicon film may be used or the crystalline silicon film may be directly deposited. Furthermore, the crystalline silicon film may be formed by using the known technology of SOI (Silicon On Insulators) that bonds single crystal silicon onto the substrate.

Unnecessary portions of the crystalline silicon film thus formed are etched away to form island-like semiconductor films (hereinafter called the "active layers") 104, 105 and 106. Boron (B) may be doped in advance in a concentration of about $1x10^{15}$ to $1x10^{17}$ cm^{-3} into regions of the crystalline silicon film where n-channel TFT is to be formed, in order to control a threshold voltage.

Next, a gate insulation film 107 consisting essentially of silicon oxide or silicon nitride as the principal component is so formed as to cover the active layers 104, 105 and 106. The gate insulation film 107 is formed to a thickness of 10 to 200 nm, preferably 50 to 150 nm. For example, a silicon nitride oxide film is formed by a plasma CVD process to a thickness of 75 nm from N_2O and SiH_4 as the starting materials. This film is then oxidized thermally at 800 to 1,000° C in an oxygen atmosphere or in a mixed atmosphere of oxygen and hydrochloric acid, giving a 115 nm-thick gate insulation film.

FIG. 1B shows the formation of an n^- region.

Resist masks 108, 109, 110 and 111 are formed over the surface of the active layers 104 and 106, the entire surface of the regions in which wiring is to be formed, and over a part of the active layer 105 (inclusive of the region which is to serve as the channel formation region). An n-type imparting impurity element is added to form a low concentration impurity region 112. This low concentration impurity region 112 is the impurity region for forming later an LDD region (which is called the "Lov region" in this specification with "ov" representing "overlap") that overlaps with the gate wiring through the gate insulation film beneath the n-channel TFT of a CMOS circuit. The concentration of the impurity element for imparting the n-type that is contained in the resulting low concentration impurity region, is expressed by "n^-". Therefore, the low concentration impurity region 112 can be paraphrased to the "n^- region" in this specification.

In this example, phosphorus is added by ion doping that excites phosphine (PH_3) by plasma excitation without executing mass separation. An ion implantation method that executes mass separation may be used naturally. In this process step, phosphorus is added to the semiconductor layer beneath the gate insulation film 107 through this film 107. The phosphorus concentration to be doped is preferably within the range of $2x10^{16}$

to 5×10^{19} atoms/cm^3, and is hereby 1×10^{18} atoms/cm^3.

After the resist masks 108, 109, 110 and 111 are removed, heat-treatment is carried out at 400 to 900°C, preferably 550 to 800°C, for 1 to 12 hours in a nitrogen atmosphere so as to activate phosphorus that is doped. This activation may be effected by irradiating a laser beam. Though this process step can be omitted, a higher activation ratio can be expected if this step is conducted.

FIG. 1C shows the formation of conductive films for gate wirings.

A first conductive film 113 is formed to a thickness of 10 to 100 nm by using an element selected from the group consisting of tantalum (Ta), titanium (Ti), molybdenum (Mo) and tungsten (W), or conductive materials of any of these elements as the principal component. Tantalum nitride (TaN) or tungsten nitride (WN), for example, is preferably used for the first conductive film 113.

A second conductive film 114 is formed to a thickness of 100 to 400 nm on the first conductive film 113 by using an element selected from the group consisting of Ta, Ti, Mo and W, or a conductive material of any of these elements as the principal component. For example, Ta may be formed to a thickness of 200 nm. It is hereby effective to form a silicon film to a thickness of about 2 to 20 nm beneath the first conductive film 113 or on the second conductive film 114 in order to prevent oxidation of the conductive films 113 and 114 (particularly, the conductive film 114).

FIG. 2A shows the formation of a p-channel gate wiring and the formation of p^{++} regions.

After resist masks 115, 116, 117 and 118 are formed, the first conductive film and the second conductive film (which will be handled hereinafter as a laminate film) are etched, giving a gate wiring 119 (also called the "gate electrode") of the p-channel TFT and gate wirings 120 and 121. Incidentally, the conductive films 122 and 123 are left non-etched in such a manner as to cover the entire surface of the region that is to serve as the n-channel TFT.

The resist masks 115, 116, 117 and 118 are left as the masks, and a process step of doping an impurity element for imparting the p-type is carried out for a part of the semiconductor layer 104 at which the p-channel TFT is formed. Boron is used hereby as the impurity element and is doped by an ion doping method using diborane (B_2H_6). (Needless to say, an ion implantation method may be employed, too.) In this instance, boron is doped in a concentration of $5x10^{20}$ to $3x10^{21}$ atoms/cm^3. Incidentally, the concentration of the p-type imparting impurity element contained in the resulting impurity region is hereby expressed as "p^{++}". Therefore, the impurity regions 124 and 125 can be paraphrased to the "p^{++} regions" in this specification.

Incidentally, in this process step, a process step may be carried out which etches away the gate insulation film 107 using the resist masks 115, 116, 117 and 118 to expose a part of the active layer 104 and then adds the p-type imparting impurity element. In this case, since the acceleration voltage may be low, damage to the active layer is small, and throughput can be improved.

FIG. 2B shows the formation of n-channel gate wirings.

After the resist masks 115, 116, 117 and 118 are removed, resist masks 126, 127, 128 and 129 are formed, and gate wirings 130 and 131 of the n-channel TFT are formed. At this time, the gate wiring 130 is formed in such a manner as to overlap with the n^- region 112 through the gate insulation film 107.

FIG. 2C shows the formation of n^+ regions.

The resist masks 126, 127, 128 and 129 are removed, and resist masks 132, 133 and 134 are formed afresh. A process step of forming an impurity region, that is to function as a source or drain region in each n-channel TFT, is carried out. The resist mask 134 is formed in such a manner as to cover the gate wiring 131 of the n-channel TFT to form the LDD region in such a manner that the gate wiring does not overlap with the n-channel TFT of the pixel unit in a subsequent process step.

An n-type imparting impurity element is added to form impurity regions 135, 136, 137, 138 and 139. Here, the ion doping method that uses phosphine (PH_3) is employed. (Needless to say, the ion implantation method may be employed, as well.) The phosphorus concentration in this region is $1x10^{20}$ to $1x10^{21}$ atoms/cm^3. The concentration of the n-type imparting impurity element contained in the impurity regions 137, 138 and 139 is hereby expressed as "n^+". Therefore, the impurity regions 137, 138 and 139 in this specification can be paraphrased to the "n^+ regions". Strictly speaking, since the n^- region has been formed already, the impurity region 135 contains phosphorus in a somewhat higher concentration than the impurity regions 136, 137, 138 and 139.

In this process step, a step of adding the n-type imparting impurity element may be conducted after the gate insulation film 107 is etched using the resist masks 132, 133 and 134 and the gate wiring 130 as the masks to expose a part of the active layers 105 and 106. In this case, since the acceleration voltage may be low, damage to the active layer is small and throughput can be improved.

FIG. 3A shows the formation of n^{--} regions.

The resist masks 132, 133 and 134 are removed, and a process step of adding an n-type imparting impurity element to the active layer 106, that is to serve as the n-channel TFT, is carried out. The impurity regions 140, 141, 142 and 143 thus formed contain phosphorus in a concentration of 1/2 to 1/10 (more concretely, 1×10^{16} to 5×10^{18} atoms/cm^3) of the n^- region described above. Incidentally, the concentration of the n-type imparting impurity element contained in these impurity regions 140, 141, 142 and 143 is hereby expressed by "n^{--}". Therefore, the impurity regions 140, 141, 142 and 143 can be paraphrased to the "n^{--} regions" in this specification. In this process step, phosphorus is added in the concentration of n^{--} into all the impurity regions except for the impurity region 167 that is hidden by the gate wiring. However, this concentration n^{--} can be neglected because it is extremely low.

FIG. 3B shows a thermal activation step.

A protective insulation film 144, that is to serve later as a first inter-layer insulation film, is formed. The protective insulation film 144 may be a silicon nitride film, a silicon oxide film, a silicon nitride oxide film or their laminate film. The film thickness may be within the range of 100 to 400 nm.

A heat-treatment step is carried out in order to activate the n-type or p-type imparting impurity element added in each concentration. This process step can be conducted by a furnace annealing method, a laser annealing method, or a rapid thermal annealing method (RTA). This example uses the furnace annealing method. The heat-treatment is carried out in a nitrogen atmosphere at 300 to 650° C, preferably 400 to 550° C, and hereby 450° C, for 2 hours.

A heat-treatment is further carried out in an atmosphere containing 3 to 100% hydrogen at 300 to 450° C for 1 to 12 hours so as to hydrogenate the active layer. This is the process step for terminating the dangling bonds of the semiconductor layer by hydrogen that is heated and excited. Plasma hydrogenation (using hydrogen that is excited by plasma) may be employed as another means for hydrogenation.

FIG. 3C shows the formation of inter-layer insulation films, source/drain wirings, a shading film, a pixel electrode and a holding capacitance.

After the activation step is completed, a 0.5 to 1.5 µm-thick inter-layer insulation film 145 is formed on the protective insulation film 144. A laminate film comprising the protective insulation film 144 and the inter-layer insulation film 145 is used as the first inter-layer insulation film.

Thereafter, contact holes reaching the source or drain regions of the TFT are bored, and source wirings 146, 147 and 148 and drain wirings 149 and 150 are formed. In this example, the source wirings and the drain wirings comprise a three-layered laminate film that is formed continuously by sputtering a Ti film having a thickness of 100 nm, a Ti-containing aluminum film having a thickness of 300 nm and a Ti film having a thickness of 150nm. Incidentally, a laminate film of a copper film and a titanium nitride film may be used as the source wirings and the drain wirings.

Next, a silicon nitride film, a silicon oxide film or a silicon nitride oxide film is formed as a passivation film 151 to a thickness of 50 to 500 nm (typically, 200 to 300 nm). When hydrogenation treatment is carried out under this condition, desired results can be obtained for improving characteristics of the TFT. Similar effects can be obtained, for instance, when heat-treatment is carried out in an atmosphere containing 3 to 100% hydrogen at 300 to 450° C for 1 to 12 hours, or by the plasma hydrogenation method. Open portions may be formed in the passivation film 151 at positions where contact holes for connecting the pixel electrodes to the drain wirings are to be later formed.

Next, a second inter-layer insulation film 152 made of an organic resin is formed to a thickness of about 1 µm. Polyimide, acrylic, polyamide, polyimideamide, BCB (benzocyclobutene), etc. can be used as the organic resin. The advantages brought forth by using the organic resin film are that the film formation method is simple, the parasitic capacitance can be reduced because a specific dielectric constant is low, and planarity is high. Organic resin films other than those described above and organic SiO compounds can be used, too. This example uses polyimide of the type that can be polymerized thermally after the application to the substrate, and the film is formed by firing at 300° C.

Next, the shading film 153 is formed on the second inter-layer insulation film 152 in the region that is to serve as the pixel unit. The shading film 153 is made of the element selected from the group consisting of aluminum (Al), titanium (Ti) and tantalum (Ta), or a material containing any of them as the principal component, and the film is formed to a thickness of 100 to 300 nm. An oxide (oxide film) 154 is formed to a thickness of 30 to 150 nm (preferably, 50 to 75 nm) on the surface of the shading film 153 by an anodic oxidation method or a plasma oxidation method. This example uses the aluminum film or the film consisting essentially of aluminum as the principal component for the shading film 153 and the aluminum oxide film (alumina film) for the oxide 154.

Though the insulation film is deposited only to the surface of the shading film in this example, the insulation film may be formed by the gaseous phase method such as the plasma CVD method, the thermal CVD method or the sputtering method. In such a case, too, the film thickness is preferably 30 to 150 nm (preferably, 50 to 75 nm). A silicon oxide film, a silicon nitride film, a silicon nitride oxide film, a DLC (Diamond-like Carbon) film or an organic resin film may be used. Furthermore, a laminate film combining these films may be used, too.

Next, contact holes reaching the drain wiring 150 are formed in the second inter-layer insulation film 152, thereby forming a pixel electrode 155. Incidentally, pixel electrodes 156 and 157 are the pixel electrodes of other adjacent pixels. The pixel electrodes 155, 156 and 157 are formed of a transparent conductive film in the case of fabricating a transmission type liquid crystal display device, and are formed of a metal film in the case of fabricating a reflection type liquid crystal display device. Here, a film consisting essentially of a compound between indium oxide and tin oxide (called "ITO") is fabricated by sputtering to a thickness of 100 nm in order to obtain the transmission type liquid crystal display device.

At this time, the region 158 at which the pixel electrode 155 and the shading film 153 overlap with each other through the oxide 154 constitutes a holding capacitance.

In this way, the CMOS circuit for forming the driving circuit and the active matrix substrate having the pixel unit are completed on the same substrate. Incidentally, the n-channel TFT 181 and the p-channel TFT 182 are formed in the CMOS circuit that constitutes the driving circuit, and the pixel TFT 183 comprising the n-channel TFT is formed in the pixel unit.

In the p-channel TFT 181 of the CMOS circuit, the channel formation region 161, the source region 162 and the drain region 163 are formed. Each of the source region 162 and the drain region 163 is formed of the p^{++} region. In the n-channel TFT 182, the channel formation region 164, the source region 165, the drain region 166 and the LDD region (Lov region) 167 that wholly overlaps with the gate wiring through the gate insulation film are formed. At this time, the source region 165 and the drain region 166 are the n^{+} regions, and the Lov region 167 is the n^{-} region. More strictly, the drain region 166 is a (n^{-} +

n^+) region.

Referring to FIG. 3C, the Lov region is shown disposed only on one side of the channel formation region 164 (only on the drain region side) in order to reduce the resistance component as much as possible. However, the Lov region may be disposed on both sides while sandwiching the channel formation region 164 between them.

Formed in the pixel TFT 183 are the channel formation regions 168 and 169, the source region 170, the drain region 171, the LDD regions not overlapping with the gate wiring through the gate insulation film (this LDD region will be called hereinafter the "Loff region"; "off" represents hereby "offset") 172, 173, 174 and 175, and the n^+ region 176 (which is effective for reducing the OFF current value) that keeps contact with the Loff regions 173 and 174. At this time, the source region 170 and the drain region 171 comprise the n^+ region, respectively, and the Loff regions 172, 173, 174 and 175 comprise the n^{--} region, respectively.

This invention can optimize the structure of the TFT for forming each circuit in accordance with the circuit specification required by the pixel unit and by the driving circuit, and can improve operation performance of the semiconductor device and its reliability. Speaking more concretely, the arrangement of the LDD regions is rendered different for the n-channel TFTs in accordance with the circuit specification, and the TFT structure making the most of the high speed operation or the countermeasure for the hot carrier and the TFT structure making the most of the low OFF current operation are accomplished on the same substrate because the Lov regions and the Loff regions are skillfully arranged.

In the case of the active matrix type liquid crystal display device, for example, the n-channel TFT 182 is suitable for a logic circuit such as a shift register circuit, a frequency division circuit, a signal division circuit, a level shifter circuit or a buffer circuit, for which the high speed operation is of importance. The n-channel TFT 183 is suitable for the pixel unit, a sampling circuit (called also a "transfer gate"), etc, for which the low OFF current operation is of importance.

The length (width) of the Lov region is from 0.5 to 3.0 µm for the channel length of 3 to 7 µm, typically 1.0 to 1.5 µm. The length (width) of the Loff regions 172, 173, 174 and 175 disposed in the pixel TFT 183 is 0.5 to 3.5 µm, typically 2.0 to 2.5 µm.

[Example 2]

In this example, another structure of the holding capacitance connected to the n-channel TFT 401 of the pixel unit of the active matrix substrate will be explained with reference to FIG. 4. Incidentally, the sectional structure shown in FIG. 4 is entirely the same as that of Example 1 up to the process step of forming the oxide 154, and the structure up to this step has been explained already with reference to FIGs. 1A to 1C, 2A to 2C and 3A to 3C. Therefore, only the difference of this example from Example 1 will be explained.

After the shading film 153 and the oxide 154 obtained by oxidizing the shading film 153 are formed in accordance with the process steps of Example 1, spacers 402, 403 and 404 comprising an organic resin film are formed. A film selected from the group consisting of polyimide, polyamide, polyimideamide, acrylic and BCB (benzocyclobutene) can be used for the organic resin film. Thereafter, the spacer 402, the second inter-layer insulation film 152 and the passivation film 151 are etched to form contact holes, and the pixel electrode 405 is formed using the same material as that of Example 1. Incidentally, the pixel electrodes 406 and 407 are the pixel electrodes of other adjacent pixels.

In this way, the holding capacitance 408 is formed in the region where the shading film 153 and the pixel electrode 405 overlap with each other through the oxide 154. Because the spacers 402, 403 and 404 are disposed in the manner described above, short-circuit that would otherwise occur between the shading film 153 and each pixel electrode 405, 406 and 407 can be prevented.

Incidentally, the construction of this example can be combined with the construction of Example 1.

[Example 3]

In this example, still another structure of the holding capacitance connected to the n-channel TFT of the pixel unit of the active matrix substrate will be explained with reference to FIGs. 5A to 5C. Incidentally, the sectional structure shown in FIGs. 5A to 5C is exactly the same as that of Example 1 up to the process step of forming the shading film 153, and the structure up to this process step has been explained already with reference to FIGs. 1A to 1C, 2A to 2C and 3A to 3C. Therefore, only the difference of this example from Example 1 will be explained.

After the shading film 153 is formed in accordance with the process steps of Example 1, spacers 501, 502 and 503 comprising an organic resin film are formed in such a manner as to cover the end portions of the shading film 153. A film selected from the group consisting of polyimide, polyamide, polyimideamide, acrylic and BCB (benzocyclobutene) can be used for the organic resin film (FIG. 5A).

Next, an oxide 504 is formed on the exposed surface of the shading film 153 by the anodic oxidation method or the plasma oxidation method. Incidentally, the oxide 504 is not formed at the contact portions with the spacers 501, 502 and 503 (FIG.

5B).

Next, the spacer 501, the second inter-layer insulation film 152 and the passivation film 151 are etched to form a contact hole, and a pixel electrode 505 is formed using the same material as that of Example 1. The pixel electrodes 506 and 507 are the pixel electrodes of other adjacent pixels.

In this way, the holding capacitance 508 is formed in the region where the shading film 153 and the pixel electrode 505 overlap with each other through the oxide 504. Because the spacers 501, 502 and 503 are provided, short-circuit that would otherwise occur between the shading film 153 and each pixel electrode 505, 506 and 507 can be prevented.

Incidentally, the construction of this example can be combined with the construction of Example 1.

[Example 4]

In this example, a method of fabricating an active matrix substrate having a pixel unit and a CMOS circuit as the basic form of a driving circuit disposed in the periphery of the pixel unit, that are formed simultaneously, will be explained with reference to FIGs. 6A to 6D, 7A to 7C and 8A to 8C.

To begin with, a silicon nitride oxide film 602a is formed as an underlying film on a substrate 601 to a thickness of 50 to 500 nm, typically 100 nm. The silicon nitride oxide film 602a is formed using SiH_4, N_2O, and NH_3 as the starting material gas, and the nitrogen concentration of this film is adjusted to at least 25 atomic% to less than 50 atomic%. Heat-treatment is then carried out in a nitrogen atmosphere at 450 to 650° C in order to render the silicon nitride oxide film 602a compact.

A silicon nitride oxide film 602b is further formed to a thickness of 100 to 500 nm, typically 200 nm, and an amorphous semiconductor film (not shown) is continuously formed to a thickness of 20 to 80 nm. This example uses an amorphous silicon film for the amorphous semiconductor film, but a micro-crystalline silicon film or an amorphous silicon-germanium film may be used, as well.

The amorphous silicon film is then crystallized by crystallization means described in Japanese Patent Laid-Open No. 7-130652 (corresponding to U.S. Patents No. 5,643,826 and 5,923,962), forming a crystalline silicon film that is not shown. The technology disclosed in this prior art reference is the crystallization means that uses catalytic elements for promoting crystallization (at least one member selected from the group consisting of nickel, cobalt, germanium, tin, lead, palladium, iron and copper; typically nickel) for crystallizing the amorphous silicon film. More concretely, the reference invention conducts heat-treatment under the condition where the catalytic element is supported on the surface of the amorphous silicon film to convert the amorphous silicon film to the crystalline silicon film.

After the crystalline silicon film is formed in this way, the remaining amorphous component is crystallized as an excimer laser beam is radiated to improve crystallinity of the entire film. Incidentally, the excimer laser beam may be of a pulse oscillation type or a continuous oscillation type. When the beam is processed into a linear shape and radiated, a large substrate can be processed, too.

Next, the crystalline silicon film is patterned to form active layers 603, 604, 605 and 606, and a gate insulation film 607 is so formed as to cover these active layers 603 to 606. The gate insulation film 607 is a silicon nitride oxide film prepared from SiH_4 and N_2O, and is formed to a thickness of 10 to 200 nm, preferably 50 to 150 nm (FIG. 6A).

Resist masks 608, 609, 610 and 611 are then formed in such a fashion as to cover the entire surface of the active layers

603 and 606 and a part of the active layers 604 and 605 (inclusive of the channel formation region). After an n-type imparting impurity element (phosphorus in this example) is doped by the ion doping method that uses phosphine (PH_3), n^- regions 612, 613 and 614 that are to serve as the Lov region or the Loff region are formed. Since phosphorus is added to the active layers beneath the gate insulation film 607 through this film 607, an acceleration voltage is set to 65 keV. The concentration of phosphorus added to the active layers is preferably within the range of $2x10^{16}$ to $5x10^{19}$ atoms/cm^3, and is hereby $1x10^{18}$ atoms/cm^3 (FIG. 6B).

Next, tantalum nitride (TaN) is sputtered to form a first conductive film 615. Subsequently, a second conductive film 616 consisting essentially of aluminum (Al) as the principal component is formed to a thickness of 100 to 300 nm (FIG. 6C).

The second conductive film 616 is etched to form a wiring 617. Since the second conductive film is made of Al in this example, a selection ratio to the TaN film as the underlying film by a phosphoric acid solution is excellent. A third conductive film 618 of tantalum (Ta) is formed to a thickness of 100 to 400 nm (to 200 nm in this example) over the first conductive film 615 and the wiring 617. A tantalum nitride film may be formed further on this tantalum film 618 (FIG. 6D).

Next, resist masks 619, 620, 621, 622, 623 and 624 are formed. A part of the first and third conductive films is etched away to form a connection wiring 625 having a low resistance, a gate wiring 626 of the p-channel TFT and a gate wiring 627 of the pixel unit. The conductive films 628, 629 and 630 are left on the region that is to serve as the n-channel TFT. The connection wiring 625 is formed at a portion at which the wiring resistance is minimized (for example, a wiring portion from input/output terminals of external signals to input/output terminals of the driving circuit). Because the wiring width becomes great to a certain extent from the structural limitation, the connection wiring is not suitable for the portion that requires a miniature wiring.

The first conductive film (TaN film) and the second conductive film (Ta film) can be etched by a mixed gas of CF_4 and O_2. While the resist masks 619, 620, 621, 622, 623 and 624 are left as they are, a process step of doping a p-type imparting impurity element to a part of the active layer 603 at which the p-channel TFT is formed. Here, boron is used as the impurity element, and ion doping using diborane (B_2H_6) is carried out. (Needless to say, ion implantation can be used, too.) The boron concentration is $5\text{x}10^{20}$ to $3\text{x}10^{21}$ atoms/cm^3 ($2\text{x}10^{21}$ atoms/cm^3 in this example). In this way, there are formed p^{++} regions 631 and 632 containing boron in a high concentration (FIG. 7A).

In this process step, it is also possible to conduct the process step that etches the gate insulation film 107 using the resist masks 619, 620, 621, 622, 623 and 624 as the mask to expose a part of the active layer 603 and then to add boron. In this case, since the acceleration voltage may be low, damage to the active layer is small and throughput can be improved.

Next, after the resist masks 619, 620, 621, 622, 623 and 624 are removed, resist masks 633, 634, 635, 636, 637 and 638 are formed afresh. They are for forming the gate wiring of the n-channel TFTs, and gate wirings 639, 640 and 641 of the n-channel TFTs are formed. At this time, the gate wirings 639 and 640 are formed in such a manner as to overlap with a part of the n^- regions 612, 613 and 614 (FIG. 7B).

Next, after the resist masks 633, 634, 635, 636, 637 and 638 are removed, resist masks 642, 643, 644, 645, 646 and 647 are formed afresh. The resist masks 644 and 646 are so formed as to cover the gate wirings 640 and 641 and a part of the n^-

regions 612, 613 and 614.

An n-type imparting impurity element (phosphorus in this example) is added in a concentration of $1x10^{20}$ to $1x10^{21}$ atoms/cm^3 ($5x10^{20}$ atoms/cm^3 in this example) to form n^+ regions 647, 648, 649, 650, 651, 652 and 653 in the active layers 604, 605 and 606 (FIG. 7C).

In this process step, it is also possible to conduct a process step that etches away the gate insulation film 107 using the resist masks 642, 643, 644, 645, 646 and 647 to expose a part of the active layers 604, 605 and 606 and then adds phosphorus. In this case, since the acceleration voltage may be low, damage to the active layers is small and throughput can be improved.

After the resist masks 642, 643, 644, 645 and 646 are removed, a process step of adding an n-type imparting impurity element (phosphorus in this example) to the active layer 606, that is to serve as the n-channel TFT of the pixel unit, is carried out. In this way, n^{--} regions 654, 655, 656 and 657 to which phosphorus is added in a concentration of 1/2 to 1/10 (concretely, $1x10^{16}$ to $5x10^{18}$ atoms/cm^3) of the concentration of the n^- region are formed (FIG. 8A).

In this process step, phosphorus is added in the concentration of n^{--} to all the impurity regions other than the impurity regions 658, 659 and 660 that are hidden by the gate wiring. In practice, the concentration of n^{--} is so low that it may be neglected. Strictly speaking, however, the regions represented by reference numerals 659 and 660 are the n^- regions whereas the regions represented by reference numerals 661 and 662 are the ($n^- + n^{--}$) regions that contain phosphorus in a somewhat higher concentration than the n^- regions 659 and 660.

Next, a protective insulation film 663 having a thickness of 100 to 400 nm is formed with a silicon nitride oxide film that is formed by the plasma CVD method using SiH_4, N_2O and NH_3

as the starting materials. This silicon nitride oxide film is preferably formed so that its hydrogen concentration is 1 to 30 atomic%. A silicon oxide film, a silicon nitride film and their laminate film may be used for the protective insulation film 663.

Thereafter, a heat-treatment step is carried out so as to activate the n-type or p-type imparting impurity element added in a respective concentration. This step can be carried out in accordance with the furnace annealing method, the laser annealing method or the rapid thermal annealing method (RTA method). This example employs the furnace annealing method for the activation treatment. The heat-treatment is carried out in a nitrogen atmosphere at 300 to 650° C, preferably 400 to 550° C, and at 450° C in this example, for 2 hours.

A heat-treatment is further carried out in an atmosphere containing 3 to 100% hydrogen, at 300 to 450° C for 1 to 12 hours so as to hydrogenate the active layers. This is the step that terminates the dangling bonds of the semiconductor layer by hydrogen that is thermally excited. Plasma hydrogenation (using hydrogen that is excited by plasma) may be used as another hydrogenation means (FIG. 8B).

After the activation step is completed, a 0.5 to 1.5 μm-thick inter-layer insulation film 664 is formed on the protective insulation film 663. A laminate film comprising the protective insulation film 663 and the inter-layer insulation film 664 is used as the first inter-layer insulation film.

Contact holes reaching the source region or the drain region of the respective TFT are bored, and the source wirings 665, 666, 667 and 668 and the drain wirings 669, 670, 671 and 672 are formed. Incidentally, the drain wirings 669 and 670 are connected as the same wiring in order to form the CMOS circuit, though they are not shown in the drawings. Connection wirings

673 and 674 that connect the input/output terminals with one another and circuits with one another are formed simultaneously. These wirings in this example comprise a laminate film having a three-layered structure of a 100 nm-thick Ti film, a 300 nm-thick Ti-containing aluminum film and a 150 nm-thick Ti film that are continuously formed by sputtering, though this laminate film is not shown in the drawings.

Next, a passivation film 675 is constituted by a silicon nitride film, a silicon oxide film or a silicon nitride oxide film each having a thickness of 50 to 500 nm (typically, 200 to 300 nm). This passivation film 675 may be formed from the silicon nitride oxide film prepared from SiH_4, N_2O and NH_3 by plasma CVD, or a silicon nitride film prepared from SiH_4, N_2 and NH_3.

Prior to the formation of the film, a hydrogenation step is carried out by a plasma hydrogenation treatment by introducing N_2O, N_2, NH_3, or the like. Hydrogen that is excited by this plasma treatment is supplied into the first inter-layer insulation film. As the substrate is heated to 200 to 400° C, hydrogen can be diffused into the lower layer side, too, and the active layers can be thus hydrogenated. The fabrication condition of the passivation film is not particularly restrictive, but the film is preferably a close film.

The hydrogenation step may be further carried out after the passivation film is formed. Similar effects can be obtained by, for example, carrying out heat-treatment in an atmosphere containing 3 to 100% hydrogen at 300 to 450° C for 1 to 12 hours, or by the plasma hydrogenation method. In this instance, openings may be formed in the passivation film 151 at positions where contact holes for connecting the pixel electrodes to the drain wiring are to be formed afterwards.

A second inter-layer insulation film 676 made of an organic resin is then formed to a thickness of about 1 μm. Polyimide, acrylic, polyamide, polyimideamide or BCB (benzocyclobutene) can be used as the organic resin. The advantages brought forth by the use of the organic resin film are that the formation method of the film is simple, the parasitic capacitance can be reduced because the specific dielectric constant is low, and planarity is high. Organic resin films other than those described above and organic SiO compounds can be used, too. This example uses polyimide of the type that is thermally polymerized after being applied to the substrate, and the film is fabricated by firing the resin at 300° C.

Next, a shading film 677 is formed on the second inter-layer insulation film 676 in a region that is to serve as the pixel unit. The shading film 153 is a film made of the element selected from the group consisting of aluminum (Al), titanium (Ti) and tantalum (Ta), or a film consisting of any of these elements as the principal component. The film is formed to a thickness of 100 to 300 nm. If an insulation film such as silicon oxide film is formed to a thickness of 5 to 50 nm on the second inter-layer insulation film 676, adhesion of the shading film to be formed on the second inter-layer insulation film 676 can be improved. If a plasma treatment using a CF_4 gas is applied to the surface of the second inter-layer insulation film 676 made of the organic resin, adhesion of the shading film to be formed on this film 676 can be improved through surface modification.

Other connection wiring can be formed besides the shading film. For example, the connection wiring for connecting circuits with one another inside the driving circuit can be formed. In this case, however, the contact holes must be bored in advance before the materials for shaping the shading film or the connection wiring are formed.

Next, an anodic oxide 678 is formed on the surface of the shading film 677 to a thickness of 30 to 150 nm (preferably, 50 to 75 nm) by an anodic oxidation method or a plasma oxidation method (by the anodic oxidation method in this example). Since this example uses an aluminum film or a film consisting essentially of aluminum as the principal component for the shading film 677, an aluminum oxide film (alumina film) is formed as the anodic oxide 678.

To conduct the anodic oxidation treatment, an ethylene glycol tartrate solution having a sufficiently low alkali ion concentration is first prepared. This is the solution prepared by mixing a 15% aqueous ammonium tartrate solution with ethylene glycol at a mixing ratio of 2:8, and aqueous ammonia is added to this solution to adjust the pH to 7 ± 0.5. A platinum electrode to serve as a cathode is dipped into this solution, and the substrate having the shading film 677 formed thereon is then immersed. A predetermined DC current (several to dozens of mA) is applied with the shading film 677 as the anode. The voltage between the cathode and the anode in the solution changes with time and with the growth of the oxide. However, the voltage is regulated so that the current remains constant, and the voltage is kept constant at the point when the voltage reaches 150 V. This constant voltage is kept for 15 minutes. In this way, an anodic oxide having a thickness of 50 to 75 nm can be formed on the surface of the shading film 677. Incidentally, the numerical values relating to the anodic oxidation method illustrated hereby are merely illustrative, and the optimum values naturally change in accordance with the size of the device to be fabricated, and other factors.

This example employs the construction in which the insulation film is disposed only on the surface of the shading film. However, the insulation film may be formed by the gaseous phase method such as the plasma CVD method, the thermal CVD method or the sputtering method. In such a case, too, the film thickness is 30 to 150 nm (preferably, 50 to 75 nm). The insulation film may use a silicon oxide film, a silicon nitride film, a silicon nitride oxide film, a DLC (Diamond-Like Carbon) film or an organic resin film. Furthermore, a laminate film of these films may be also used.

Next, contact holes reaching the drain wiring 672 are bored in the second inter-layer insulation film 676 and the passivation film 675 so as to form the pixel electrode 679. Incidentally, pixel electrodes 680 and 681 are the pixel electrodes of other adjacent pixels. A transparent conductive film is used as the pixel electrodes 679, 680 and 681 when a transmission type liquid crystal display device is fabricated. A metal film is used as the pixel electrodes when a reflection type liquid crystal display device is fabricated. In this example, a film of a compound of indium oxide and tin oxide (ITO) is formed to a thickness of 100 nm by sputtering to fabricate the transmission type liquid crystal display device.

At this time, a region in which the pixel electrode 679 and the shading film 677 overlap with each other through the anodic oxide 678 forms the holding capacitance.

In this way, the active matrix substrate having the CMOS circuit to serve as the driving circuit and the pixel unit on the same substrate is completed. In the driving circuit are formed the p-channel TFT 801 and the n-channel TFTs 802 and 803, and in the pixel unit is formed the pixel TFT 804 comprising the n-channel TFT (FIG. 8C).

In the p-channel TFT 801 of the CMOS circuit, the channel formation region 701, the source region 702 and the drain region 703 are formed. Each of the source region 702 and the drain region 703 is formed of the p^{++} region.

In the n-channel TFT 802 are formed the channel formation region 704, the source region 705, the drain region 706, and the Lov region 707 on one of the sides of the channel formation region. At this time, the source region 705 and the drain region 706 are formed of the ($n^- + n^+$) region, and the Lov region 707 is formed of n^- region. The Lov region 707 is formed in such a manner as to fully overlap with the gate wiring.

In the n-channel TFT 803 are formed the channel formation region 708, the source region 709, the drain region 710, and the Lov regions 711a, 712a and the Loff regions 711b and 712b on both sides of the channel formation region. In this instance, the source region 709 and the drain region 710 are formed of the ($n^- + n^+$) region, respectively. The Lov regions 711a and 712a are formed of the n^- region, and the Loff regions 711b and 712b are formed of the ($n^{--} + n^-$) region. According to this construction, the Lov regions and the Loff regions are accomplished because a part of the LDD region is so arranged as to overlap with the gate wiring.

In the pixel TFT 804 are formed the channel formation regions 713 and 714, the source region 715, the drain region 716, the Loff regions 717, 718, 719 and 720 and the n^+ region 721 keeping contact with the Loff regions 718 and 719. At this time, the source region 715 and the drain region 716 are formed of the n^+ region, respectively, and the Loff regions 717, 718, 719 and 720 are formed of the n^{--} region.

This example optimizes the structure of the TFTs for forming each circuit in accordance with the circuit specifications required for the pixel unit and for the driving circuit, and can improve operation performance and reliability of the semiconductor device. More concretely, the LDD region of the n-channel TFT is arranged in a different way in accordance with the circuit specification, and the TFT structure that lays stress on the high-speed operation or on the countermeasure against the hot carriers, and the TFT structure that lays stress on the low OFF current operation, are accomplished on the same substrate.

When the active matrix type liquid crystal display device is considered, for example, the n-channel TFT 802 is suitable for the logic circuit that requires the high speed operation such as a shift register circuit, a frequency division circuit, a signal division circuit, a level shifter circuit and a buffer circuit. In other words, the n-channel TFT employs the structure that arranges the Lov region only on one of the sides (the drain region side) of the channel formation region, and thus lays stress on the countermeasure against the hot carrier while the resistance component is reduced as much as possible. This is because the function of the source region is the same as that of the drain region in the group of the circuits described above and the moving direction of the carriers (electrons) is constant. However, the Lov regions can be arranged on both sides of the channel formation region, whenever necessary.

The n-channel TFT 803 is suitable for a sampling circuit (sample-and-hold circuit) that requires both of the countermeasure against the hot carriers and the low OFF current operation. In other words, the countermeasure against the hot carriers is achieved as the Lov region is disposed and the low OFF current operation is achieved as the Loff region is disposed. In the sampling circuit, the function of the source region is reversed to that of the drain region and the moving direction of the carriers changes by 180° . Therefore, the structure must have symmetry of line with the gate wiring as the center. Incidentally, only the Lov region is disposed depending on cases.

The n-channel TFT 804 is suitable for the pixel unit and the sampling circuit (sample-and-hold circuit) that lays stress on the low OFF current operation. In other words, the Lov region that might increase the OFF current value is not disposed but only the Loff region is disposed so as to attain the low OFF current operation. The LDD region having a lower concentration than that of the LDD region of the driving circuit is used as the Loff region so that even when the ON current value drops to a certain extent, the OFF current value can be reduced as much as possible. Furthermore, it has been confirmed that the n^+ region 721 is extremely effective for reducing the OFF current value.

The length (width) of the Lov region 707 of the n-channel TFT 802 may be 0.5 to 3.0 µm, typically 1.0 to 1.5 µm, for the channel length of 3 to 7 µm. The length (width) of the Lov regions 711a and 712a of the n-channel TFT 803 may be 0.5 to 3.0 µm and typically 1.0 to 1.5 µm. The length (width) of the Loff regions 711b and 712b may be 1.0 to 3.5 µm and typically 1.5 to 2.0 µm. The length (width) of the Loff regions 717, 718, 719 and 720 disposed in the pixel TFT 804 may be 0.5 to 3.5 µm and typically 2.0 to 2.5 µm.

It is another feature of the present invention that the p-channel TFT 801 is formed in self-alignment and the n-channel TFTs 802, 803 and 804 are formed in non-self-alignment.

Incidentally, this example is based on the construction of the active matrix substrate explained in Example 1 and only the structure of the n-channel TFT 803 is added to this construction. Therefore, the conditions of the thin film materials during the fabrication process, the range of the numerical values of the impurity doping process, the range of the film thickness of the thin films, and so forth, explained in Example 1, can be as such used in this example, too. The construction of this example can be combined with the construction of Example 2 or Example 3.

[Example 5]

In this example, the fabrication process of fabricating an active matrix type liquid crystal display device from an active matrix substrate will be explained. As shown in FIG. 9, an orientation film 901 is formed on the substrate under the condition shown in FIG. 8C. A polyimide resin is used in most cases for the orientation film of the liquid crystal display device. A transparent conductive film 903 and an orientation film 904 are formed on an opposing substrate 902. After the orientation films are formed, rubbing treatment is carried out so that the liquid crystal molecules are oriented with a certain predetermined pre-tilt angle. The active matrix substrate having the pixel unit and the CMOS circuit formed thereon and the opposing substrate are bonded to each other through a sealing material or a spacer (both being not shown) by a known cell assembly step. Thereafter, a liquid crystal material 905 is charged between both substrates and is completely sealed by a sealant (not shown). A known liquid crystal material may be used as the liquid crystal material. In this way, the active matrix type liquid crystal display device shown in FIG. 9 is completed.

Next, the construction of this active matrix type liquid crystal display device will be explained with reference to a perspective view of FIG. 10 and top views of FIGs. 11A and 11B. Incidentally, common reference numerals will be used because FIGs. 10, 11A and 11B correspond to the structural sectional view of FIGs. 6A to 6D, 7A to 7C and 8A to 8C. The sectional structure along a line A - A′ shown in FIG. 11B corresponds to the sectional view of the pixel unit shown in FIG. 8C.

The active matrix substrate comprises a pixel unit 1001, a scanning (gate) line driving circuit 1002 and a signal (source) line driving circuit 1003 that are formed on a glass substrate 601. The pixel TFT 804 of the pixel unit is the n-channel TFT, and the driving circuit disposed in the periphery of the pixel unit comprises a CMOS circuit as a basic circuit. The scanning (gate) line driving circuit 1002 and the signal (source) line driving circuit 1003 are connected to the pixel unit 1001 by gate wiring 641 and source wiring 668, respectively. Connection wirings 625 and 673 are so disposed as to extend from external input/output terminals 1005, to which the FPC 1004 is connected, to input/output terminals of the driving circuit.

FIGs. 11A and 11B are top views showing a part (one pixel) of the pixel unit 1001. FIG. 11A is a top view showing in superposition the active layer, the gate wiring and the source wiring. FIG. 11B is a top view showing in superposition a shading film and a pixel electrode on the members shown in FIG. 11A. Referring to FIG. 11A, the gate wiring 641 crosses the active layer 606 below it through a gate insulation film, not shown. A source region, a drain region and an Loff region comprising an n^{--} region are formed in the active layer 606, though they are not shown in the drawings. Reference numeral 1101 denotes a contact portion between the source wiring 668 and the active layer 606 and reference numeral 1102 denotes a contact portion between the drain wiring 672 and the active layer 606.

In FIG. 11B, there are formed the shading film 677 having an anodic oxide (which is not hereby shown but corresponds to the anodic oxide 678 shown in FIG. 8C) formed on the pixel TFT and the pixel electrode 679, 680 and 681 for each pixel. A holding capacitance 682 is fabricated by the region in which the shading film 677 and the pixel electrode 679 overlap with each other through the anodic oxide. Incidentally, reference numeral 1103 denotes a contact portion between the drain wiring 672 and the pixel electrode 679.

This example uses an alumina film having a high specific dielectric constant of 7 to 9 for the dielectric of the holding capacitance, and can therefore reduce the area for securing the necessary capacitance. Furthermore, because this example uses the shading film formed on the pixel TFT as one of the electrodes of the holding capacitance, it can improve the aperture ratio of the image display part of the active matrix type liquid crystal display device.

Incidentally, the active matrix type liquid crystal display device of this example has been explained with reference to the construction explained in Example 4, but it can be freely combined with the construction of any of Examples 1, 2 and 3 so as to fabricate the active matrix type liquid crystal display device.

[Example 6]

The holding capacitance provided to each pixel of the pixel unit can be constituted by using the electrode, that is not connected to the pixel electrode (the shading film in the present invention), as the fixed potential. In such a case, the shading film is preferably kept under the floating condition (under the electrically isolated condition) or under the common potential (at an intermediate potential of the image signals that are sent as data).

In this example, therefore, a connection method when the shading film is fixed to the common potential will be explained with reference to FIGs. 12A and 12B. Referring to FIG. 12A, reference numeral 1201 denotes the pixel TFT that is fabricated in the same way as in Example 1, and reference numeral 1202 denotes the shading film that functions as one of the electrodes of the holding capacitance. The shading film 1202 extends outside the pixel unit and is connected to a power source line 1203 that gives the common potential through a contact hole 1206 bored in a second inter-layer insulation film 1204 and a passivation film 1205.

When the shading film 1202 is electrically connected to the power source line giving the common potential outside the pixel unit in this way, the common potential can be secured. In this case, therefore, a process step of etching the second inter-layer insulation film 1204 and the passivation film 1205 prior to the formation of the shading film 1202 becomes necessary.

Referring next to FIG. 12B, reference numeral 1207 denotes the pixel TFT that is fabricated in the same way as in Example 1, and reference numeral 1208 denotes the shading film that functions as one of the electrodes of the holding capacitance. The shading film 1208 extends outside the pixel unit and overlaps with a conductive film 1210 through an oxide 1211 in the region that is represented by reference numeral 1209. This conductive film 1210 is formed simultaneously with a pixel electrode 1212.

The conductive film 1210 is connected to a power source line 1216 giving a common potential through a contact hole 1215 that is bored in a second inter-layer insulation film 1213 and a passivation film 1214. At this time, a capacitor comprising the shading film 1208, the oxide 1211 and the conductive film 1210 is constituted in the region 1209. When driven by an AC, this capacitor undergoes substantial short-circuit. In other words, since the shading film 1208 and the conductive film 1210 are electrically connected to each other by electrostatic coupling in the region 1209, the shading film 1208 and the power source line 1216 are connected substantially to each other.

Since this example employs the construction shown in FIG. 12B, it can set the shading film to the common potential without increasing the number of process steps.

Incidentally, the construction of this example can be freely combined with the construction of any of Examples 1 to 5.

[Example 7]

FIG. 13 shows an example of the circuit construction of the active matrix substrate represented by Example 4. The active matrix substrate of this example includes a source signal line side driving circuit 1301, a gate signal line side driving circuit (A) 1307, a gate signal line side driving circuit (B) 1311, a pre-charge circuit 1312 and a pixel unit 1306. The source signal line side driving circuit 1301 includes a shift register circuit 1302, a level shifter circuit 1303, a buffer circuit 1304 and a sampling circuit 1305. The gate signal line side driving circuit (A) 1307 includes a shift register circuit 1308, a level shifter circuit 1309 and a buffer circuit 1310. The gate signal line side driving circuit (B) 1311 has a similar construction.

A driving voltage of each shift register circuit 1302, 1308 is 5 to 16 V (typically, 10V), and the n-channel TFT used for a CMOS circuit that constitutes the shift register circuit has suitably the structure represented by reference numeral 802 in FIG. 8C.

The level shifter circuits 1303 and 1309 and the buffer circuits 1304 and 1310 use a high driving voltage of 14 to 16 V. A CMOS circuit containing the n-channel TFT 802 shown in FIG. 8C is suitable for them in the same way as the shift register circuit. Incidentally, it is effective to use a double-gate structure for the gate wiring so as to improve reliability of the circuit.

The sampling circuit 1305 uses a driving voltage of 14 to 16 V. A CMOS circuit containing the n-channel TFT 803 shown in FIG. 8C is suitable because the source region is inverted relative to the drain region and moreover, the OFF current value must be reduced. Incidentally, the n-channel TFT and the p-channel TFT are combined with one another when the sampling circuit is fabricated in practice.

The pixel unit 1306 uses a driving voltage of 14 to 16 V. A lower OFF current value is required for this pixel unit

1306 than for the sampling circuit 1305. Therefore, a complete LDD structure (in which the Lov region is not disposed) is preferably employed, and the n-channel TFT 804 shown in FIG. 8C is preferably used, too.

The construction of this example can be freely combined with the construction of any of Examples 2 to 6.

[Example 8]

In this example, a process step of forming an active layer to function as an active layer of the TFT will be explained with reference to FIGs. 14A to 14E. To begin with, an underlying film 1402 comprising a 200 nm-thick silicon nitride oxide film and a 50 nm-thick amorphous semiconductor film 1403 (an amorphous silicon film in this example) are continuously formed on a substrate 1401 (a glass substrate in this example) without exposing them to the atmospheric air.

Next, an aqueous solution (an aqueous nickel acetate solution) containing 10 ppm by weight of a catalytic element (nickel in this example) is applied by spin coating to form a catalytic element-containing layer 1404 on the entire surface of the amorphous semiconductor film 1403. Examples of the catalytic elements that can be used in this example include germanium (Ge), iron (Fe), palladium (Pd), tin (Sn), lead (Pb), cobalt (Co), platinum (Pt), copper (Cu) and gold (Au) (FIG. 14A) besides nickel (Ni).

Though this example employs a spin coating as the method of adding nickel, a thin film (a nickel film in this example) of a catalytic element may be formed by a vapor deposition or a sputtering on the surface of the amorphous semiconductor film.

Next, prior to the crystallization step, a heat-treatment step is carried out at 400 to 500° C for about 1 hour so as to dissociate hydrogen from inside the film. A heat-treatment is further carried out at 500 to 650° C (preferably at 550 to 570° C) for 4 to 12 hours (preferably for 4 to 6 hours). In this example, this heat-treatment is carried out at 550° C for 4 hours to form a crystalline semiconductor film (a crystalline silicon film in this example) 1405 (FIG. 14B).

Next, a gettering step is carried out in order to remove nickel used in the crystallization step from the crystalline silicon film. First, a mask insulation film 1406 is formed to a thickness of 150 nm on the surface of the crystalline semiconductor film 1405, and an opening 1407 is bored by patterning. A process step of adding an element of the Group 15 of the Periodic Table (phosphorus in this example) to the exposed crystalline semiconductor film is carried out. This process step gives a gettering region 1408 containing phosphorus in a concentration of $1x10^{19}$ to $1x10^{20}$ atoms/cm^3 (FIG. 14C).

A heat-treatment is then carried out in a nitrogen atmosphere at 450 to 650° C (preferably at 500 to 550° C) for 4 to 24 hours (preferably for 6 to 12 hours). Due to this heat-treatment, nickel in the crystalline semiconductor film moves in a direction represented by an arrow in the drawing and is collected into the gettering region 1408 by the gettering operation of phosphorus. In other words, since nickel is removed from inside the crystalline semiconductor film, the nickel concentration in the crystalline semiconductor film 1409 can be lowered to $1x10^{17}$ atoms/cm^3 or lower, preferably $1x10^{16}$ atoms/cm^3 or lower (FIG. 14D).

After the mask insulation film 1406 is removed, patterning is conducted in such a manner as to completely remove the gettering region 1408 to acquire an active layer 1410. Incidentally, though FIG. 14E shows only one active layer 1410, a plurality of active layers are naturally formed simultaneously over the substrate.

Each active layer 1410 so formed comprises a crystalline semiconductor film having extremely high crystallinity because it uses the catalytic element (nickel in this example) for promoting crystallization. The catalytic element is removed by the gettering operation of phosphorus after crystallization, and the concentration of the catalytic element remaining in the active layer 1410 is $1x10^{17}$ atoms/cm^3 or lower, preferably $1x10^{16}$ atoms/cm^3 or lower.

Incidentally, the construction of this example can be freely combined with the construction of any of Examples 1 to 7.

[Example 9]

In this example, a process step of forming an active layer to function as an active layer of the TFT will be explained with reference to FIGs. 15A to 15E. More concretely, this example employs the technology described in Japanese Patent Laid-Open No. 10-247735 (corresponding to U.S. Patent Application Serial No. 09/034,041).

First, an underlying film 1502 comprising a 200 nm-thick silicon nitride oxide film and a 50 nm-thick amorphous semiconductor film (an amorphous silicon film in this example) 1503 are formed continuously on a substrate 1501 (a glass substrate in this example) without exposing them to the atmospheric air. Next, a mask insulation film 1504 comprising a silicon oxide film is formed to a thickness of 200 nm to form an opening 1505.

Next, an aqueous solution (an aqueous nickel acetate solution in this example) containing 100 ppm by weight of a catalytic element (nickel in this example) is applied by spin coating to form a catalytic element-containing layer 1506. At this time, the catalytic element-containing layer 1506 comes into selective contact with the amorphous semiconductor film 1503 in the region in which the opening 1505 is formed. Examples of the catalytic elements that can be used hereby include germanium (Ge), iron (Fe), palladium (Pd), tin (Sn), lead (Pb), cobalt (Co), platinum (Pt), copper (Cu) and gold (Au), besides nickel (Ni) (FIG. 15A).

Though this example employs a spin coating as the method of adding nickel, it is possible to employ means for forming a thin film made of a catalytic element (the nickel film in this example) on the amorphous semiconductor film by a vapor deposition or a sputtering.

Next, prior to a crystallization step, heat-treatment is carried out at 400 to 500° C for about 1 hour to dissociate hydrogen in the film. A heat-treatment is carried out further at 500 to 650° C (preferably at 550 to 600° C) for 6 to 16 hours (preferably, for 8 to 14 hours). In this example, the heat-treatment is carried out at 570° C for 14 hours. As a result, the crystallization proceeds in a direction indicated by the arrow substantially parallel to the substrate drawn in the FIG. 15B with the opening 1505 as the start point. A crystalline semiconductor film (a crystalline silicon film in this example) 1507, in which the crystal growing direction is macroscopically aligned, is thus formed (FIG. 15B).

Next, a gettering step is carried out so as to remove nickel used in the crystallization step from the crystalline silicon film. In this example, a process step of adding an element (phosphorus in this example) belonging to the Group 15 of the Periodic Table is carried out using as such the mask insulation film 1504 formed previously. A gettering region 1508 containing phosphorus in a concentration of $1\text{x}10^{19}$ to $1\text{x}10^{20}$ atoms/cm^3 is thus formed in the crystalline semiconductor film exposed in the opening 1505 (Fig. 15C).

Next, a heat-treatment is carried out in a nitrogen atmosphere at 450 to 650° C (preferably at 500 to 550° C) for 4 to 24 hours (preferably for 6 to 12 hours). Nickel in the crystalline semiconductor film moves in a direction indicated by the arrow drawn in the FIG. 15D due to this heat-treatment and is collected into the gettering region 1508 by the gettering operation of phosphorus. In other words, since nickel is removed from inside the crystalline semiconductor film, the nickel concentration in the crystalline semiconductor film 1509 can be reduced to $1x10^{17}$ atoms/cm^3 or lower, preferably $1x10^{16}$ atoms/cm^3 or lower (FIG. 15D).

After the mask insulation film 1504 is removed, patterning is so conducted as to completely remove the gettering region 1508 to acquire an active layer 1510. Incidentally, FIG. 15E shows only one active layer 1510, but a plurality of active layers can be of course formed simultaneously on the substrate.

The active layer 1510 formed in the way described above comprises a crystalline semiconductor film having extremely high crystallinity because the crystallization is effected by selectively adding the catalytic element (nickel in this example) that promotes crystallization. More concretely, this film has a crystal structure in which rod-like or pillar-like crystal grains are aligned with specific directivity. The catalytic element is removed after the crystallization by the gettering operation of phosphorus, and the concentration of the catalytic element remaining in the active layer 1510 is not higher than $1x10^{17}$ atoms/cm^3, preferably not higher than $1x10^{16}$ atoms/cm^3.

Incidentally, the construction of this example can be combined freely with the construction of any of Examples 1 to 7.

[Example 10]

Examples 8 and 9 use phosphorus for gettering the catalytic element used for crystallizing the semiconductor film. In this example, a method of gettering the catalytic element by the use of other elements will be explained.

First, the crystalline semiconductor film is obtained in the same way as in Example 8 or 9. However, the substrate that can be used in this example is a heat-resistant substrate that can withstand a temperature of 700° C or more, and its typical examples include a quartz substrate, a metal substrate and a silicon substrate. The concentration of the catalytic element (nickel, for example) used for crystallization is lowered as much as possible in this example. More concretely, a nickel-containing layer containing 0.5 to 3 ppm by weight is formed on the amorphous semiconductor film and a heat-treatment is then carried out to attain crystallization. The concentration of nickel contained in the resulting crystalline semiconductor film is $1x10^{17}$ to $1x10^{19}$ atoms/cm^3 (typically, $5x10^{17}$ to $1x10^{18}$ atoms/cm^3).

After the crystalline semiconductor film is formed, a heat-treatment is carried out in an oxidizing atmosphere containing a halogen element. The temperature is 800 to 1,150° C (preferably, at 900 to 1,000° C), and the treatment time is 10 minutes to 4 hours (preferably, 30 minutes to 1 hour).

In this example, the heat-treatment is carried out in an atmosphere containing 3 to 10 volume% of hydrogen chloride at 950° C for 30 minutes. As a result of this heat-treatment, nickel in the crystalline semiconductor film is converted to a volatile chloride (nickel chloride) and dissociates into the treatment atmosphere. In other words, nickel can be removed by the gettering operation of the halogen element. If the nickel concentration in the crystalline semiconductor film is too high, however, the problem develops in that an oxidation proceeds abnormally at the segregation portion of nickel. Therefore, the concentration of nickel used in the crystallization step must be reduced as low as possible.

The concentration of nickel remaining in the crystalline semiconductor film so formed is not higher than $1x10^{17}$ atoms/cm^3, preferably not higher than $1x10^{16}$ atoms/cm^3. Thereafter, the crystalline semiconductor film is patterned to form the active layer, which can be used as the active layer of the TFT.

Incidentally, the construction of this example can be freely combined with the construction of any of Examples 1 to 9. In other words, it can be used in combination with the gettering step by phosphorus that is described in Examples 8 and 9.

[Example 11]

In this example, a process step for improving crystallinity of a crystalline semiconductor film (a crystalline silicon film by way of example) used in the present invention will be explained. First, an active layer is formed in accordance with the step of any of Examples 8, 9 and 10. However, a substrate capable of withstanding to the temperature of 800 to 1,150° C must be used as a substrate on which TFTs are to be formed. Examples of such substrates include a quartz substrate, a metal substrate, a silicon substrate and a ceramic substrate (inclusive of a ceramic glass substrate).

A gate insulation film comprising a silicon nitride oxide film, a silicon oxide film or a laminate film of a silicon nitride film and a silicon oxide film is formed on the substrate. The film thickness of the gate insulation film is 20 to 120 nm (typically, 60 to 80 nm). In this example, the silicon oxide film is formed at 800° C by using a mixture of SiH_4 and N_2O as a starting material.

After the gate insulation film is formed, a heat-treatment is carried out in an oxidizing atmosphere. The temperature is 800 to 1,150° C (preferably, 900 to 1,000° C) and the treatment time is 10 minutes to 4 hours (preferably, 30 minutes to 1 hour).

In this case, a dry oxidation method is the most preferred method but a wet oxidation method may be used, as well. The oxidizing atmosphere may be a 100% oxygen atmosphere, or a halogen element may be contained in the same way as in Example 10.

As a result of this heat-treatment, the active layer formed of the crystalline semiconductor film is oxidized in the proximity of the interface between the active layer and the gate insulation film, thereby forming a thermal oxide film. In consequence, the interface level is reduced and the particularly excellent interface performance can be obtained. Furthermore, since the active layer is oxidized, the film thickness of the active layer is decreased. Excessive silicon that is generated at the time of oxidation drastically improves the defects in the film, and a semiconductor film comes to possess an extremely small defect density and excellent crystallinity.

The process steps of this example are regulated, when the example is worked in practice, so that the final film thickness of the active layer is 20 to 60 nm and that of the gate insulation film is 50 to 150 nm (typically, 80 to 120 nm). In order to make the most of the reducing effect of the defect density, it is preferred to oxidize the active layer by at least 50 nm.

An n^- region that is to serve as the Lov region is then formed by doping an n-type imparting impurity element. Further, a heat-treatment is carried out in an inert atmosphere at 700° C to 950° C (more preferably at 750° C to 800° C) for the purpose of activating the n-type imparting impurity element. The process steps subsequent to the heat-treatment are followed by the process steps subsequent to FIG. 1C of Example 1 or the process steps subsequent to FIG. 6C of Example 4.

The crystal structure of the active layer after these process steps of this example becomes a peculiar crystal structure having continuity in the crystal lattice. The feature will be explained next.

The active layer formed by the steps described above has microscopically a crystal structure of the aggregate of a plurality of needle-like or rod-like crystals (hereinafter called the "rod-like crystals"). This can be confirmed easily by the observation through TEM (transmission electron microscope).

It has been confirmed through an electron diffraction and a X-ray diffraction that the surface (the channel formation portion) of the active layer has a {110} plane as a main orientation plane, though some variances exist in the crystal axes. The inventors of the present invention have examined in detail an electron diffraction photograph having a spot diameter of about 1.5 µm and have confirmed that the diffraction spots corresponding to the {110} plane appear beautifully but each dot has a distribution on the same concentric circle.

The inventors of the present invention have also observed the crystal grain boundary formed by the contact portions of the individual rod-like crystals through HR-TEM (high-resolution transmission electron microscope) and have confirmed that continuity of the crystal lattice exists in the crystal grain boundary. This can be confirmed easily from the fact that the lattice fringes are continuously linked with one another in the crystal grain boundary.

Incidentally, continuity of the crystal lattice in the crystal grain boundary results from the fact that its crystal grain boundary is the grain boundary that is called a "planar grain boundary". The definition of the planar grain boundary in this specification corresponds to the term "planar boundary" described in "Characterization of High-Efficiency Cast-Si Solar Cell Wafers by MBIC Measurement", by Ryuichi Shimokawa and Yutaka Hayashi, Japanese Journal of Applied Physics, Vol. 27, No. 5, pp. 751-758, 1988.

According to the article mentioned above, the term "planar boundary" includes a twin boundary, a special laminar defect, a special twist boundary, and so forth. This planar boundary has a feature in that it is electrically inactive. In other words, though it is a crystal grain boundary, the planar boundary does not function as a trap that impedes movement of the carriers. For this reason, it can be regarded as being substantially absent.

Particularly when the crystal axis (an axis perpendicular to the crystal plane) is the <110> axis, the {211} twin boundary is also called correspondence boundary Σ3. It is known that the Σ value is a parameter as the index that represents the degree of matching of the correspondence boundary, and smaller this Σ value, the higher matching the grain boundary has.

As a result of detailed observation of the crystalline silicon film obtained by working this example through TEM, the inventors of the present invention have clarified that almost all of the crystal grain boundary (at least 90%, typically at least 95%) is the Σ3 correspondence boundary, that is, the {211} twin boundary.

It is known that when the plane orientation of both of two crystals is {110} in the crystal grain boundary formed between two crystal grains, the grain boundary becomes the Σ3 correspondence boundary when the angle θ between the lattice fringes corresponding to the {111} plane is 70.5°.

In the crystalline silicon film of this example, each lattice fringe of the adjacent crystal grain in the crystal grain boundary exactly continues one another at an angle of about 70.5°. The present inventors have reached from this fact the conclusion that this crystal grain boundary is the {211} twin boundary.

Incidentally, when the angle θ is 38.9°, the grain boundary becomes the correspondence boundary of Σ9, and such other boundaries also exist in this film.

Such a crystal structure (speaking more strictly, the structure of the crystal grain boundary) represents that two different crystal grains are bonded to each other with extremely high matching in the crystal grain boundary. In other words, this is the crystal structure in which the crystal lattices continue one another continuously in the crystal grain boundary, and the trap level resulting from the crystal defect or the like is extremely difficult to be created. Therefore, the semiconductor thin film having such a crystal structure can be regarded as a film not having substantially the crystal grain boundary.

Furthermore, the TEM observation reveals that the defects existing in the crystal grains are almost extinguished as a result of a heat-treatment at a temperature as high as 700 to 1,150° C (that corresponds to the thermal oxidation step or to the gettering step in this example). This is clear from the fact that the number of defects after the heat-treatment step becomes drastically smaller than that of before the heat-treatment.

The difference of the number of defects appears as the difference of the spin density in electron spin resonance (ESR). It has been found out at present that the spin density of the crystalline silicon film formed by the process steps of this example is not greater than 5×10^{17} spins/cm^3 (preferably, not greater than 3×10^{17} spins/cm^3). However, because this measurement value is approximate to the detection limit of existing measuring instruments, the practical spin density is expected to be further lower.

From the observation described above, it may be possible to believe that the crystalline silicon film obtained by this example is substantially free from the crystal grain boundary in the crystal grains, and is a single crystal silicon film or a substantial single crystal silicon film.

(Observation of electrical characteristics of TFT):

The TFT using the active layer of this example exhibits the electric characteristics approximate to those of a MOSFET. The following data can be obtained from the TFT fabricated tentatively by the present inventors (with the proviso that the film thickness of the active layer is 30 nm and the film thickness of the gate insulation film is 100 nm).

(1) A sub-threshold coefficient as an index of switching performance (rapidness of ON/OFF switching operation) is as small as 60 to 100 mV/decade (typically, 60 to 85 mV/decade) in both the n-channel TFT and the p-channel TFT.

(2) Field effect mobility (μ_{FE}) as an index of the operation speed of the TFT is as great as 200 to 650 cm^2/Vs (typically, 300 to 500 cm^2/Vs) for the n-channel TFT and 100 to 300 cm^2/Vs (typically, 150 to 200 cm^2/Vs) for the p-channel TFT.

(3) A threshold voltage (V_{th}) as an index of the driving voltage of the TFT is as small as -0.5 to 1.5 V for the n-channel TFT and -1.5 to 0.5 V for the p-channel TFT.

As described above, it has been confirmed that extremely excellent switching characteristics and high-speed operation characteristics can be accomplished. Incidentally, the construction of this example can be freely combined with the construction of any of Examples 1 to 10. It is of importance, however, that this example uses the catalytic element, that promote crystallization as illustrated in Examples 8 to 10, for crystallizing the amorphous semiconductor film.

[Example 12]

In this example, means for gettering the catalytic element (nickel in this example by way of example) used for crystallization from the crystalline semiconductor film (the crystalline silicon film, by way of example) that is crystallized by the means of Example 8 or 9 is explained. Incidentally, this explanation will be given with reference to FIGs. 16A to 16C.

First, the condition shown in FIG. 2B is reached in the same way as in Example 1. Next, phosphorus is added in the same way as the process step shown in FIG. 2C. In this instance, this example uses a resist mask 1601 shown in FIG. 16A in place of the resist mask 132 shown in FIG. 2C. In other words, whereas the resist mask is so disposed in FIG. 2C as to cover the entire region that serves as the p-channel TFT, the resist mask is formed in FIG. 16A in such a manner as not to hide the end portion of the p^{++} regions.

Phosphorus is added under this condition in the same way as the step shown in FIG. 2C. As a result, phosphorus is added also to the end portions of the p^{++} regions 124 and 125 of the p-channel TFT, and ($p^{++} + n^{+}$) regions 1602 and 1603 are thus formed. However, the p-type imparting impurity element contained in the p^{++} regions is added in a sufficiently higher concentration than phosphorus contained in the n^{+} region. Therefore, these regions can be kept as the p^{++} regions.

Next, after the resist masks 1601, 133 and 134 are removed, the phosphorus-doping step is carried out in the same concentration as that of FIG. 3A of Example 1. As a result, the n^{--} regions 140, 141, 142 and 143 are formed (FIG. 16B).

The activation step of the impurity element (phosphorus or boron) added is then carried out in the same way as in the step FIG. 3B of Example 1. In this example, the activation step is preferably conducted by means of a furnace annealing or a lamp annealing. When the furnace annealing is employed, the heat-treatment is carried out at 450 to 650° C, preferably at 500 to 550° C, and 500° C in this Example, for 4 hours (FIG. 16C).

In this example, the source regions or the drain regions of both the n-channel TFT and the p-channel TFT always include the region that contains phosphorus in the concentration corresponding to the n^+ region. For this reason, the nickel-gettering effect by phosphorus can be obtained in the heat-treatment step for thermal activation. In other words, nickel moves from the channel formation region in the direction indicated by arrow drawn in FIG. 16C, and is gettered by the operation of phosphorus contained in the source region or the drain region.

When this example is executed, the activation step of the impurity element added to the active layer functions also as the gettering step of the catalytic element used for crystallization. As a result, the process steps can be simplified effectively.

The construction of this example can be freely combined with the construction of any of Examples 1 to 11. However, this example provides the technology that is effective when the catalytic element that promotes crystallization is used for crystallizing the amorphous semiconductor film.

[Example 13]

In this example, explanation will be given with reference to FIGs. 17A and 17B about the case where the construction of the pixel unit is different from the construction of Example 5 (see FIGs. 11A and 11B). Incidentally, since the basic construction is the same as the construction of Examples 4 and 5, the same reference numeral will be used to identify the same portion.

FIG. 17A is a sectional view of the pixel unit in this example. This example has the feature in that a gate wiring 1700 (except for the overlapping portion with the active layer) is formed by laminating a first conductive film 1701, a second conductive film 1702 and a third conductive film 1703. This gate wiring 1700 is formed simultaneously with the connection wiring 625 explained in Example 4. Therefore, the first conductive film is consisting essentially of tantalum nitride as the principal component, the second conductive film consists essentially of aluminum as the principal component and the third conductive film is the tantalum film.

The top view at this time is shown in FIG. 17B. The portions of the gate wiring, that overlap with the active layer (that may be called the "gate electrode"), 1704a and 1704b have a laminate structure of the first and third conductive films. On the other hand, the gate wiring 1700 has a greater wiring width than the gate wirings 1704a and 1704b and has a three-layered structure as shown in FIG. 17A. In other words, among the gate wirings, the portions that are merely used for the wiring preferably employ the construction of this example in order to reduce the wiring resistance as much as possible.

Incidentally, the construction of this example may be freely combined with the construction of any of Examples 1 to 12.

[Example 14]

In this example, explanation will be given with reference to FIGs. 18A to 18C about the case where the TFT is fabricated in the process steps different from those of Example 4. Since the intermediate steps are the same as those of Example 4, the same reference numeral will be used for the same process step. The impurity element added is the same as the impurity element used in Example 4, by way of example.

First, the condition shown in FIG. 7B is reached in accordance with the steps of Example 4. This condition is shown in FIG. 18A in this example. Next, the resist masks 633, 634, 635, 636, 637 and 638 are removed, and the phosphorus doping step is carried out to form the n^{--} region. The doping condition is the same as that of the process step of Example 4 shown in

FIG. 8A. In FIG. 18B, the regions represented by reference numerals 1801, 1802 and 1803 are the regions in which phosphorus corresponding to the n^{--} region is added to the n^- region. Reference numerals 1804, 1805 and 1806 denote the n^{--} regions that serve as the Loff region of the pixel TFT (FIG. 18B).

Next, resist masks 1807, 1808, 1809, 1810 and 1811 are formed, and phosphorus is added under the same condition as that of FIG. 7C. This process step provides the regions 1812, 1813, 1814, 1815, 1816, 1817 and 1818 to which phosphorus is added in a high concentration (FIG. 18C).

Thereafter, the process steps of FIG. 8B and so on are carried out in accordance with the process steps of Example 4, and the pixel unit having the structure explained with reference to FIG. 8C can be obtained. When this example is employed, phosphorus in the concentration corresponding to the n^+ region is not added to the source and drain regions of the p-channel TFT that constitute the CMOS circuit. Therefore, the boron concentration necessary for the p^{++} addition step may be low, and throughput can be improved. If phosphorus is added to the end portions of the p^{++} regions of the n-channel TFT in the process step shown in FIG. 18C, the gettering step of Example 12 can be carried out.

When the n^+ region or the p^{++} region that constitutes the source region or the drain region is formed, it is possible to etch the gate insulation film to expose a part of the active layer before the impurity element is added, and then to add the impurity element to the portion so exposed. In this case, since the acceleration voltage may be low, damage to the active layer is small and throughput can be improved.

When this example is executed, the concentration of the impurity element contained in the impurity regions formed finally in the active layer, may be sometimes different from that of

Example 4. However, since the substantial function of each impurity region remains unchanged, the explanation of the construction of FIG. 8C can be as such applied to the explanation of the final construction of this example. The construction of this example can be applied to Example 1 or 4, and can be freely combined with the construction of any of Examples 2, 3 and 5 to 13.

[Example 15]

In this example, explanation will be given with reference to FIGs. 19A to 19C on the case where the TFT is fabricated in the process steps different from those of Example 4. Since these steps up to the intermediate steps are the same as those of Example 4, the same reference numeral will be used for the same process step. The impurity element added is the same as the impurity element used in Example 4, by way of example.

First, the condition shown in FIG. 6D is reached in accordance with the process steps of Example 4. Next, the gate wiring of the n-channel TFT and other connection wirings are formed. In FIG. 19A, reference numerals 1901 and 1902 denote connection wirings and reference numerals 1903, 1904 and 1905 denote gate wirings of the n-channel TFT. Reference numeral 1906 denotes a conductive film for forming the gate wiring of the p-channel TFT.

Next, resist masks 1907, 1908, 1909, 1910 and 1911 are formed, and phosphorus is added under the same condition as that of the step of FIG. 7C in Example 4. In this way, there are formed the impurity regions 1912, 1913, 1914, 1915, 1916, 1917 and 1918 containing phosphorus in a high concentration (FIG. 19A).

After the resist masks 1907, 1908, 1909, 1910 and 1911 are removed, resist masks 1919, 1920, 1921, 1922, 1923 and 1924 are formed afresh, and a gate wiring 1925 of the p-channel TFT is formed. Boron is added under the same condition as that of FIG. 7A, forming p^{++} regions 1926 and 1927 (FIG. 19B).

After the resist masks 1919, 1920, 1921, 1922, 1923 and 1924 are removed, phosphorus is added under the same condition as that of FIG. 8A. As a result, the $(n^{-} + n^{--})$ regions 1930 and 1931 and the n^{--} regions 1932, 1933, 1934 and 1935 are formed (FIG. 19C).

Thereafter, the process steps of FIG. 8B and so on are carried out in accordance with Example 4, and the pixel unit having the construction explained with reference to FIG. 8C can be obtained. When this example is employed, the construction becomes the one in which phosphorus having the concentration corresponding to the n^{+} region is not added to the source and drain regions of the p-channel TFT that constitutes the CMOS circuit. For this reason, the boron concentration required for the p^{++} addition step may be low, and throughput can be improved.

When the n^{+} region or the p^{++} region that constitutes the source or drain region is formed, it is possible to etch the gate insulation film so as to expose a part of the active layer before the addition of the impurity element, and then to add the impurity element to the portion so exposed. In this case, since the acceleration voltage may be low, damage to the active layer is small and throughput can be improved.

When this example is executed, there may be the case where the concentration of the impurity element contained in the impurity regions formed finally in the active layer is different from that of Example 4. However, because the substantial function of each impurity region remains unchanged, the explanation of the construction of FIG. 8C can be applied as such to the explanation of the final construction obtained by executing this example. The construction of this example can be applied to the construction of Example 1 or 4, and can be freely combined with the construction of any of Examples 2, 3, 5 to 11 and 13.

[Example 16]

In this example, explanation will be given with reference to FIGs. 20A to 20C on the case where the TFT is fabricated in the different process order as those of Example 4. Incidentally, the same reference numeral will be used in the same process steps because the process steps up to the intermediate steps are the same as those of Example 4. The impurity element added is also the same as that of Example 4, by way of example.

First, the condition shown in FIG. 6D is reached in accordance with the process steps of Example 4, and then the condition shown in FIG. 19A is reached in accordance with the process steps of Example 15. This condition is shown in FIG. 20A in this example. Incidentally, reference numerals used in FIG. 20A are the same as those used in FIG. 19A.

After the resist masks 1907, 1908, 1909, 1910 and 1911 are removed, phosphorus is added under the same condition as that of FIG. 8A. As a result, $(n^- + n^{--})$ regions 2001 and 2002 and the n^{--} regions 2003, 2004, 2005 and 2006 are formed (FIG. 20B).

Next, resist masks 2007, 2008, 2009, 2010, 2011 and 2012 are formed, and a gate wiring 2013 of the p-channel TFT is formed. Boron is added under the same condition as that of FIG. 7A, thereby forming the p^{++} regions 2014 and 2015 (FIG. 20C).

Thereafter, the process steps of FIG. 8B and so on are carried out in accordance with Example 4, and the pixel unit having the construction explained with reference to FIG. 8C can be obtained. When this example is employed, the construction becomes the one in which phosphorus is not at all added to the source and drain regions of the p-channel TFT that forms the CMOS circuit. Therefore, the boron concentration necessary for the p^{++} addition step may be low, and throughput can be improved.

When the n^{+} region or the p^{++} region that constitutes the source region or the drain region is formed, the gate insulation film may be etched away before the addition of the impurity element so as to expose a part of the active layer and then the impurity element may be added to the portion so exposed. In this case, since the acceleration voltage may be low, damage to the active layer is small and throughput can be improved.

When this example is executed, there may be the case where the concentration of the impurity element contained in the impurity regions formed finally in the active layer is different from that of Example 4 due to the change of the process order. However, because the substantial function of each impurity region remains unchanged, the explanation of the construction of FIG. 8C can be applied as such to the explanation of the final construction obtained by this example. The construction of this example can be applied to Example 1 or 4, or can be freely combined with the construction of any of other Examples 2, 3, 5 to 11 and 13.

[Example 17]

In this example, explanation will be given with reference to FIGs. 21A to 21D on the case where the TFT is fabricated in the different process order from that of Example 4. Incidentally, the process steps are the same as those of Example 4 up to the intermediate steps, the same reference numeral is used in the same process step. The impurity element added is the same as that of Example 4 by way of example.

First, the condition shown in FIG. 6D is reached in accordance with Example 4. Next, the gate wiring of the n-channel TFT and other connection wirings are formed in the same way as in FIG. 7B without conducting the process step shown in FIG. 7A (the formation step of the gate wiring of the p-channel TFT and the p^{++} regions). Incidentally, the same reference numerals are used in FIG. 21A as those in FIG. 7B. As to the region that functions as the p-channel TFT, however, a resist mask 2101 is formed, and a conductive film 2102 that will later serve as the gate wiring of the p-channel TFT is left.

While the resist mask is left unremoved, phosphorus is added under the same condition as that of FIG. 8A. As a result, there are formed (n^{-} + n^{--}) regions 2103, 2104 and 2105 and n^{--} regions 2106, 2107 and 2108 (FIG. 21B).

Next, resist masks 2109, 2110, 2111, 2112 and 2113 are formed, and phosphorus is added under the same condition as that of FIG. 7C of Example 4. In this way, impurity regions 2114, 2115, 2116, 2117, 2118, 2119 and 2120 containing phosphorus in a high concentration are formed (FIG. 21C).

After the resist masks 2109, 2110, 2111, 2112 and 2113 are removed, resist masks 2121, 2122, 2123, 2124, 2125 and 2126 are formed afresh, and a gate wiring 2127 of the p-channel TFT is formed. Boron is added under the same condition as that of FIG. 7A, thereby forming p^{++} regions 2128 and 2129 (FIG. 21D).

Thereafter, the process steps after the step shown in FIG. 8B are carried out in the same way as in Example 4, and the pixel unit having the construction explained with reference to FIG. 8C can be obtained. When this example is employed, the construction becomes the one in which phosphorus is not at all added into the source and drain regions of the p-channel TFT that constitutes the CMOS circuit. Therefore, the boron concentration necessary for the p^{++} addition step may be low, and throughput can be improved.

When the n^{+} region or the p^{++} region that constitutes the source region or the drain region is formed, the gate insulation film may be so etched as to expose a part of the active layer before the addition of the impurity element and the impurity element may be added to the portion so exposed. In this case, since the acceleration voltage may be small, damage to the active layer is small and throughput can be improved.

When this example is executed, there may be the case where the concentration of the impurity element contained in the impurity regions formed finally in the active layer is different from that of Example 4 because the process order changes. However, since the substantial function of each impurity region remains unchanged, the explanation of the construction of FIG. 8C can be applied as such to the final construction obtained by this example. The construction of this example can be applied to the construction of Example 1 or 4, or can be freely combined with the construction of any of other Examples 2, 3, 5 to 11 and 13.

[Example 18]

In this example, explanation will be given with reference to FIGs. 22A to 22C on the case where the TFT is fabricated by different process order from those of Example 4. Incidentally, since the process steps up to the intermediate step are the same as those of Example 4, the same reference numerals are used in the same process step. The impurity element added is also the same as that of Example 4, by way of example.

First, the condition shown in FIG. 6D is reached in accordance with Example 4, and the condition shown in FIG. 21B is reached in accordance with Example 17. In this example, this condition is shown in FIG. 22A. Incidentally, the reference numerals used in FIG. 22A are the same as those of FIG. 21B.

After the resist masks are removed, resist masks 2201, 2202, 2203, 2204, 2205 and 2206 are formed afresh, and a gate wiring 2207 of the p-channel TFT is formed. Boron is then added under the same condition as that of FIG. 7A, thereby forming p^{++} regions 2208 and 2209 (FIG 22B).

Next, resist masks 2210, 2211, 2212, 2213 and 2214 are formed, and phosphorus is added in the same way as in FIG. 7C. In this way, impurity regions 2215, 2216, 2217, 2218, 2219, 2220 and 2221 containing phosphorus in a high concentration are formed (FIG. 22C).

Thereafter, the process steps of FIG. 8B and so on are carried out in accordance with Example 4, and the pixel unit having the construction explained with reference to FIG. 8C can be obtained. When this example is employed, the construction becomes the one in which phosphorus is not at all added to the source and drain regions of the p-channel TFT that constitutes the CMOS circuit. Therefore, the boron concentration necessary for the p^{++} addition step may be small, and throughput can be improved. If phosphorus is added also to the end portions of the p^{++} regions 2208 and 2209 in the step shown in FIG. 22C, the gettering step of Example 12 can be carried out.

When the n^{+} region or the p^{++} region that constitutes the source region or the drain region is formed, the gate insulation film may be so etched as to expose a part of the active layer before the addition of the impurity element. The impurity element may be then added to the portion so exposed. In this case, since the acceleration voltage may be low, damage to the active layer is small and throughput can be improved.

When this example is executed, there may be the case where the concentration of the impurity element contained in the impurity regions formed finally in the active layer is different from that of Example 4 because the process order changes. However, since the substantial function of each impurity region remains unchanged, the explanation of the construction of FIG. 8C can be as such applied to the explanation of the final construction obtained by this example. The construction of this example can be applied to the construction of Example 1 or 4, and can be freely combined with the construction of any of other Examples 2, 3 and 5 to 13.

[Example 19]

The fabrication steps illustrated in Examples 4 and 14 to 18 are based on the premise that the n^- region, which is to later function as the Lov region, is formed in advance before the gate wiring of the n-channel TFT is formed. These process steps are characterized also in that both p^{++} regions and the n^{--} regions are formed in self-alignment.

However, the effect of the present invention can be acquired if the final construction is the one that is shown in FIG. 3C or FIG. 8C, and the process steps up to the final construction are not particularly restrictive. Therefore, the p^{++} regions and the n^{--} regions can be formed in some cases using resist masks. In such a case, the examples of the fabrication steps are not limited to Examples 4 and 14 to 18 but can be combined in every possible combination.

In order to add the impurity element for imparting one conductivity type to the active layer that is the active layer of the TFT, four process steps, that is, the formation of the n^- regions, the formation of the n^+ regions, the formation of the n^{--} regions and the formation of the p^{++} regions, are necessary in the present invention. Therefore, there are 24 orders of the process steps in all by merely changing the order of these four steps. Examples 4 and 14 to 18 represent six orders among them. However, because the effects of the present invention can be obtained in all of the remaining 18 orders, the impurity regions may be formed in any of the orders.

When the n^+ region or the p^{++} region that constitutes the source region or the drain region is formed, the gate insulation film may be etched in such a manner as to expose a part of the active layer before the addition of the impurity element. The impurity element may then be added to the portion so exposed. In this case, since the acceleration voltage may be low, damage to the active layer is small and throughput can be improved.

The construction of this example can be freely combined with the combination of any of Examples 2 to 11 and 13. It can be combined also with Example 12 depending on the order of the process steps.

[Example 20]

In this example, explanation will be given on the case where the present invention is used for a bottom gate TFT. More concretely, FIG. 23 shows the case where the present invention is used for an inverted stagger type TFT. The inverted stagger type TFT does not have a remarkable difference from the top gate type TFT of the present invention except for the positional relationship between the gate wiring and the active layer is different. In this example, therefore, explanation will be given particularly on the remarkable difference from the construction shown in FIG. 8C and the explanation of the rest of the portions will be omitted because they are the same as those shown in FIG. 8C.

In FIG. 23, reference numerals 11 and 12 denote a p-channel TFT and an n-channel TFT of a CMOS circuit that constitutes a shift register circuit or the like, respectively. Reference numeral 13 denotes an n-channel TFT for forming a sampling circuit or the like, and reference numeral 14 denotes an n-channel TFT for forming a pixel unit. These thin film transistors are formed over the substrate on which an underlying film is formed.

Reference numeral 15 denotes a gate wiring of the p-channel TFT 11 and reference numeral 16 denotes a gate wiring of the n-channel TFT 12. Reference numeral 17 denotes a gate wiring of the n-channel TFT 13 and reference numeral 18 denotes a gate wiring of the n-channel TFT 14. Each of these gate wirings can be formed by using the same material as that of the gate wiring explained in Example 4. Reference numeral 19 denotes a gate insulation film, which can be formed by using the same material as that of Example 4, too.

An active layer of each TFT 11, 12, 13 and 14 is formed over the gate wirings and the gate insulation film described above. A source region 20, a drain region 21 and a channel formation region 22 are formed in the active layer of the p-channel TFT 11.

A source region 23, a drain region 24, an LDD region (an Lov region 25 in this case) and a channel formation region 26 are formed in the active layer of the n-channel TFT 12.

A source region 27, a drain region 28, LDD regions (Lov regions 29a, 30a and Loff regions 29b, 30b in this case) and a channel formation region 31 are formed in the active layer of the n-channel TFT 13.

A source region 32, a drain region 33, LDD regions (Loff regions 34, 35, 36 and 37 in this case), channel formation regions 38, 39 and an n^+ region 40 are formed in the active layer of the n-channel TFT 14.

Incidentally, insulation films represented by reference numerals 41, 42, 43, 44 and 45 are formed in order to protect the channel formation regions and to form the LDD regions.

As described above, the present invention can be easily applied to the bottom gate type TFT typified by the inverted stagger type TFT. To fabricate the inverted stagger type TFT of this example, the process steps described in other Examples of this specification may be applied to the known fabrication process of the inverted stagger type TFT. The construction of this example can also be applied to the active matrix type liquid crystal display device illustrated in Examples 5 and 7.

[Example 21]

In this example, explanation will be given on the case where the present invention is applied to a reflection type liquid crystal display device fabricated on a silicon substrate (a silicon wafer). This example can be executed by adding an n-type or p-type imparting impurity element to the silicon substrate in place of the active layer comprising the crystalline silicon film in Example 1 or 4 so as to accomplish the TFT structure of the present invention. Since the liquid crystal display device is of the reflection type, a metal film having a high reflection factor is used for the pixel electrode.

In other words, the LDD regions of the n-channel TFTs that include at least the pixel unit and the driving circuit on the same substrate and form the driving circuit are arranged in such a fashion that at least a part or the entire part thereof overlap with the gate wirings. The LDD regions of the pixel TFTs that constitute the pixel unit are arranged in such a fashion as not to overlap with the gate wirings. Furthermore, the LDD regions of the n-channel TFTs that constitute the driving circuit contain the n-type imparting impurity element in a higher concentration than the LDD regions of the pixel TFTs.

Incidentally, the construction of this example can be freely combined with the construction of any of Examples 1 to 7 and 13 to 19.

[Example 22]

In Examples 1 to 21, explanation has been given on the premise that the Lov regions and the Loff regions are arranged only in the n-channel TFTs and their positions are used properly in accordance with the circuit specification. This may hold true of the p-channel TFT when the TFT size becomes small (the channel length becomes short).

Namely, when the channel length is 2 µm or less, the short channel effect becomes remarkable, and it becomes necessary from time to time to dispose the Lov region also in the p-channel TFT. In other words, the p-channel TFT in the present invention is not limited particularly to the structure described in Examples 1 to 21 but may have the same structure as that of the n-channel TFT.

Needless to say, the construction of this example can be applied to the construction of any of Examples 1 to 21 and to their combinations.

[Example 23]

FIG. 33 shows a graph of a relation between drain current (ID) and gate voltage (VG) of the n-channel TFT 802 fabricated by the process steps according to the Example 4. Hereinafter, the graph is called as ID-VG curve. FIG. 33 further shows a graph of a relation between field effect mobility (μ_{FE}) and the gate voltage (VG) of the n-channel TFT 802. Here, a source voltage (VS) is 0V and a drain voltage (VD) is 1V or 14V. In this connection, the n-channel TFT 802 has a channel length (L) of 8 μm, a channel width (W) of 7.5 μm and a thickness of a gate insulation film (Tox) of 115 nm.

The bold lines represent the first ID-VG curve prior to a stress test, and the dotted lines represent the second ID-VG curve subsequent to the stress test in FIG. 33. Because little change is observed between the first ID-VG curve and the second ID-VG curve, we find that the degradation owing to hot carriers is restricted. The stress test is the test for accelerating the degradation owing to hot carriers by applying a source voltage of 0V, a drain voltage of 20V and a gate voltage of 2V for 60 seconds at a room temperature.

FIG. 34 shows the change of degradation rate of the field effect mobility (μ_{FE}) dependent on the length of the Lov region. The degradation rate of the μ_{FE} is represented as a following expression.

1 - (μ_{FE} prior to the stress test / μ_{FE} subsequent to the stress test) x 100

As a result, we find that the degradation of the μ_{FE} owing to hot carriers is restricted when the length of the Lov region is 0.5 μm or more (preferably, 1.0 μm or more).

FIGs. 35A and 35B show the result of a long time reliability test with respect to the liquid crystal display device fabricated by the process steps in accordance with the Examples 4 and 5. The reliability test is performed in an atmosphere of 85° C. The power source of a first shift register constituting a source side driving circuit is kept at a positive power source 9.6V, a first negative power source -2.4V and a second negative power source -9.6V during the reliability test; the power source of a second shift register constituting a gate side driving circuit is kept at a positive power source 9.6V, a first negative power source -2.4V and a second negative power source -11.0V during the reliability test.

FIG. 35A shows the time dependent change of current consumption (S_IDD) in the case of the first shift register constituting the source side driving circuit, and little change is observed until 3000 hours. FIG. 35B shows the time dependent change of the lowest operation voltage (S_VDD) in the case of the first shift register constituting the source side driving circuit (the lowest voltage which the first shift register operates), and little change is also observed until 3000 hours. In the second shift register constituting the gate side driving circuit, almost the same results as the FIGs. 35A and 35B are obtained although not shown here.

[Example 24]

FIG. 36 shows a graph of a relation between drain current (ID) and gate voltage (VG) of the n-channel TFT (the same structure as the n-channel TFT 802) fabricated by the process steps according to the Example 11. FIG. 33 further shows a graph of a relation between field effect mobility (μ_{FE}) and the gate voltage (VG) of the n-channel TFT. Here, a source voltage (VS) is 0V and a drain voltage (VD) is 1V or 14V. In this connection, the n-channel TFT has a channel length (L) of 8.1 μm, a channel width (W) of 7.6 μm and a thickness of a gate insulation film (Tox) of 120 nm.

The bold lines represent the first characteristic prior to a stress test, and the dotted lines represent the second characteristic subsequent to the stress test in FIG. 36. FIG. 36 shows that the degradation owing to hot carriers is observed very little. The stress test is performed under a condition almost the same as the condition explained in Example 23 although a gate voltage is set at 4V.

FIG. 37 shows the change of degradation rate of the field effect mobility (μ_{FE}) dependent on the length of the Lov region. The degradation rate of the μ_{FE} is defined in Example 23. FIG. 37 clearly shows that the degradation of the μ_{FE} due to hot carriers is restricted when the length of the Lov region is 1 μm or more.

FIGs. 38A and 38B show the result of a long time reliability test with respect to the liquid crystal display device fabricated by the process steps in accordance with the Examples 4, 5 and 11. The reliability test is performed in an atmosphere of 80° C. The power source of a first shift register constituting a source side driving circuit and a second shift register constituting a gate side driving circuit are kept at a first positive power source 8.5V, a second positive power source 4.2V and a negative power source -8.0V during the reliability test.

FIG. 38A shows the time dependent change of current consumption (S_IDD) in the case of the first shift register constituting the source side driving circuit, and little change is observed until 2000 hours. FIG. 38B shows the time dependent change of the lowest operation voltage (S.VDD) in the case of the first shift register constituting the source side driving circuit, and little change is also observed until 2000 hours. In the second shift register constituting the gate side driving circuit, almost the same results as the FIGs. 38A and 38B are obtained although not shown here.

[Example 25]

The present invention can be employed also for the case where an inter-layer insulation film is formed on a conventional MOSFET and then a TFT is formed on this film. In other words, a semiconductor device having a three-dimensional structure can be accomplished, too. SOI substrates such as a SIMOX, Smart-Cut (trade name of SOITEC Co.), ELTRAN (trade name of Canon Co.), and so forth, can be used for the substrate.

Incidentally, the construction of this example can be freely combined with the construction of any of Examples 1 to 7, 13 to 19, 21 and 22.

[Example 26]

The liquid crystal display device fabricated by the present invention can use various liquid crystal materials. Examples of such materials include a TN liquid crystal, a PDLC (Polymer Dispersion type Liquid Crystal), an FLC (a Ferroelectric Liquid Crystal), an AFLC (Anti-Ferroelectric Liquid Crystal) and a mixture of the FLC and the AFLC.

For example, it is possible to use those liquid crystal materials which are described in H. Furue et al.; "Characteristics and Driving Scheme of Polymer-Stabilized Mono-stable FLCD Exhibiting Fast Response Time and High Contrast Ratio with Gray-Scale Capability, SID, 1998", T. Yoshida et al.; "A Full-Color Thresholdless Antiferroelectric LCD Exhibiting Wide Viewing Angle with Fast Response Time, 841, SID97 DIGEST, 1997", and U.S. Patent No. 5,594,569.

Particularly when the thresholdless antiferroelectric LCD (hereinafter abbreviated as "TL-AFLC") is used, the operating voltage of the liquid crystal can be lowered to about ±2.5 V, and the power source voltage may be from about 5 to 8 V in some cases. In other words, the driving circuit and the pixel unit can be operated at the same power source voltage, and power consumption of the liquid crystal device can be reduced as a whole.

The ferroelectric liquid crystal and the antiferroelectric liquid crystal have the advantage that their response time is higher than that of the TN liquid crystal. Because the crystalline silicon TFT used in the present invention can achieve the TFT having an extremely high operation speed, the present invention can accomplish a liquid crystal display device having a high image response speed by making the most of the high response speed of the ferroelectric liquid crystal and the antiferroelectric liquid crystal.

Needless to say, the liquid crystal display device of this example can be used effectively as a display unit of electric/electronic appliances such as a personal computer.

The construction of this example can be combined freely with the construction of any of Examples 1 to 22 and 25.

[Example 27]

The present invention can be applied to an active matrix type EL (electroluminescence) display (called also the "EL display device"). FIG. 24 shows its example.

FIG. 24 is a circuit diagram of the active matrix type EL display of this example. Reference numeral 81 denotes a display region. An X direction (source side) driving circuit 82 and a Y direction (gate side) driving circuit 83 are disposed round the display region 81. Each pixel of the display region 81 includes a switching TFT 84, a capacitor 85, a current controlling TFT 86 and an EL cell 87. An X direction signal line (source signal line) 88a (or 88b) and a Y direction signal line (gate signal line) 89a (or 89b, 89c) are connected to the switching TFT 84. Power source lines 90a and 90b are connected to the current controlling TFT 86.

The active matrix type EL display of this example can be combined with the construction of any of Examples 1 to 4, 6 and 8 to 22 and 25.

[Example 28]

In this example, explanation will be given on the case where the present invention is applied to the fabrication of an EL (electroluminescence) display device. FIG. 25A is a top view of the EL display device of this example and FIG. 25B is its sectional view.

Referring to FIG. 25A, reference numeral 4002 denotes a pixel unit, reference numeral 4003 denotes a source side driving circuit and reference numeral 4004 does a gate side driving circuit. Each driving circuit is extended via a wiring 4005 to an FPC (flexible printed circuit) 4006 and is then connected to an external appliance.

In this instance, a first seal member 4101, a cover member 4102, a filler 4103 and a second seal member 4104 are disposed in such a fashion as to encompass the pixel unit 4002, the source side driving circuit 4003 and the gate side driving circuit 4004.

FIG. 25B is a sectional view taken along a line A - A' of FIG. 25A. Driving TFTs 4201 (an n-channel TFT and a p-channel TFT being shown hereby) contained in the source side driving circuit 4003 and a current controlling TFT 4202 (TFT for controlling the current to the EL cell) contained in the pixel unit 4002 are fabricated over the substrate 4001.

This example uses a TFT having the same structure as that of the p-channel TFT 181 and the n-channel TFT 182 shown in FIGs.

3A to 3C for the driving TFT 4201, and a TFT having the same structure as that of the p-channel TFT 181 shown in FIGs. 3A to 3C for the current controlling TFT 4202. A holding capacitance (not shown) connected to the gate of the current controlling TFT 4202 is disposed in the pixel unit 4002.

An inter-layer insulation film (planarization film) 4301 made of a resin material is formed over the driving TFT 4201 and the pixel TFT 4202, and a pixel electrode (anode) 4302 electrically connected to the drain of the pixel TFT 4202 is formed on the inter-layer insulation film 4301. A transparent conductive film having a high work function is used for the pixel electrode 4302. A compound between indium oxide and tin oxide or a compound between indium oxide and zinc oxide can be used for the transparent conductive film.

An insulation film 4303 is formed on the pixel electrode 4302, and an opening is bored in the insulation film 4303 on the pixel electrode 4302. An EL (electroluminescence) layer 4304 is formed at this opening on the pixel electrode 4302. A known organic or inorganic EL material can be used for the EL layer 4304. Low molecular weight type (monomer type) materials and polymer type materials can be used for the organic EL materials.

The EL layer 4304 can be formed by a known vapor deposition technology or application technology. The structure of the EL layer may be either a laminate structure or a single layer structure of a positive hole injection layer, a positive hole transportation layer, a light emitting layer, an electron transportation layer or an electron injection layer by combining them freely.

A cathode 4305 comprising a conductive film having a shading property (typically, a conductive film made of aluminum, copper or silver as the principal component or its laminate film with other conductive film) is formed on the EL layer 4304. The moisture and oxygen that may exist in the interface between the cathode 4305 and the EL layer 4304 are preferably removed as much as possible. Therefore, these films are continuously formed in vacuum, or the EL layer 4304 is first formed in a nitrogen or inert gas atmosphere and is shaped into the cathode 4305 without being brought into contact with oxygen and moisture. To achieve such film formation, this example uses a multi-chamber system (cluster tool system) film formation apparatus.

The cathode 4305 is electrically connected to the wiring 4005 in the region represented by reference numeral 4306. The wiring 4005 applies a predetermined voltage to the cathode 4305 and is electrically connected to the FPC 4006 through an anisotropic conductive film 4307.

The EL cell comprising the pixel electrode (anode) 4302, the EL layer 4304 and the cathode 4305 are formed in the manner described above. This EL cell is encompassed by the first seal member and the cover material 4102 bonded to the substrate 4001 by the first seal member 4101. The EL cell is further sealed by the filler 4103.

Examples of the cover material 4102 include a glass sheet, a metal sheet (typically, a stainless steel sheet), a ceramic sheet, an FRP (fiberglass-reinforced plastic) sheet, a PVF (polyvinyl fluoride) film, a Mylar film, a polyester film and an acrylic resin film. A laminate sheet sandwiching an aluminum foil by the PVF films or the Mylar films can also be used.

When the radiation direction of light from the EL cell travels towards the cover material side, however, the cover material must be transparent. In this case, a transparent material such as a glass sheet, a plastic sheet, a polyester film or an acrylic resin film is used.

A UV-curing resin or a thermosetting resin can be used for the filler 4103. Examples include PVC (polyvinyl chloride), an acrylic resin, a polyimide resin, an epoxy resin, a silicone resin, PVB (polyvinyl butyral) and EVA (ethylene-vinyl acetate). Degradation of the EL cell can be restrained if a hygroscopic material (preferably, barium oxide) is disposed inside this filler 4103.

The filler 4103 may further contain a spacer. If the spacer is made of barium oxide, the spacer itself becomes hygroscopic. When the spacer is disposed, it is also effective to dispose a resin film on the cathode 4305 as a buffer layer for buffering the pressure from the spacer.

The wiring 4005 is electrically connected to the FPC 4006 through the anisotropic conductive film 4307. The wiring 4005 transmits the signals transferred to the pixel unit 4002, the source side driving circuit 4003 and the gate side driving circuit 4004, to the FPC 4006. The wiring 4005 is electrically connected to the external appliance by the FPC 4006.

In this example, the second seal member 4104 is disposed in such a fashion as to cover the exposed portion of the first seal member 4101 and a part of the FPC 4006 and to completely cut off the EL cell from the external atmosphere. In this way, the EL display device having the sectional structure shown in FIG. 25B can be obtained. Incidentally, the EL display device of this example may be fabricated in combination with the construction of any of Examples 1 to 4, 6 to 20 and 22.

FIG. 26 shows a further detailed sectional structure of the pixel unit, FIG. 27A shows its top structure and FIG. 27B shows its circuit diagram. Since common reference numerals are used in these drawings, cross-reference should be made with one another.

In FIG. 26, the switching TFT 4402 disposed on the substrate 4401 is formed of the n-channel TFT 183 shown in FIG. 3C.

Therefore, reference should be made to the explanation of the structure of the n-channel TFT 183 for the detail of the structure. The wiring represented by reference numeral 4403 is the one that electrically connects the gate wirings 4404a and 4404b of the switching TFT 4402.

Incidentally, this example has the double-gate structure in which two channel formation regions are formed, but it may have a single gate structure in which only one channel formation region is formed, or a triple-gate structure in which three channel formation regions are formed.

The drain wiring 4405 of the switching TFT 4402 is electrically connected to the gate electrode 4407 of the current controlling TFT 4406. Incidentally, the current controlling TFT 4406 is formed of the p-channel TFT 181 shown in FIG. 3C. Therefore, as to the explanation of the structure, reference should be made to the explanation of the p-channel TFT 181. Though this example employs the single gate structure, it may be a double-gate structure or a triple-gate structure.

A first passivation film 4408 is disposed on the switching TFT 4402 and the current controlling TFT 4406, and a planarization film 4409 made of a resin is formed on this passivation film 4408. It is of utmost importance to planarize the steps resulting from the TFTs by using this planarization film 4409. Since the EL layer to be formed later is extremely thin, the existence of any step may invite a luminescence defect. Therefore, planarization is preferably effected before the formation of the pixel electrodes so that the EL layer can be shaped into a plane as planar as possible.

Reference numeral 4410 denotes a pixel electrode (an anode of the EL cell) comprising a transparent conductive film. The pixel electrode 4410 is electrically connected to a drain wiring 4411 of the current controlling TFT 4406. A conductive film made of a compound between indium oxide and tin oxide or a compound between indium oxide and zinc oxide can be used for the pixel electrode 4410.

An EL layer 4412 is formed on the pixel electrode 4410. Though FIG. 26 shows only one pixel, the EL layers are formed properly so as to correspond to R (red), G (green) and B (blue) colors, respectively, in this example. In this example, a low molecular weight organic EL material is formed by vapor deposition. More concretely, the EL layer has a laminate structure in which a 20 nm-thick copper phthalocyanine (CuPc) film is disposed as a positive hole injection layer, and a 70 nm-thick tris-8-quinolinolatoaluminum complex (Alq_3) film as a light-emitting layer is disposed on the CuPc film. The luminescence color can be controlled when a fluorescent pigment is added to Alq_3.

However, the example given above represents merely one example of the organic EL materials that can be used for the EL layer, and does not restrict the invention. The EL layer (the layer for luminescence and for moving the carrier for luminescence) may be formed by freely combining the luminescence layer, the charge transportation layer and the charge injection layer. Though this example uses the low molecular weight organic EL material for the EL layer, it can use a polymeric organic EL material, too. Inorganic materials such as silicon carbide can also be used for the charge transportation layer and the charge injection layer. Known materials can be used for these organic EL materials and the inorganic materials.

Next, a cathode 4413 comprising a shading conductive film is disposed on the EL layer 4412. In this example, an alloy film of aluminum and lithium is used for the shading conductive film. Needless to say, a known MgAg film (an alloy film of magnesium and silver) may be used, too. A conductive film made of the elements belonging to the Group 1 or 2 of the Periodic Table, or a conductive film containing any of these elements may be used for the cathode materials.

The EL cell 4414 is completed at the point of time when this cathode 4413 is completed. Incidentally, the term "EL cell 4414" hereby used means a capacitor comprising the pixel electrode (anode) 4410, the EL layer 4412 and the cathode 4413.

Next, the top structure of the pixel in this example will be explained with reference to FIG. 27A. The source of the switching TFT 4402 is connected to the source wiring 4415 and the drain is connected to the drain wiring 4405. The drain wiring 4405 is electrically connected to the gate electrode 4407 of the current controlling TFT 4406. The source of the current controlling TFT 4406 is electrically connected to a current supply line 4416 and the drain is electrically connected to the drain wiring 4417. The drain wiring 4417 is electrically connected to the pixel electrode (anode) 4418 represented by dotted line.

At this time, a holding capacitance is formed in a region represented by reference numeral 4419. The holding capacitance 4419 is defined by a semiconductor film 4420 electrically connected to the current supply line 4416, an insulation film (not shown) that is the same layer as the gate insulation film and the gate electrode 4407. A capacitance defined by the gate electrode 4407, the same layer (not shown) as the first inter-layer insulation film and the current supply line 4416 can also be used as the holding capacitance.

Incidentally, the construction of this example can be freely combined with the construction of any of Examples 1 to 4, 6 and 8 to 22 and 25.

[Example 29]

In this example, explanation will be given with reference to FIG. 28 on the EL display device that has a different pixel structure from that of Example 28. For the explanation of the portions indicated by the same reference numerals as those in FIG. 26, reference should be made to the explanation of Example 26.

Referring to FIG. 28, a TFT having the same structure as that of the n-channel TFT 182 shown in FIG. 3C is used for the current controlling TFT 4501. Needless to say, the gate electrode 4502 of the current controlling TFT 4501 is connected to the drain wiring 4405 of the switching TFT 4402. The drain wiring 4503 of the current controlling TFT 4501 is electrically connected to the pixel electrode 4504.

In this example, the pixel electrode 4504 functions as the cathode of the EL cell, and is formed of a shading conductive film. More concretely, an alloy film of aluminum and lithium is used, but a conductive film made of any of the elements belonging to the Group 1 or 2 of the Periodic Table or a conductive film added with these elements may be used.

The EL layer 4505 is formed on the pixel electrode 4504. Though FIG. 28 shows only one pixel, the EL layer corresponding to G (green) is formed in practice by vapor deposition and coating (preferably, spin coating) in this example. More concretely, the EL layer has a laminate structure in which a 20 nm-thick lithium fluoride (LiF) film is disposed as the electron injection layer and a 70 nm-thick PPV (poly-paraphenylene vinylene) film is disposed as the luminescence layer on the LiF film.

Next, the anode 4506 comprising a transparent conductive film is disposed on the EL layer 4505. In this example, a conductive film made of a compound between indium oxide and tin oxide or a compound between indium oxide and zinc oxide is used as the transparent conductive film.

The EL cell 4507 is completed at the point when this anode

4506 is formed. Incidentally, the term "EL cell 4507" used hereby means a capacitor comprising the pixel electrode (cathode) 4504, the EL layer 4505 and the anode 4506.

At this time, it is of utmost importance that the current controlling TFT 4501 has the construction of the present invention. The current controlling TFT 4501 is a device for controlling the quantity of the current flowing through the EL cell 4507. Therefore, a large quantity of the current flows through this TFT and the TFT has a high possibility of degradation by heat and degradation by hot carriers. Therefore, the construction of the present invention, wherein the LDD region 4509 is so disposed as to overlap with the gate electrode 4502 through the gate insulation film 4508 on the drain side of the current controlling TFT 4501, is extremely effective.

The current controlling TFT 4501 in this example forms also a parasitic capacitance called a "gate capacitance" between the gate electrode 4502 and the LDD region 4509. The function equivalent to the holding capacitance 4419 shown in FIGs. 27A and 27B can be achieved by adjusting this gate capacitance. Particularly when the EL display device is operated in a digital driving system, the capacitance of the holding capacitance may be smaller than when the EL display device is driven by an analog driving system. Therefore, the gate capacitance can substitute the holding capacitance.

Incidentally, the construction of this example can be freely combined with the construction of Examples 1 to 4, 6 and 8 to 22 and 25.

[Example 30]

This example represents an example of a pixel structure that can be used for the pixel unit of the EL display device shown in Example 28 or 29, with reference to FIGs. 29A, 29B and 29C. In this example, reference numeral 4601 denotes a source wiring of a switching TFT 4602 and reference numeral 4603 denotes a gate wiring of the switching TFT 4602. Reference numeral 4604 denotes a current controlling TFT and reference numeral 4605 denotes a capacitor. Reference numerals 4606 and 4608 denote current supply lines and reference numeral 4607 denotes an EL cell.

FIG. 29A shows an example where the current supply line 4606 is shared in common between two pixels. In other words, this example has the feature in that two pixels are formed in symmetry of line with the current supply line 4606 as the center. In this case, since the number of current supply lines can be reduced, the pixel unit can be further miniaturized.

FIG. 29B shows an example where the current supply line 4608 is disposed in parallel with the gate wiring 4603. Incidentally, FIG. 29B shows a structure in which the current supply line 4608 and the gate wiring 4603 do not overlap with each other, but they may overlap with each other through an insulation film so long as they are formed in different layers. In this case, since the occupying area can be shared between the power supply line 4608 and the gate wiring 4603, the pixel unit can be further miniaturized.

The feature of the construction shown in FIG. 29C lies in that the current supply line 4608 is disposed in parallel with the gate wiring 4603 in the same way as in FIG. 29B, and that the two pixels are arranged in symmetry of line with the current supply line 4608 as the center. It is also effective to dispose the current supply line 4608 in such a fashion as to overlap with either one of the gate wirings 4603. In this case, since the number of current supply lines can be decreased, the pixel unit can be further miniaturized.

[Example 31]

The electro-optical device and the semiconductor circuit according to the present invention can be used for the display portion of electrical appliances and signal processing circuits. Such electric appliances include video cameras, digital cameras, projectors, projection TVs, goggle type displays, head-mount displays, navigation systems, audio reproduction apparatuses, notebook type personal computers, game machines, portable information terminals (mobile computers, cellular telephones, portable game machines, electronic books, etc.), image reproduction apparatuses equipped with a recording medium, and so forth. FIGs. 30A to 30F, 31A to 31D, 32A and 32B show concrete examples of such electric appliances.

FIG. 30A shows the cellular telephone, which comprises a main body 2001, a sound output unit 2002, a sound input unit 2003, a display unit 2004, an operation switch 2005 and an antenna 2006. The electro-optical device of the present invention can be used for this display unit 2004, and the semiconductor circuit of the present invention can be used for the sound output unit 2002, the sound input unit 2003 or the CPU and the memory.

FIG. 30B shows the video camera, which comprises a main body 2101, a display unit 2102, a sound input unit 2103, an operation switch 2104, a battery 2105 and an image reception unit 2106. The electro-optical device of the present invention can be used for the display unit 2102, and the semiconductor circuit of the present invention can be used for the sound input unit 2103 or the CPU and the memory.

FIG. 30C shows the mobile computer, which comprises a main body 2201, a camera unit 2202, an image reception unit 2203, an operation switch 2204 and a display unit 2205. The electro-optical device of the present invention can be used for the display unit 2205, and the semiconductor circuit of the present invention can be used for the CPU and the memory.

FIG. 30D shows the goggle type display, which comprises a main body 2301, a display unit 2302 and an arm unit 2303. The electro-optical device of the present invention can be used for the display unit 2302, and the semiconductor circuit of the present invention can be used for the CPU and the memory.

FIG. 30E shows the rear projector or the projection TV, which comprises a main body 2401, a light source 2402, a liquid crystal display device 2403, a polarization beam splitter 2404, reflectors 2405 and 2406 and a screen 2407. The present invention can be applied to the liquid crystal display device 2403, and the semiconductor circuit of the present invention can be used for the CPU and the memory.

FIG. 30F shows the front projector, which comprises a main body 2501, a light source 2502, a liquid crystal display device 2503, an optical system 2504 and a screen 2505. The present invention can be applied to the liquid crystal display device 2503, and the semiconductor circuit of the present invention can be used for the CPU and the memory.

FIG. 31A shows the personal computer, which comprises a main body 2601, an image input unit 2602, a display unit 2603, a keyboard 2604 and so forth. The electro-optical device of the present invention can be used for the display unit 2603, and the semiconductor circuit of the present invention can be used for the CPU and the memory.

FIG. 31B shows the electronic game machine, which comprises a main body 2701, a memory medium 2702, a display unit 2703 and a controller 2704. The sound and the image outputted from this electronic game machine are reproduced by a display including a casing 2705 and a display unit 2706. Wired communication, wireless communication or optical communication can be used as communication means between the controller 2704 and the main body 2701 or between the electronic game machine and the display. In this example, sensor units 2707 and 2708 detect infrared rays.

The electro-optical device of the present invention can be used for the display units 2703 and 2706, and the semiconductor circuit of the present invention can be used for the CPU and the memory.

FIG. 31C shows a player (image reproduction apparatus) using a recording medium having a program recorded thereon (hereinafter called the "recording medium"). The player comprises a main body 2801, a display unit 2802, a speaker unit 2803, a recording medium 2804 and an operation switch 2805. Incidentally, this image reproduction apparatus uses a DVD (Digital Versatile Disc), a CD and so forth as the recording medium, and can enjoy listening to music, movies, games and Internet communication. The electro-optical device of the present invention can be used for the display unit 2802, the CPU and the memory.

FIG. 31D shows the digital camera, which comprises a main body 2901, a display unit 2902, an eyepiece unit 2903, an operation switch 2904 and an image reception unit (not shown). The electro-optical device of the present invention can be used for the display unit 2902, the CPU and the memory.

FIGs. 32A and 32B show detailed explanation of the optical engine that can be used for the rear projector shown in FIG. 30E and the front projector shown in FIG. 30F. Incidentally, FIG. 32A shows the optical engine and FIG. 32B shows the light source optical system that is assembled in the optical engine.

The optical engine shown in FIG. 32A includes a light source optical system 3001, mirrors 3002, 3005, 3006 and 3007, dichroic mirrors 3003 and 3004, optical lenses 3008a, 3008b and 3008c, a prism 3011, liquid crystal display devices 3010 and a projection optical system 3012. The projection optical system 3012 is the optical system that is equipped with a projection lens. Though this example illustrates a three-plate system using three liquid crystal display devices 3010, a single plate system may also be used. Optical lenses, a film having a polarization function, a film for adjusting a phase difference, an IR film and so forth, may be disposed in the optical paths represented by arrows drawn in FIG. 32A.

As shown in FIG. 32B, the light source optical system 3001 includes light sources 3013 and 3014, a synthetic prism 3015, collimator lenses 3016 and 3020, lens arrays 3017 and 3018, and a polarization-conversion element 3019. Though the light source optical system shown in FIG. 32B uses two light sources, the light source may be one, or three or more. Optical lenses, a film having a polarization function, a film for adjusting a phase difference, an IR film and so forth, may be inserted into any positions of the light source optical system.

As described above, the range of the application of the present invention is extremely broad, and the present invention can be applied to electric/electronic appliances of all fields. The electric/electronic appliances of this example can be accomplished by any combination of Examples 1 to 30.

The present invention makes it possible to arrange those circuits that have appropriate performance in accordance with the required specifications, and to drastically improve the operation performance and the reliability of a semiconductor device (more concretely, the electro-optical device).

The present invention can form the holding capacitance having a large capacity with a small area in the pixel unit of the electro-optical device typified by the AM-LCD. Therefore, the present invention can secure a sufficient holding capacity even in the AM-LCD having an interior opposing angle of not greater than 1 inch without lowering the aperture ratio.

Moreover, the present invention can improve the operation performance and the reliability of a semiconductor device (more concretely, the electrical appliance) including the electro-optical device used as a display medium.

What is claimed is:

1. A semiconductor device including a pixel unit and a driving circuit which are formed over a substrate, wherein:

a first LDD region of an n-channel TFT forming said driving circuit is formed in such a fashion that a part or the whole part of said first LDD region overlaps with a gate wiring of said n-channel TFT while sandwiching a gate insulation film between them; and

a second LDD region of a pixel TFT forming said pixel unit is formed in such a fashion that said second LDD region does not overlap with a gate wiring of said pixel TFT while sandwiching a gate insulation film between them.

2. A semiconductor device including a pixel unit and a driving circuit which are formed over a substrate, wherein:

a first LDD region of an n-channel TFT forming said driving circuit is formed in such a fashion that a part or the whole part of said first LDD region overlaps with a gate wiring of said n-channel TFT while sandwiching a gate insulation film between them;

a second LDD region of a pixel TFT forming said pixel unit is formed in such a fashion that said second LDD region does not overlap with a gate wiring of said pixel TFT while sandwiching a gate insulation film between them; and

a holding capacitance of said pixel unit comprises a shading film disposed on a resin film, an oxide of said shading film, and a pixel electrode disposed on said oxide.

3. A semiconductor device including a pixel unit and a driving circuit which are formed over a substrate, wherein:

said driving circuit includes a first n-channel TFT formed in such a fashion that the whole part of at least one first LDD region overlaps with a gate wiring while sandwiching a gate insulation film between them and a second n-channel TFT formed in such a fashion that a part of at least one second LDD region overlaps with a gate wiring while sandwiching a gate insulation film between them; and

said pixel unit includes a pixel TFT formed in such a fashion that at least one third LDD region does not overlap with a gate wiring while sandwiching a gate insulation film between them.

4. A semiconductor device including a pixel unit and a driving circuit which are formed over a substrate, wherein:

said driving circuit includes a first n-channel TFT formed in such a fashion that the whole part of at least one first LDD region overlaps with a gate wiring while sandwiching a gate insulation film between them and a second n-channel TFT formed in such a fashion that a part of at least one second LDD region overlaps with a gate wiring while sandwiching a gate insulation film between them;

said pixel unit includes a pixel TFT formed in such a fashion that at least one third LDD region does not overlap with a gate wiring while sandwiching a gate insulation film between them; and

a holding capacitance of said pixel unit comprises a shading film disposed on a resin film, an oxide of said shading film, and a pixel electrode disposed on said oxide.

5. A semiconductor device according to claim 1 or 2, wherein said first LDD region contains an element belonging to the Group 15 of the Periodic Table in a higher concentration than said second LDD region.

6. A semiconductor device according to claim 3 or 4, wherein said at least one first LDD region and said at least one second LDD region contain an element belonging to the Group 15 of the Periodic Table in a higher concentration than said at least one third LDD region.

7. A semiconductor device according to claim 1 or 2,

wherein said first LDD region contains an element belonging to the Group 15 of the Periodic Table in a concentration higher by 2 to 10 times than a concentration in said second LDD region.

8. A semiconductor device according to claim 3 or 4, wherein said at least one first LDD region and said at least one second LDD region contain an element belonging to the Group 15 of the Periodic Table in a concentration higher by 2 to 10 times than a concentration in said at least one third LDD region.

9. A semiconductor device according to claim 3 or 4, wherein said at least one first LDD region is formed between a channel formation region and a drain region, and said at least one second LDD region is so formed as to sandwich a channel formation region.

10. A semiconductor device according to claim 2 or 4, wherein said shading film is formed of an aluminum film or a film consisting essentially of aluminum as the principal component.

11. A semiconductor device according to claim 2 or 4, wherein said oxide is a film comprising an aluminum oxide.

12. A semiconductor device according to any of claims 1 through 4, wherein said pixel unit includes an EL cell.

13. An electric appliance using said semiconductor device according to any of claims 1 through 4 for the display part.

14. A method of fabricating a semiconductor device including a pixel unit and a driving circuit which are formed over a substrate, comprising the steps of:

forming a first channel formation region, a first source region, a first drain region and a first LDD region between said first drain region and said first channel formation region, in a first active layer of an n-channel TFT forming said driving circuit;

forming a second channel formation region, a second source region and a second drain region in a second active layer of a p-channel TFT forming said driving circuit; and

forming a third channel formation region, a third source region, a third drain region and a second LDD region between said third drain region and said third channel formation region, in a third active layer of a pixel TFT forming said pixel unit;

wherein said first LDD region is formed in such a fashion that a part or the whole part of said first LDD region overlaps with a gate wiring of said n-channel TFT while sandwiching a gate insulation film; and

said second LDD region of said pixel TFT is formed in such a fashion that said second LDD region does not overlap with a gate wiring of said pixel TFT while sandwiching a gate insulation film.

15. A method of fabricating a semiconductor device according to claim 14, wherein said first LDD region contains an element belonging to the Group 15 of the Periodic Table in a higher concentration than said second LDD region.

16. A method of fabricating a semiconductor device including a pixel unit and a driving circuit which are formed over a substrate, comprising the steps of:

forming a first channel formation region, a first source region, a first drain region and a first LDD region between said first drain region and said first channel formation region, in a first active layer of a first n-channel TFT forming said driving circuit;

forming a second channel formation region, a second source region, a second drain region, a second LDD region between said second source region and said second channel formation region and a second LDD region between said second drain region and said second channel formation region, in a second active layer of a second n-channel TFT forming said driving circuit;

forming a third channel formation region, a third source region and a third drain region in a third active layer of a p-channel TFT forming said driving circuit; and

forming a fourth channel formation region, a fourth source region, a fourth drain region and a third LDD region between said fourth drain region and said fourth channel formation region, in a fourth active layer of a pixel TFT forming said pixel unit;

wherein said first LDD region is formed in such a fashion that the whole part of said first LDD region overlaps with a gate wiring of said first n-channel TFT while sandwiching a gate insulation film between them;

said second LDD region is formed in such a fashion that a part of said second LDD region overlaps with a gate wiring of said second n-channel TFT while sandwiching a gate insulation film between them; and

said third LDD region of said pixel TFT is arranged in such a fashion as not to overlap with a gate wiring of said pixel TFT while sandwiching a gate insulation film.

17. A method of fabricating a semiconductor device according to claim 16, wherein said first LDD region and said second LDD region contain an element belonging to the Group 15 of the Periodic Table in a higher concentration than said third LDD region.

18. A method of fabricating a semiconductor device including a pixel unit and a driving circuit which are formed over a substrate, comprising:

a first step of forming at least a first active layer of a first n-channel TFT, a second active layer of a second n-channel TFT and a third active layer of a p-channel TFT over said substrate;

a second step of forming a gate insulation film in contact with said first active layer, said second active layer and said third active layer;

a third step of adding an element belonging to the Group 15 of the Periodic Table to said first active layer, in order to form at least one n^- region;

a fourth step of forming a conductive film on said gate insulation film;

a fifth step of performing a first patterning of said conductive film and forming a third gate wiring of said p-channel TFT;

a sixth step of adding an element belonging to the Group 13 of the Periodic Table in self-alignment to said third active layer with said third gate wiring as a mask, in order to form at least one p^{++} region;

a seventh step of performing a second patterning of said conductive film and forming a first gate wiring of said first n-channel TFT and a second gate wiring of said second n-channel TFT;

an eighth step of adding an element belonging to the Group 15 of the Periodic Table to said first active layer and said second active layer, in order to form at least one n^+ region; and

a ninth step of adding an element belonging to the Group 15 of the Periodic Table in self-alignment using said second gate wiring as a mask, in order to form at least one n^{--} region,

wherein said driving circuit and said pixel unit comprise said first n-channel TFT and said second n-channel TFT respectively.

19. A method of fabricating a semiconductor device including a pixel unit and a driving circuit which are formed over a substrate, comprising:

a first step of forming a first active layer of a first n-channel TFT, a second active layer of a second n-channel TFT and a third active layer of a p-channel TFT over said substrate;

a second step of forming a gate insulation film in contact with said first active layer, said second active layer and said third active layer;

a third step of adding an element belonging to the Group 15 of the Periodic Table to said first active layer, in order to form at least one n^- region;

a fourth step of forming a conductive film on said gate insulation film;

a fifth step of performing a first patterning of said conductive film and forming a third gate wiring of said p-channel TFT;

a sixth step of adding an element belonging to the Group 13 of the Periodic Table in self-alignment to said third active layer with said third gate wiring as a mask, in order to form at least one p^{++} region;

a seventh step of performing a second patterning of said conductive film and forming a first gate wiring of said first n-channel TFT and a second gate wiring of said second n-channel TFT;

an eighth step of adding an element belonging to the Group 15 of the Periodic Table in self-alignment using said second gate wiring as a mask, in order to form at least one n^{--} region; and

a ninth step of adding an element belonging to the Group 15 of the Periodic Table to said first active layer and said second active layer, in order to form at least one n^+ region,

wherein said driving circuit and said pixel unit comprise said first n-channel TFT and said second n-channel TFT respectively.

20. A method of fabricating a semiconductor device including a pixel unit and a driving circuit which are formed

over a substrate, comprising:

a first step of forming a first active layer of a first n-channel TFT, a second active layer of a second n-channel TFT and a third active layer of a p-channel TFT over said substrate;

a second step of forming a gate insulation film in contact with said first active layer, said second active layer and said third active layer;

a third step of adding an element belonging to the Group 15 of the Periodic Table to said first active layer of said first n-channel TFT, in order to form at least one n^- region;

a fourth step of forming a conductive film on said gate insulation film;

a fifth step of performing a first patterning of said conductive film and forming a first gate wiring of said first n-channel TFT and a second gate wiring of said second n-channel TFT;

a sixth step of adding an element belonging to the Group 15 of the Periodic Table in self-alignment to said first active layer with said first gate wiring as a mask, in order to form at least one n^+ region;

a seventh step of performing a second patterning of said conductive film and forming a third gate wiring of said p-channel TFT;

an eighth step of adding an element belonging to the Group 13 of the Periodic Table in self-alignment to said third active layer, in order to form at least one p^{++} region; and

a ninth step of adding an element belonging to the Group 15 of the Periodic Table in self-alignment with said second gate wiring as a mask, in order to form at least one n^{--} region,

wherein said driving circuit and said pixel unit comprise said first n-channel TFT and said second n-channel TFT respectively.

21. A method of fabricating a semiconductor device including a pixel unit and a driving circuit which are formed over a substrate, comprising:

a first step of forming a first active layer of a first n-channel TFT, a second active layer of a second n-channel TFT and a third active layer of a p-channel TFT over said substrate;

a second step of forming a gate insulation film in contact with said first active layer, said second active layer and said third active layer;

a third step of adding an element belonging to the Group 15 of the Periodic Table to said first active layer, in order to form at least one n^- region;

a fourth step of forming a conductive film on said gate insulation film;

a fifth step of performing a first patterning of said conductive film and forming a first gate wiring of said first n-channel TFT and a second gate wiring of said second n-channel TFT;

a sixth step of adding an element belonging to the Group 15 of the Periodic Table in self-alignment to said first active layer with said first gate wiring as a mask, in order to form at least one n^+ region;

a seventh step of adding an element belonging to the Group 15 of the Periodic Table in self-alignment with said second gate wiring and said conductive film remaining over said third active layer as a mask, in order to form at least one n^{--} region;

an eighth step of performing a second patterning of said conductive film and forming a third gate wiring of said p-channel TFT; and

a ninth step of adding an element belonging to the Group 13 of the Periodic Table to said third active layer, in order to form at least one p^{++} region, wherein said driving circuit and said pixel unit comprise said first n-channel TFT and said second n-channel TFT respectively.

22. A method of fabricating a semiconductor device including a pixel unit and a driving circuit which are formed over a substrate, comprising:

a first step of forming a first active layer of a first n-channel TFT, a second active layer of a second n-channel TFT and a third active layer of a p-channel TFT over said substrate;

a second step of forming a gate insulation film in contact with said first active layer, said second active layer and said third active layer;

a third step of adding an element belonging to the Group 15 of the Periodic Table to said first active layer, in order to form at least one n^- region;

a fourth step of forming a conductive film on said gate insulation film;

a fifth step of performing a first patterning of said conductive film and forming a first gate wiring of said first n-channel TFT and a second gate wiring of said second n-channel TFT;

a sixth step of adding an element belonging to the Group 15 of the Periodic Table in self-alignment to said second active layer with said second gate wiring and said conductive film remaining over said third active layer as a mask, in order to form at least one n^{--} region;

a seventh step of adding an element belonging to the Group 15 of the Periodic Table to said first active layer and said second active layer, in order to form at least one n^+ region;

an eighth step of performing a second patterning of said conductive film remaining over said third active layer and forming a third gate wiring of said p-channel TFT; and a ninth step of adding an element belonging to the Group 13 of the Periodic Table to said second active layer and forming a p^{++} region,

wherein said driving circuit and said pixel unit comprise said first n-channel TFT and said second n-channel TFT respectively.

23. A method of fabricating a semiconductor device including a pixel unit and a driving circuit which are formed over a substrate, comprising:

a first step of forming a first active layer of a first n-channel TFT, a second active layer of a second n-channel TFT and a third active layer of a p-channel TFT over said substrate;

a second step of forming a gate insulation film in contact with said first active layer, said second active layer and said third active layer;

a third step of adding an element belonging to the Group 15 of the Periodic Table to said first active layer in order to form at least one n^- region;

a fourth step of forming a conductive film on said gate insulation film;

a fifth step of performing a first patterning of said conductive film and forming a first gate wiring of said first n-channel TFT and a second gate wiring of said second n-channel TFT;

a sixth step of adding an element belonging to the Group 15 of the Periodic Table in self-alignment to said second active layer with said second gate wiring and said conductive film remaining over said third active layer as a mask, in order to form at least one n^{--} region;

a seventh step of performing a second patterning of said conductive film remaining over said third active layer and forming a third gate wiring of said p-channel TFT;

an eighth step of adding an element belonging to the Group 13 of the Periodic Table to said third active layer, in order to form at least one p^{++} region; and

a ninth step of adding an element belonging to the Group 15 of the Periodic Table to said first active layer and said second active layer, in order to form at least one n^{+} region,

wherein said driving circuit and said pixel unit comprise said first n-channel TFT and said second n-channel TFT respectively.

24. A method of fabricating a semiconductor device according to any of claims 18 through 23, wherein said n^{-} region is formed in such a fashion that a part or a whole part of said n^{-} region overlaps with said first gate wiring while sandwiching said gate insulation film between them, and wherein said n^{--} region is formed in such a fashion as not to overlap with said second gate wiring while sandwiching said gate insulation film between them.

25. A method of fabricating a semiconductor device according to any of claims 18 through 23, wherein an element belonging to the Group 15 of the Periodic Table is added to said n^{-} region in a higher concentration than said n^{--} region.

26. A method of fabricating a semiconductor device according to any of claims 18 through 23, which further comprises the steps of:

forming an inter-layer insulation film comprising a resin material over said first n-channel TFT, said second n-channel TFT and said p-channel TFT;

forming a shading film on said inter-layer insulation film;

forming an oxide of said shading film on the surface of said shading film; and

forming a pixel electrode in such a fashion as to keep contact with said oxide of said shading film and to overlap with said shading film.

27. A method of fabricating a semiconductor device according to any of claims 18 through 23, which further comprises the steps of:

forming an inter-layer insulation film comprising a resin material over said first n-channel TFT, said second n-channel TFT and said p-channel TFT;

forming a shading film on said inter-layer insulation film;

forming an oxide of said shading film on the surface of said shading film; and

forming a pixel electrode in such a fashion as to keep contact with said oxide of said shading film and to overlap with said shading film,

wherein said shading film is an aluminum film or a film consisting essentially of aluminum as the principal component.

28. A method of fabricating a semiconductor device according to any of claims 18 through 23, which further comprises the steps of:

forming an inter-layer insulation film comprising a resin material over said first n-channel TFT, said second n-channel TFT and said p-channel TFT;

forming a shading film on said inter-layer insulation film;

forming an oxide of said shading film on the surface of said shading film; and

forming a pixel electrode in such a fashion as to keep contact with said oxide of said shading film and to overlap with said shading film,

wherein said shading film is an aluminum film or a film consisting essentially of aluminum as the principal component, and

wherein said oxide is an aluminum oxide film formed by one of an anodic oxidation method, a plasma oxidation method and a thermal oxidation method.

ABSTRACT OF THE DISCLOSURE

This invention provides a semiconductor device having high operation performance and high reliability. An LDD region 707 overlapping with a gate wiring is arranged in an n-channel TFT 802 forming a driving circuit, and a TFT structure highly resistant to hot carrier injection is achieved. LDD regions 717, 718, 719 and 720 not overlapping with a gate wiring are arranged in an n-channel TFT 804 forming a pixel unit. As a result, a TFT structure having a small OFF current value is achieved. In this instance, an element belonging to the Group 15 of the Periodic Table exists in a higher concentration in the LDD region 707 than in the LDD regions 717, 718, 719 and 720.

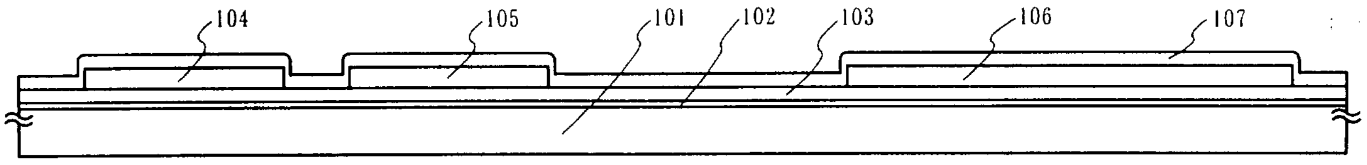


FIG. 1A

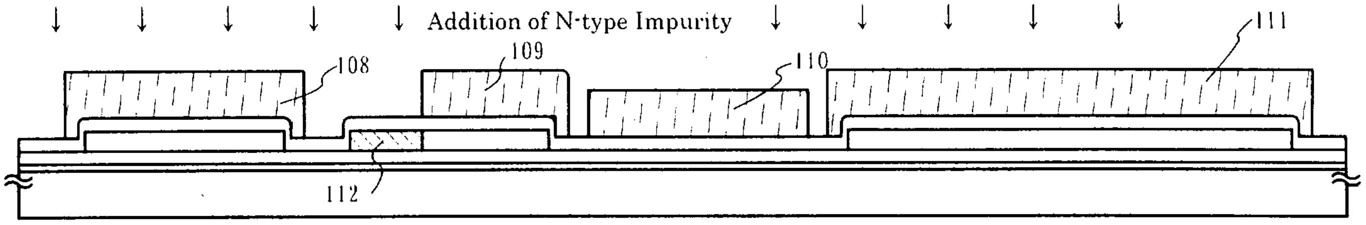


FIG. 1B

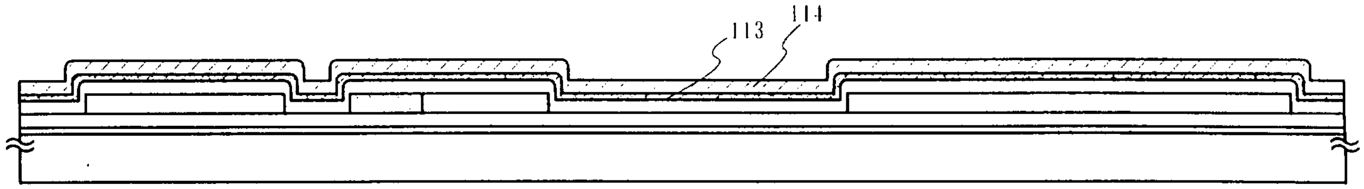


FIG. 1C

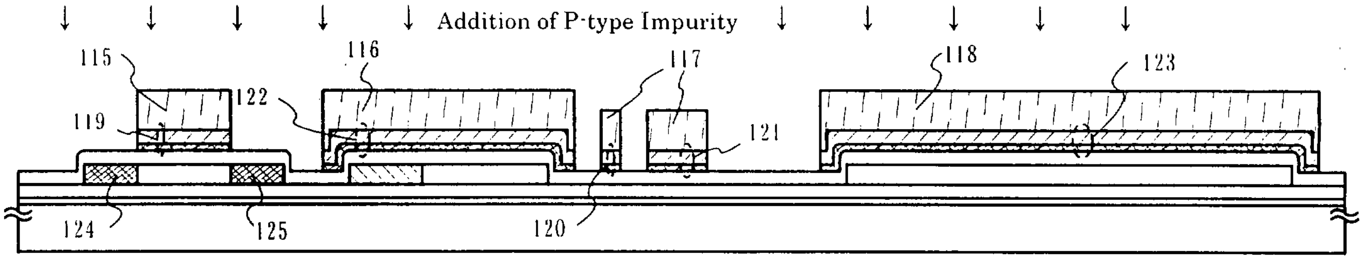


FIG. 2A

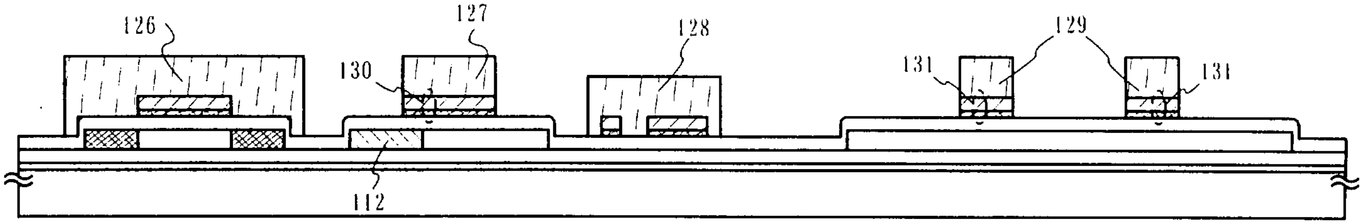


FIG. 2B

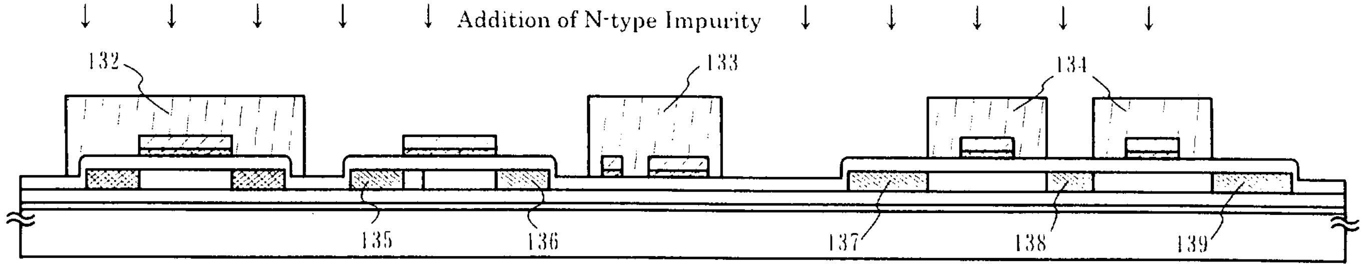


FIG. 2C

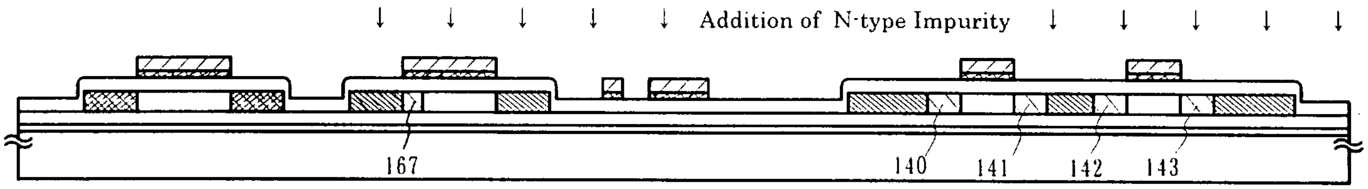


FIG. 3A

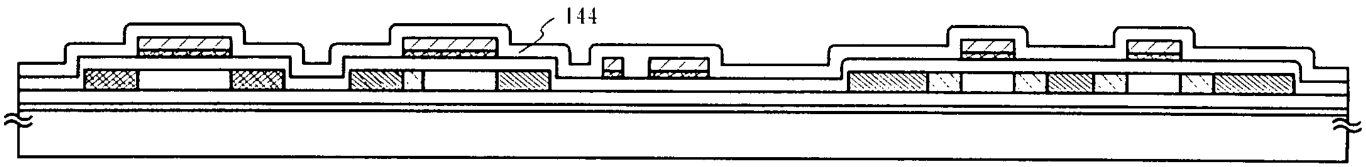


FIG. 3B

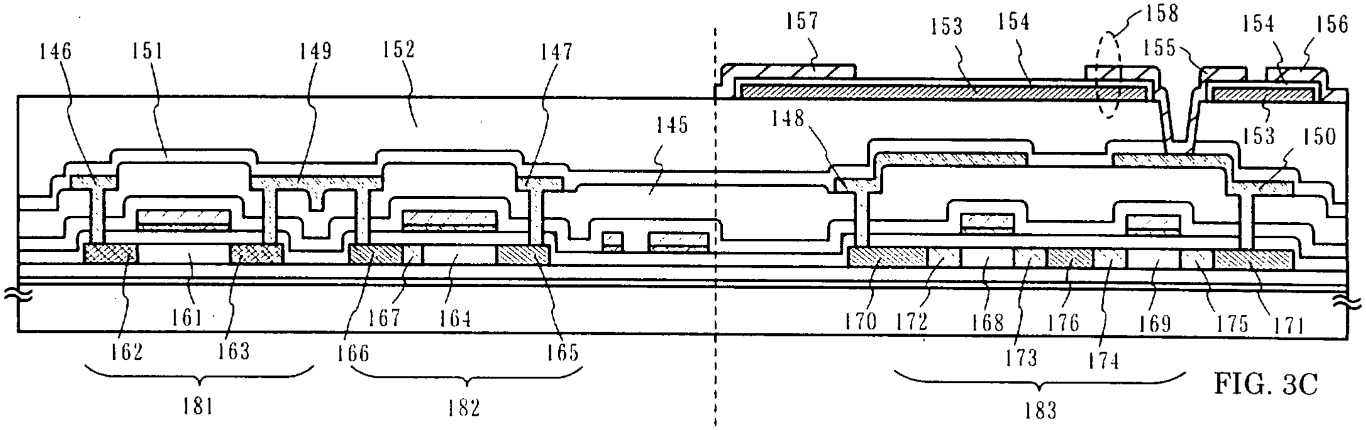


FIG. 3C

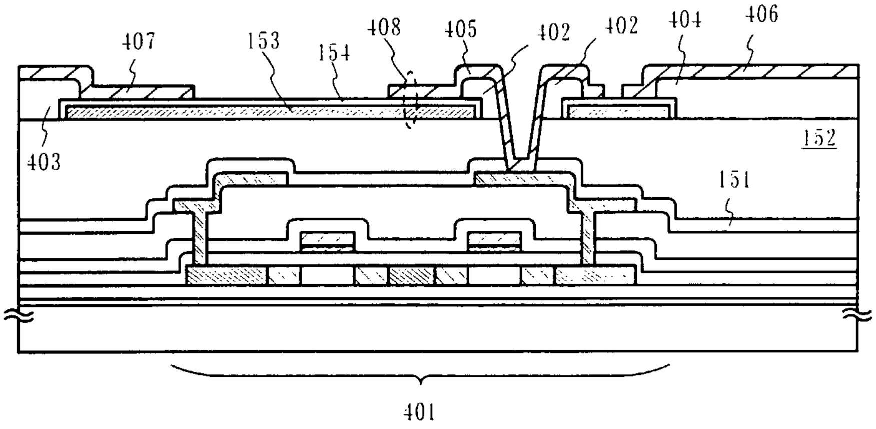


FIG. 4

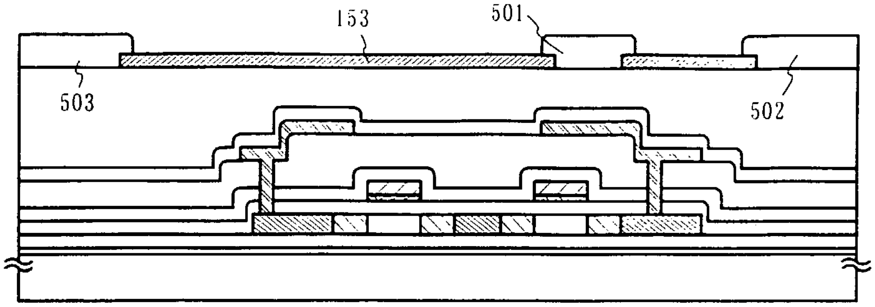


FIG. 5A

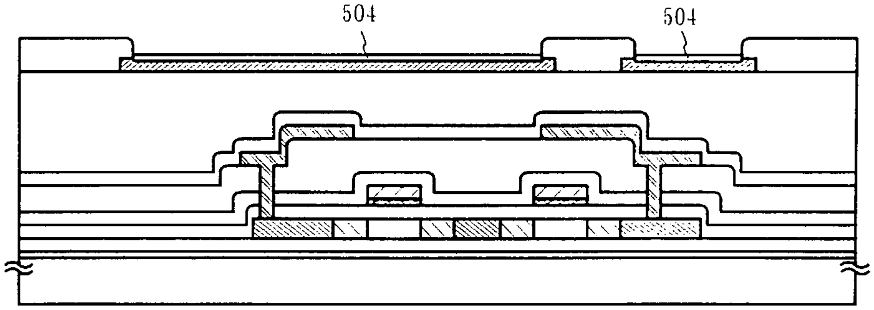


FIG. 5B

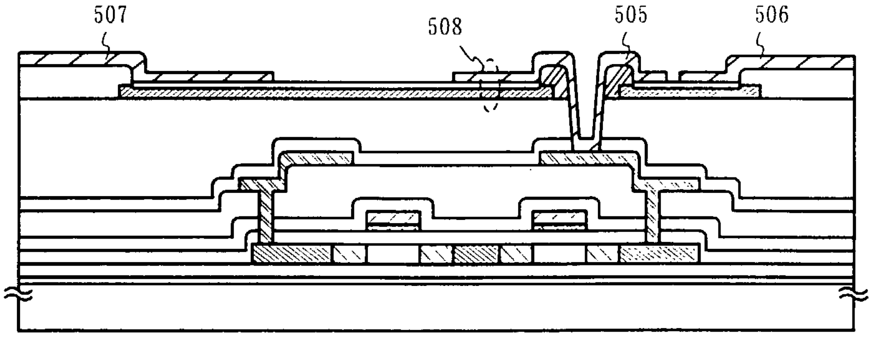


FIG. 5C

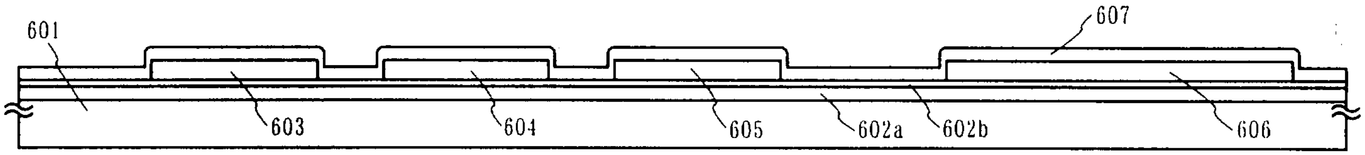


FIG. 6A

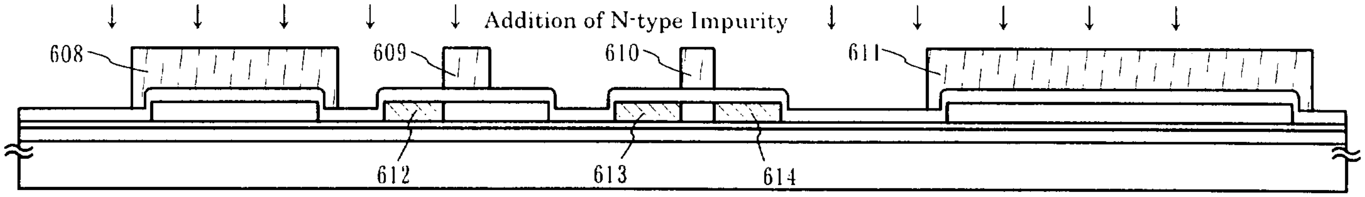


FIG. 6B

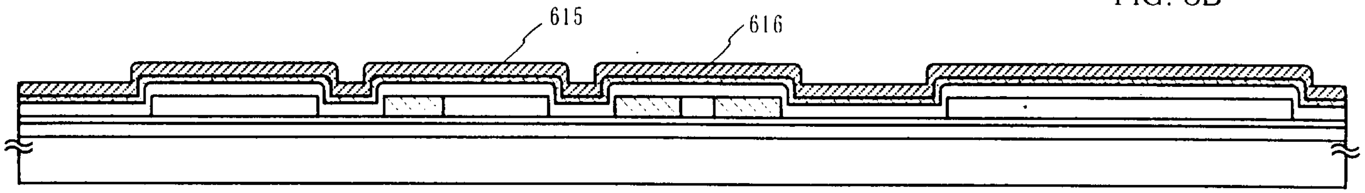


FIG. 6C

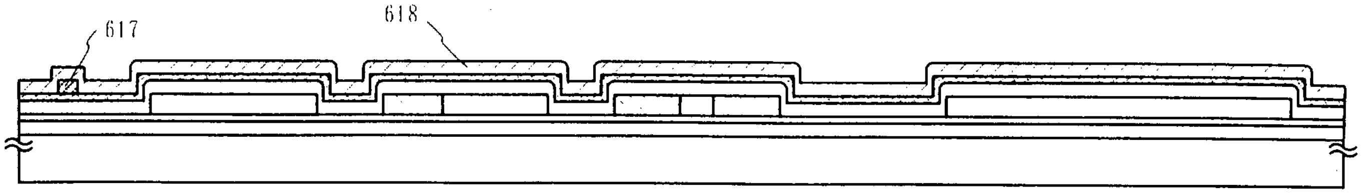


FIG. 6D

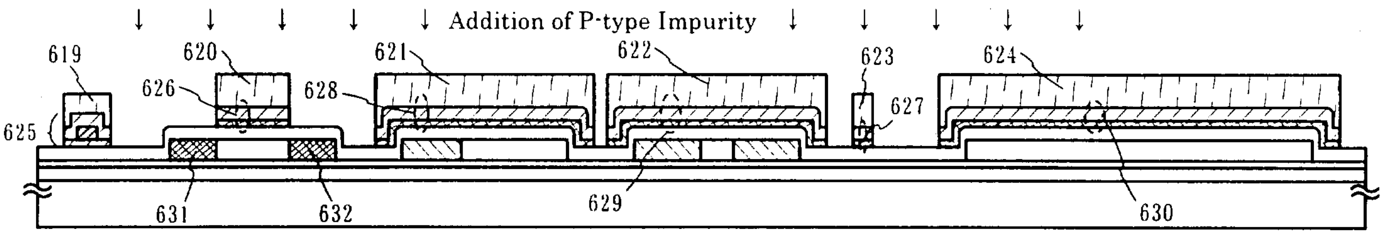


FIG. 7A

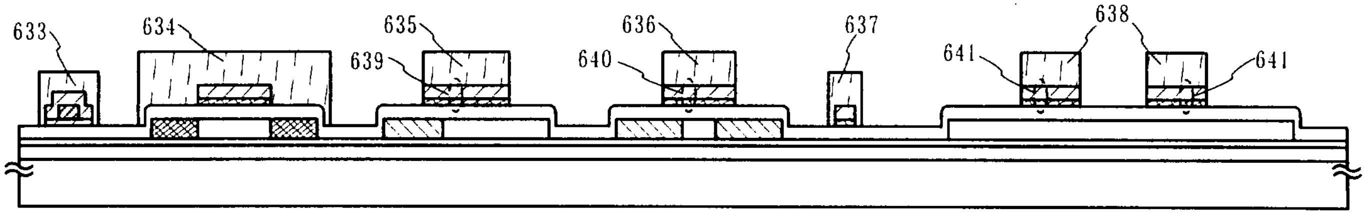


FIG. 7B

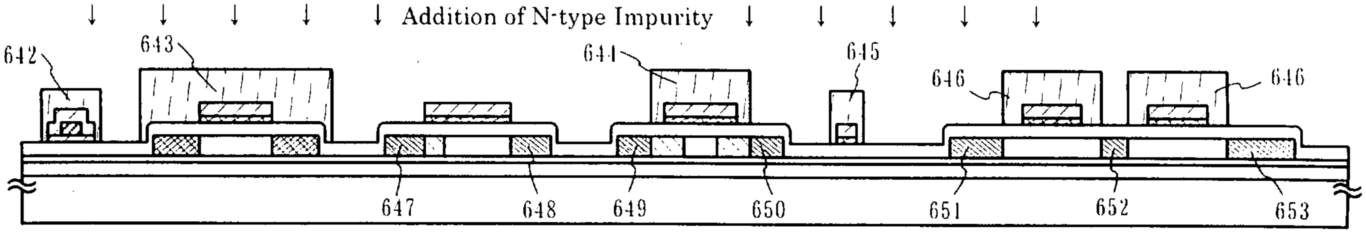


FIG. 7C

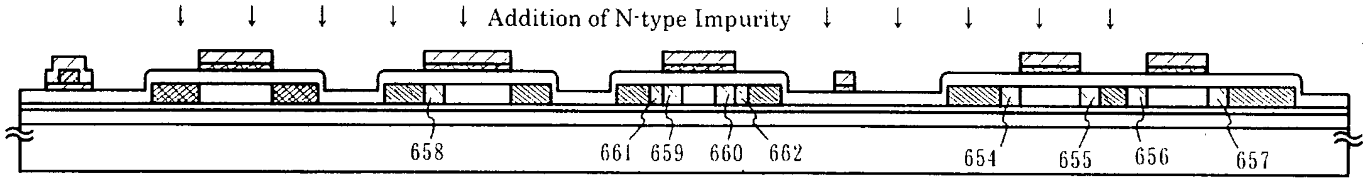


FIG. 8A

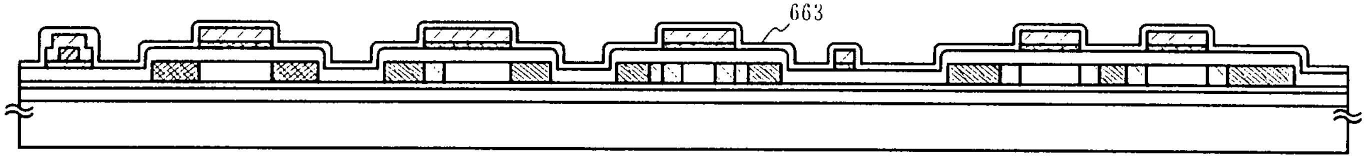


FIG. 8B

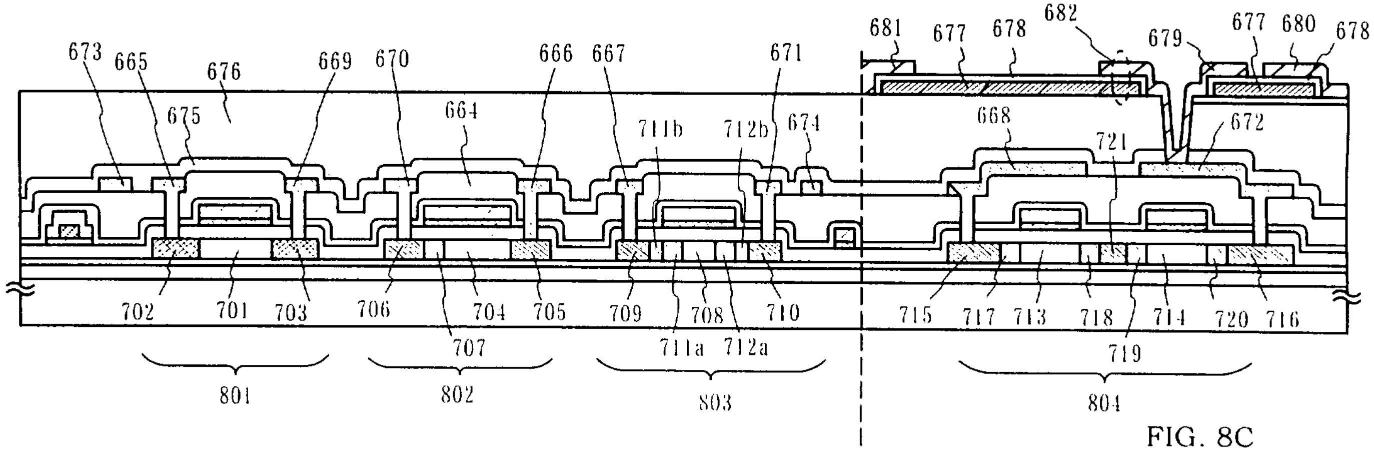


FIG. 8C

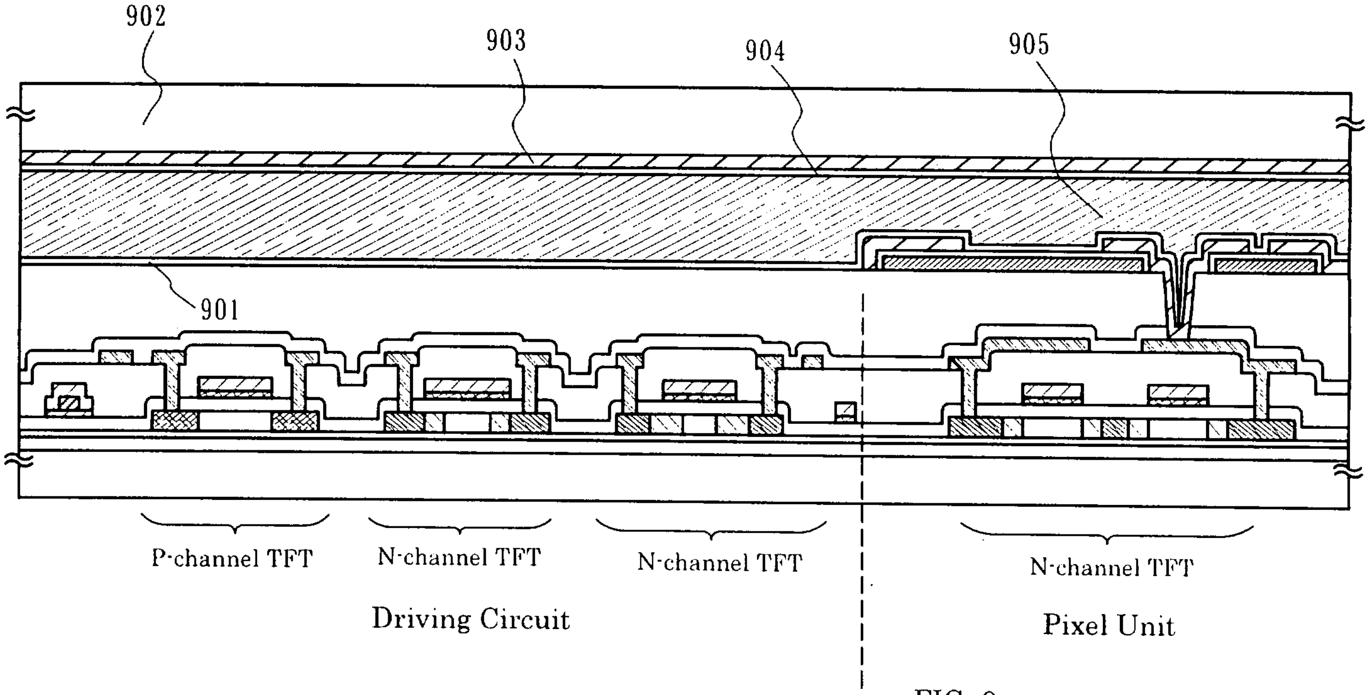

902
903
904
905
901
P-channel TFT
N-channel TFT
N-channel TFT
N-channel TFT
Driving Circuit
Pixel Unit

FIG. 9

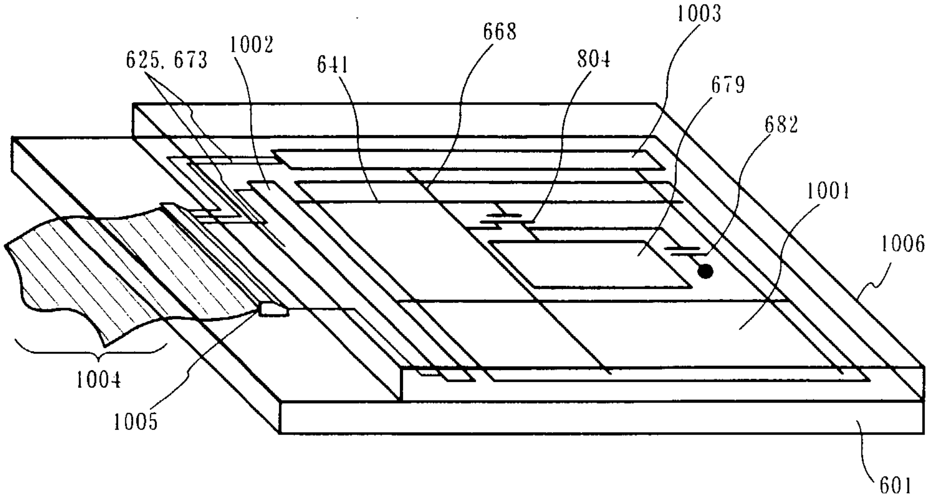


FIG. 10

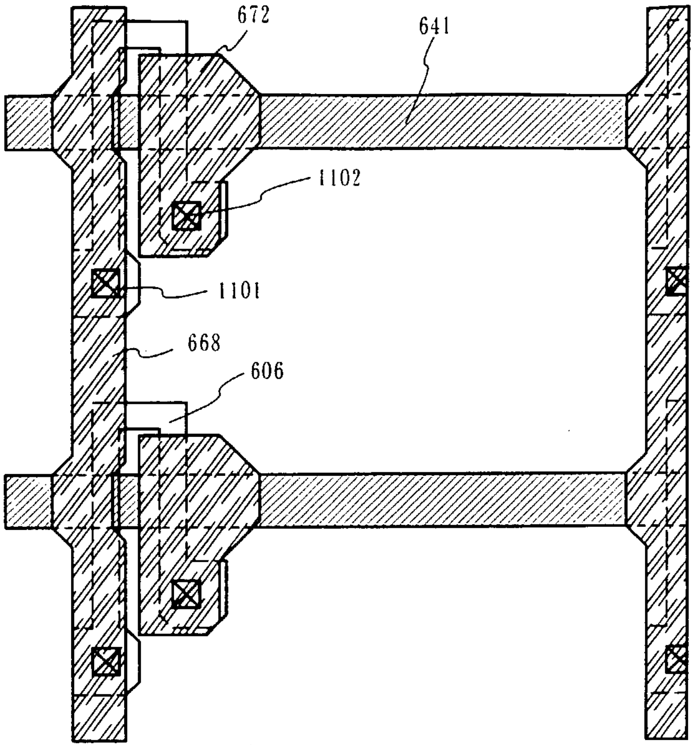


FIG. 11A

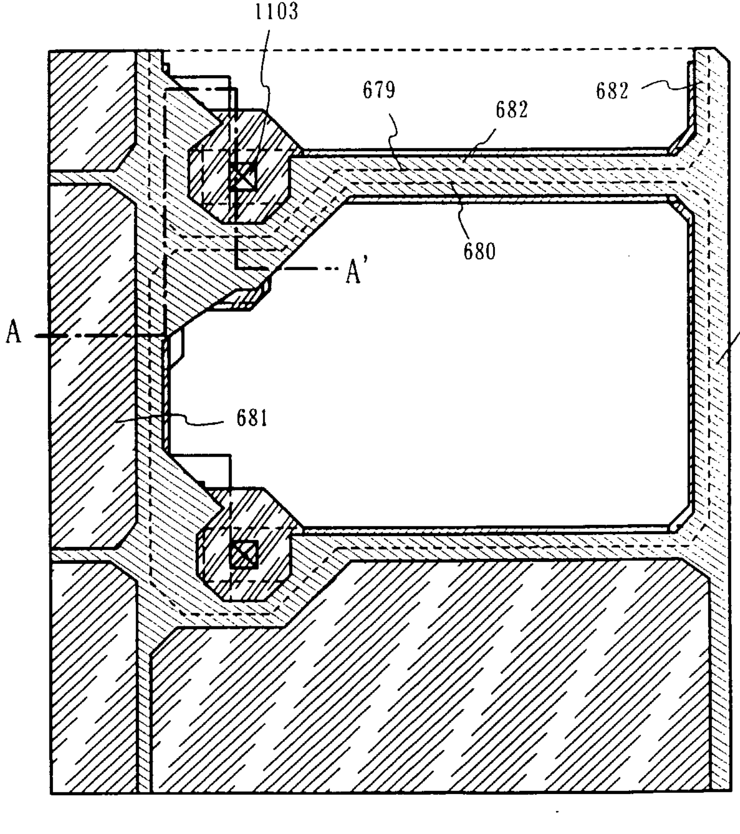


FIG. 11B

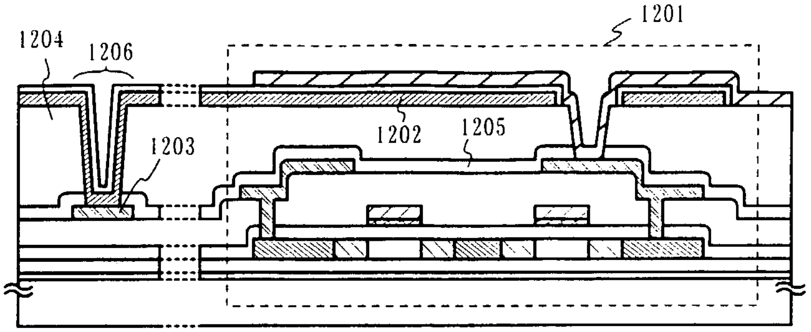


FIG. 12A

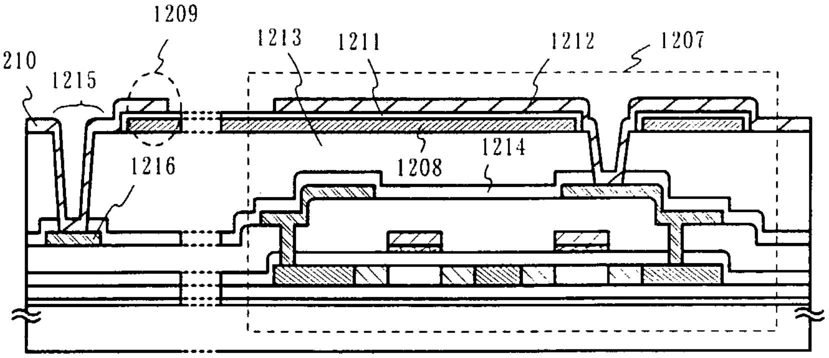


FIG. 12B

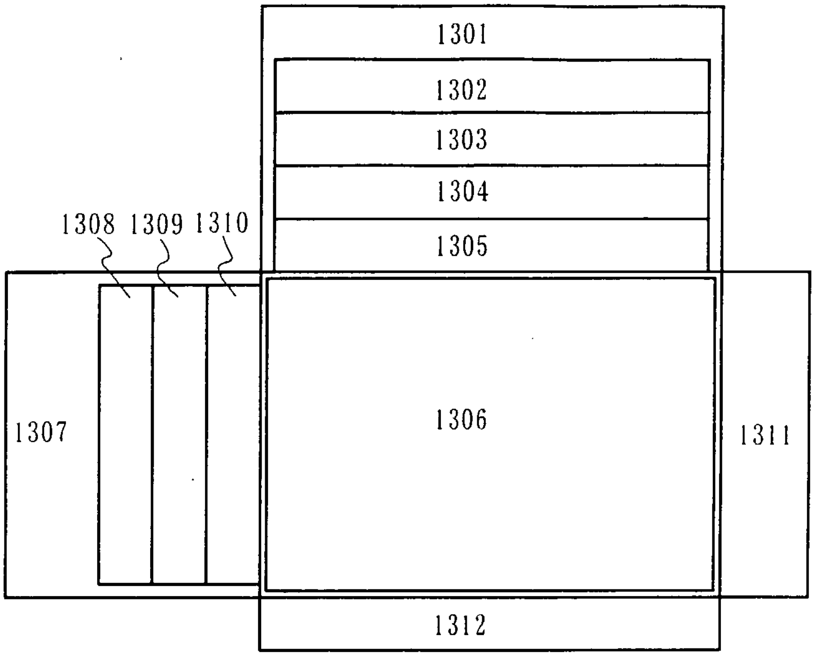


FIG. 13

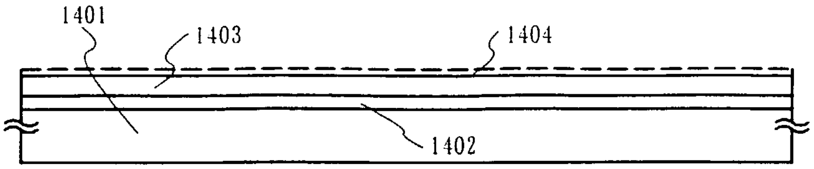


FIG. 14A

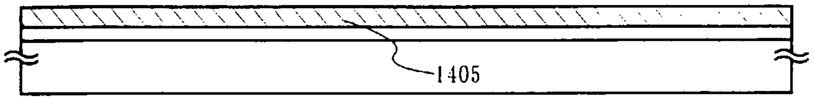


FIG. 14B

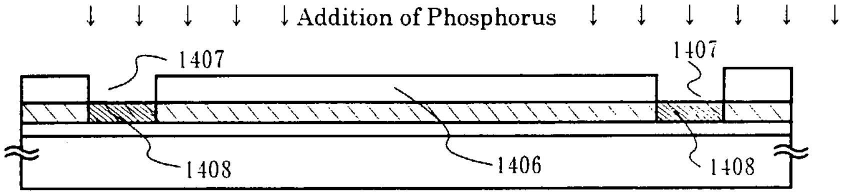


FIG. 14C

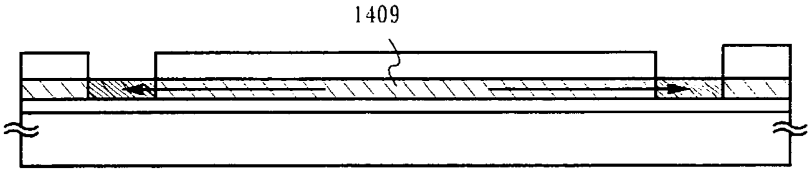


FIG. 14D

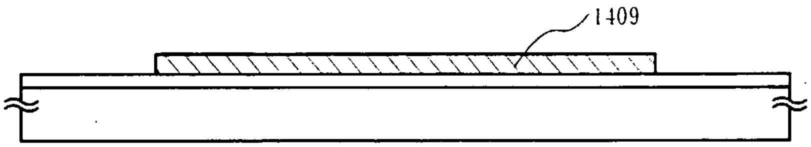


FIG. 14E

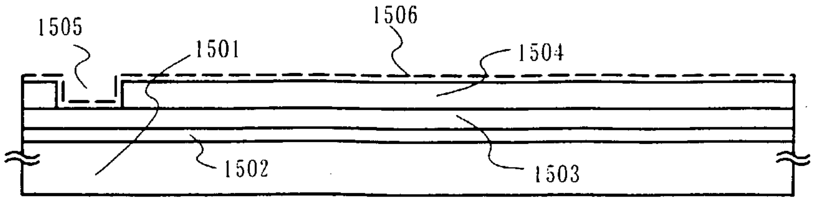


FIG. 15A

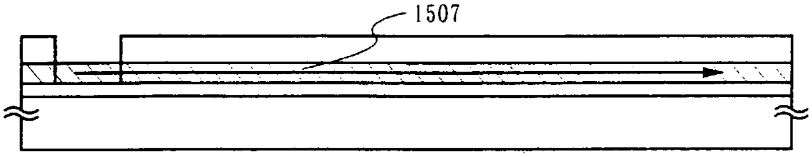


FIG. 15B

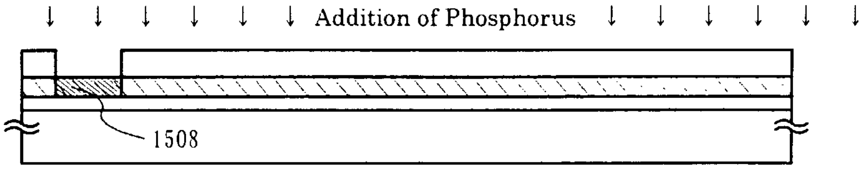


FIG. 15C

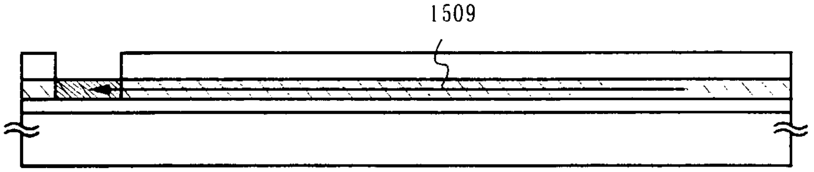


FIG. 15D

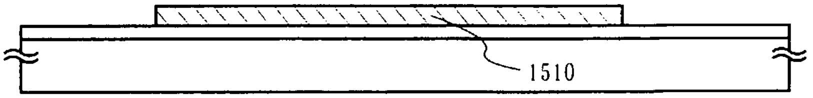


FIG. 15E

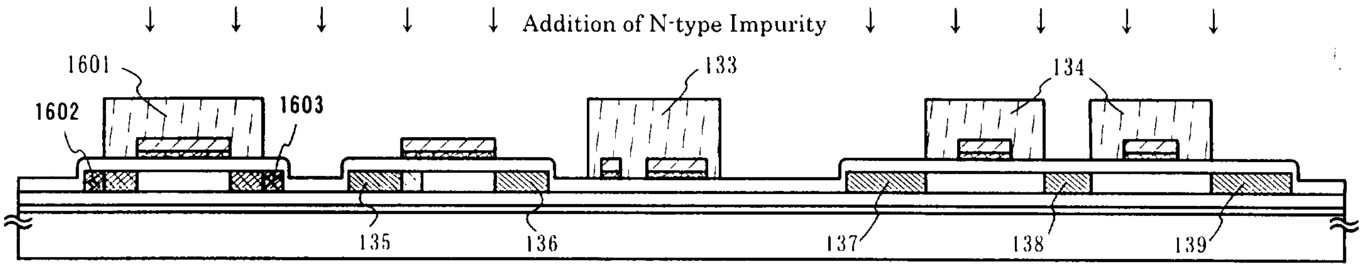


FIG. 16A

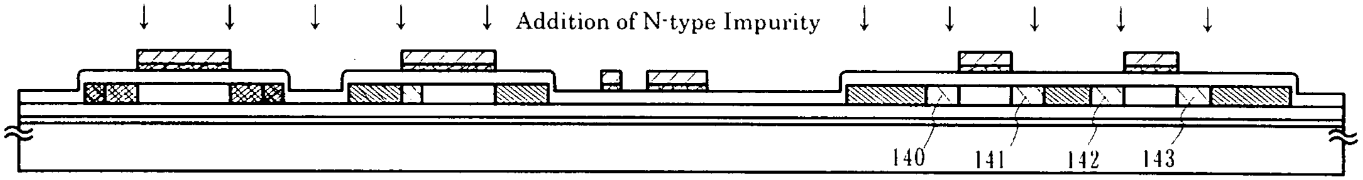


FIG. 16B

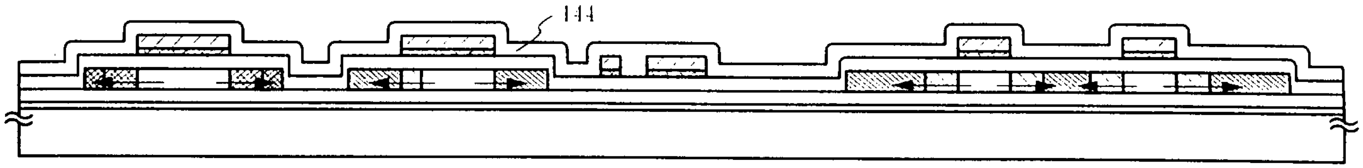


FIG. 16C

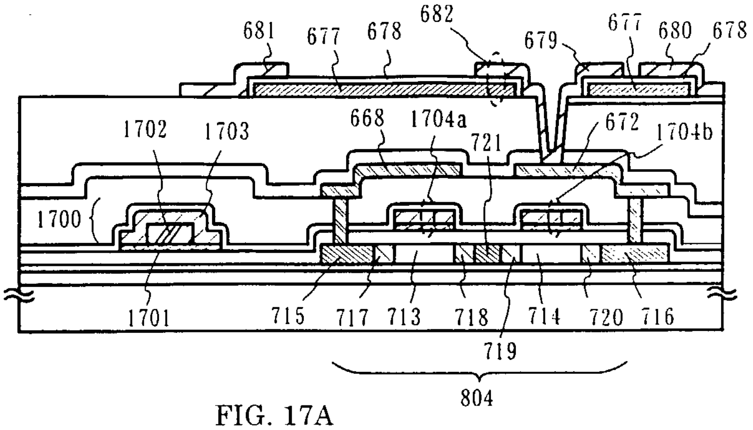


FIG. 17A

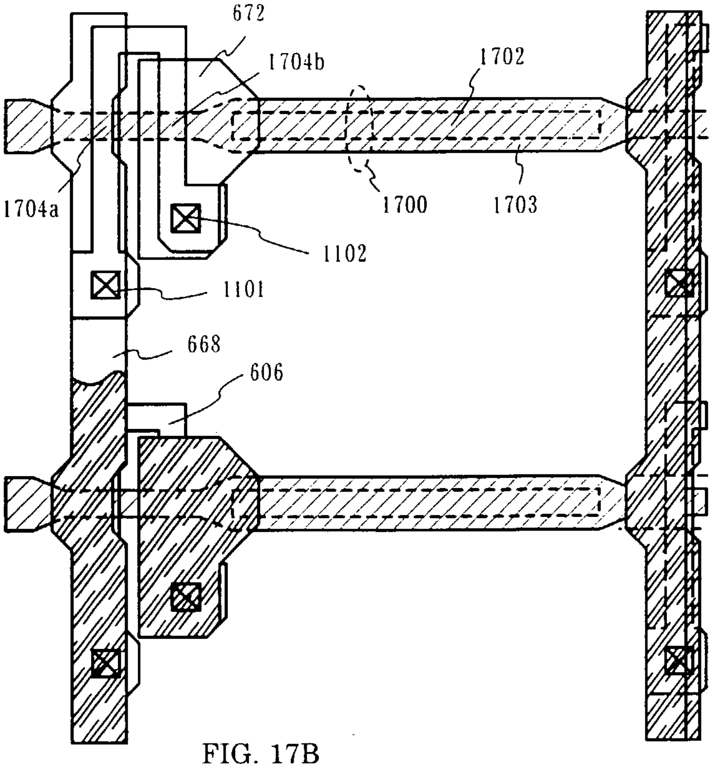


FIG. 17B

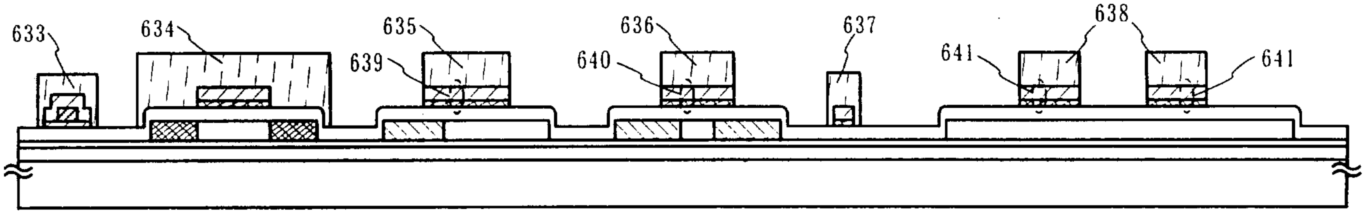


FIG. 18A

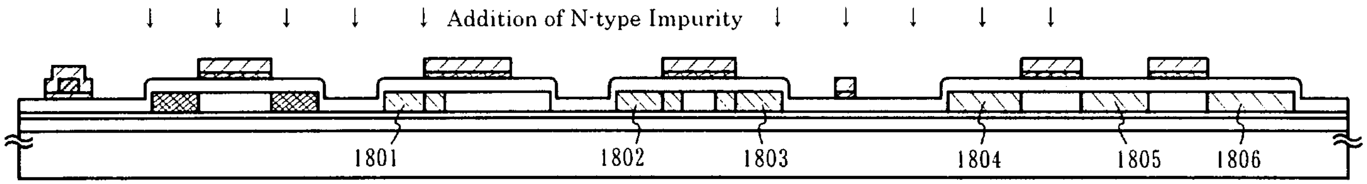


FIG. 18B

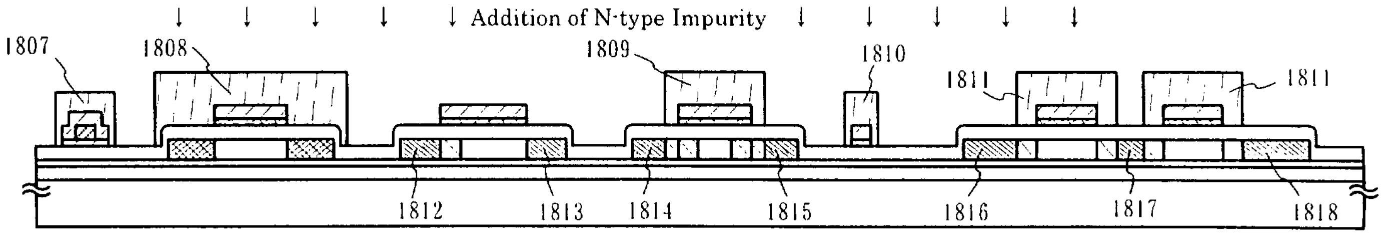


FIG. 18C

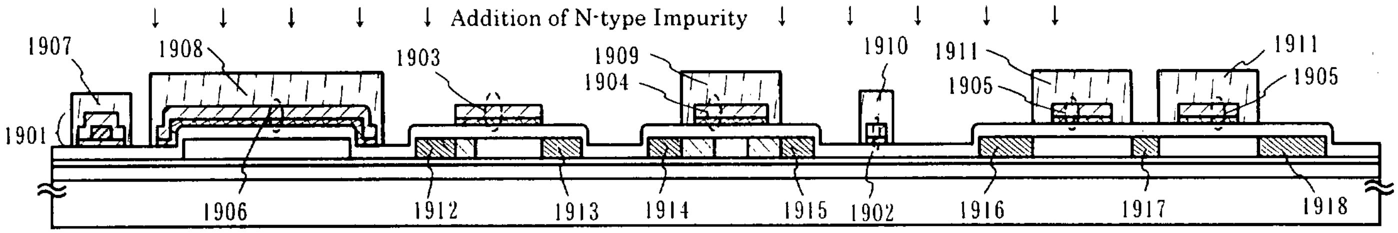


FIG. 19A

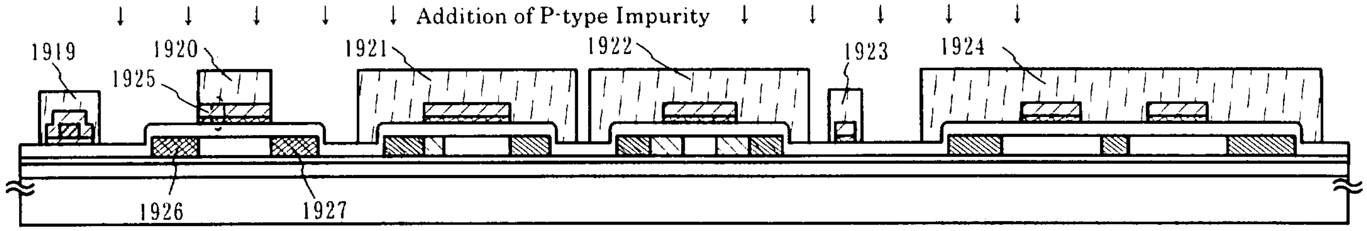


FIG. 19B

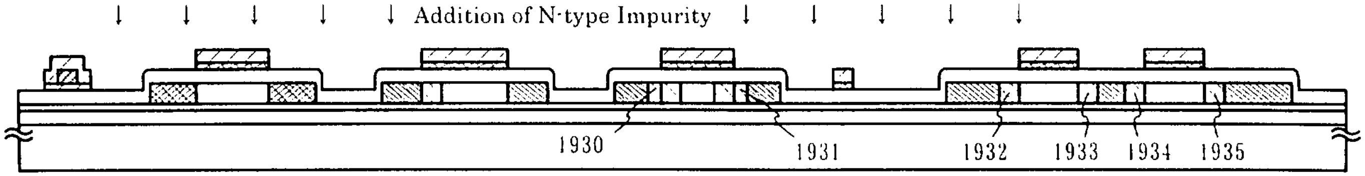


FIG. 19C

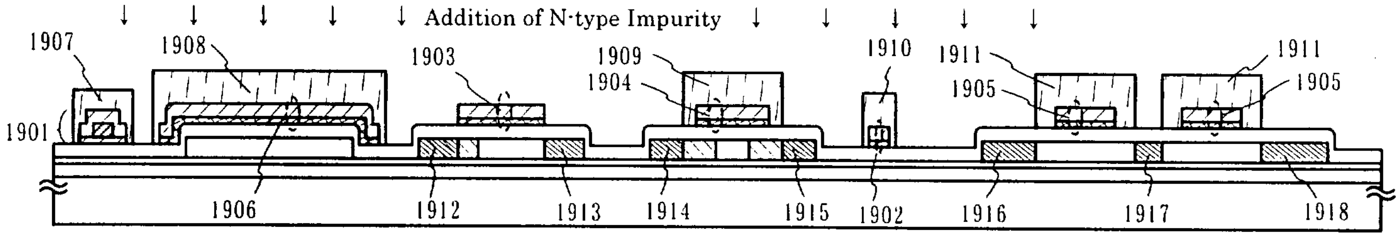


FIG. 20A

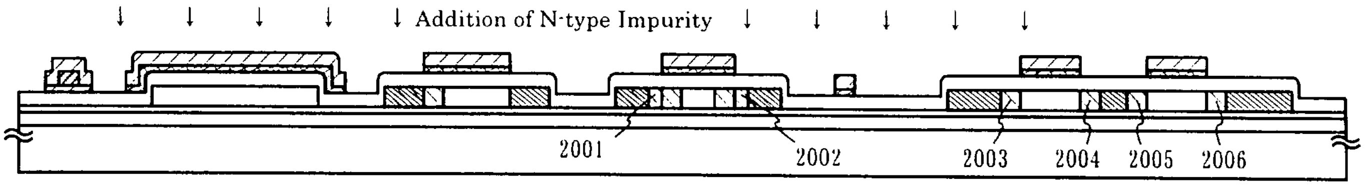


FIG. 20B

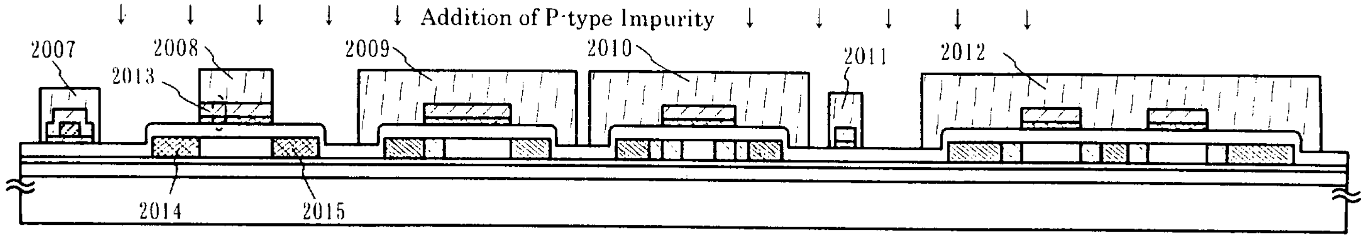


FIG. 20C

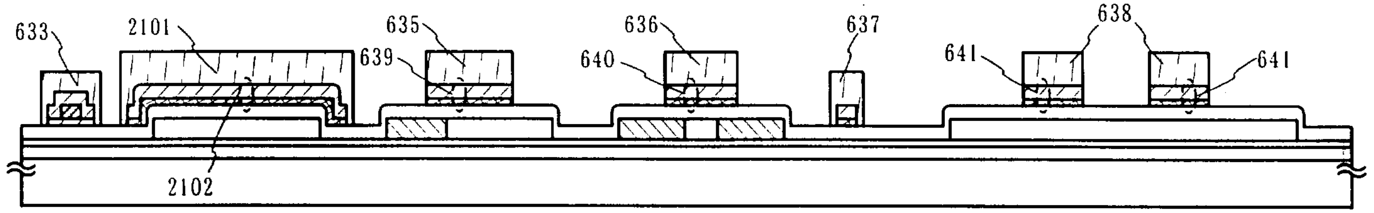


FIG. 21A

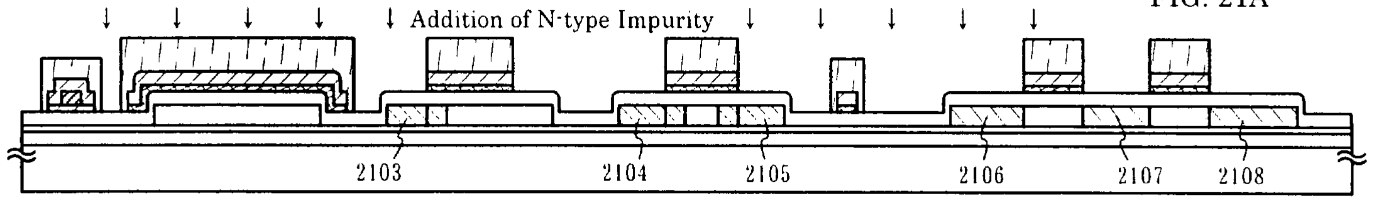


FIG. 21B

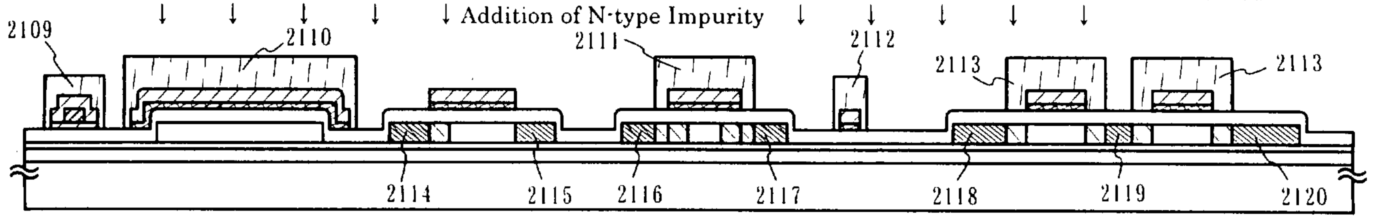


FIG. 21C

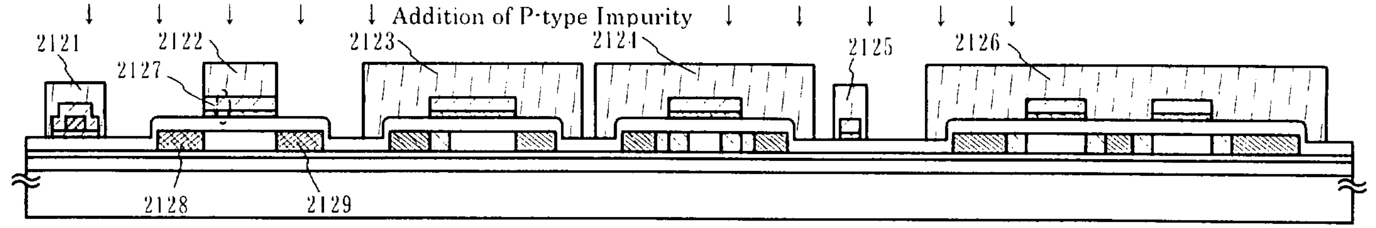


FIG. 21D

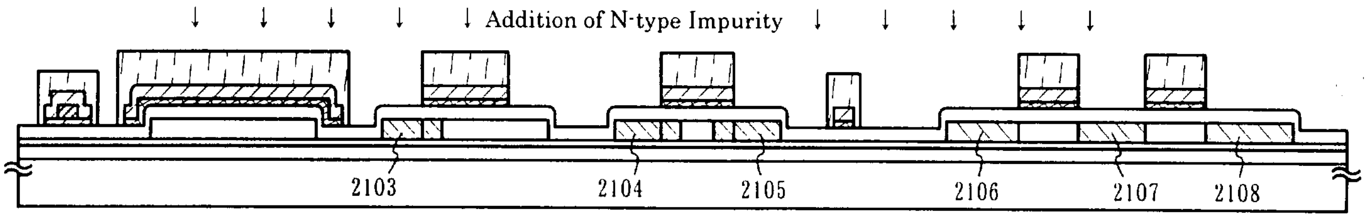


FIG. 22A

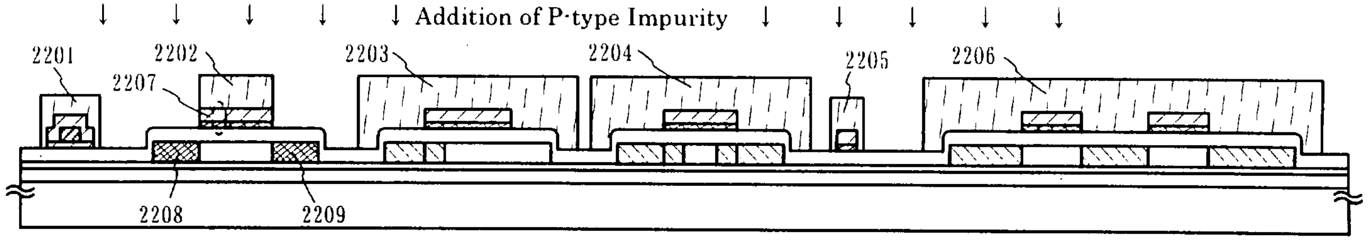


FIG. 22B

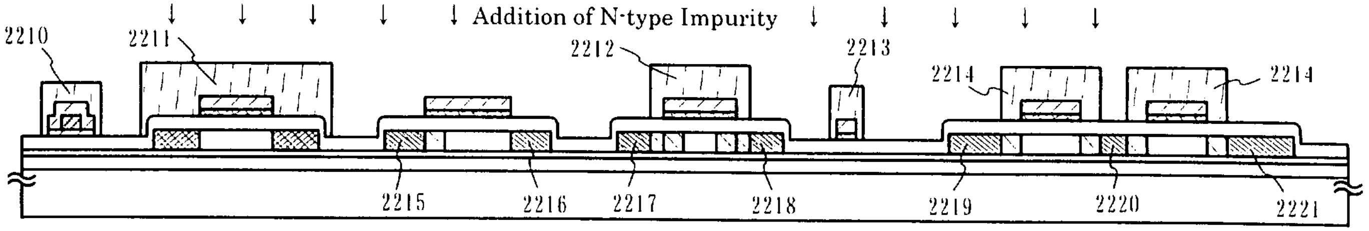


FIG. 22C

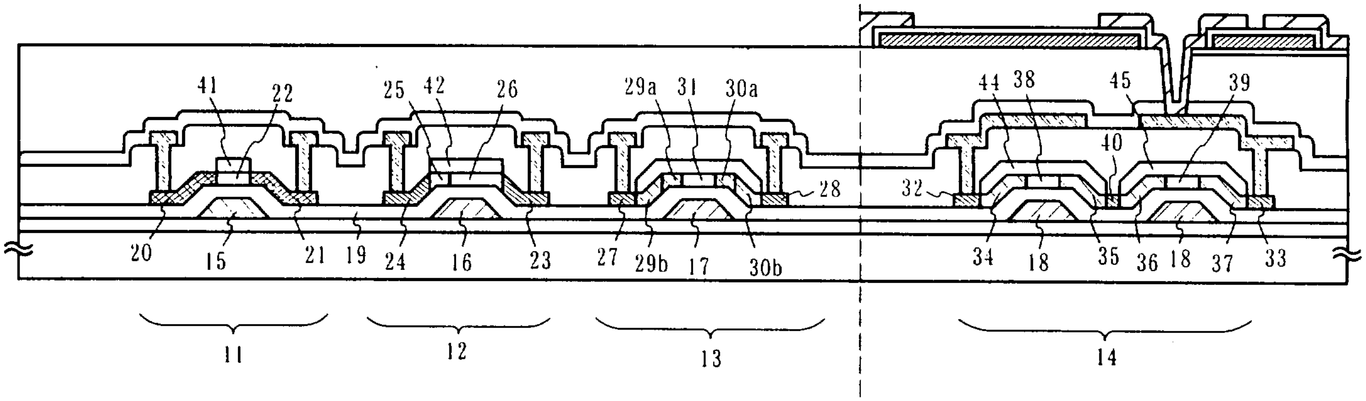

41
22
25
42
26
29a
31
30a
44
38
45
39
40
28
32
20
15
21
19
24
16
23
27
29b
17
30b
34
18
35
36
18
37
33
11
12
13
14

FIG. 23

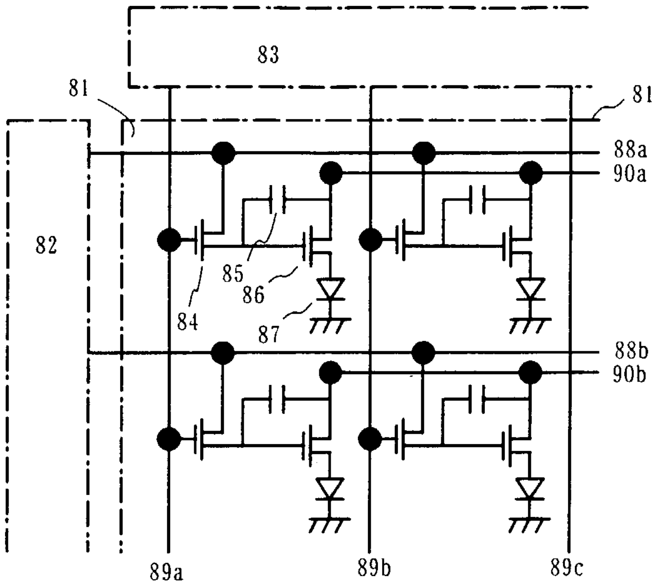


FIG. 24

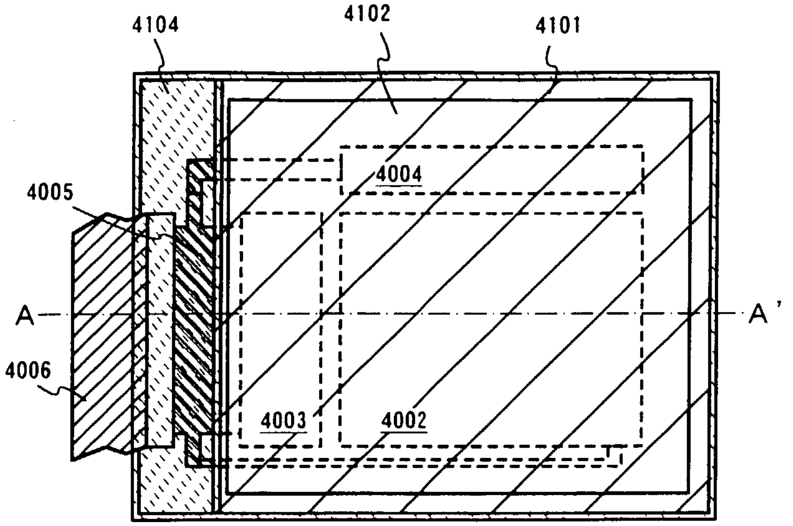


FIG.25A

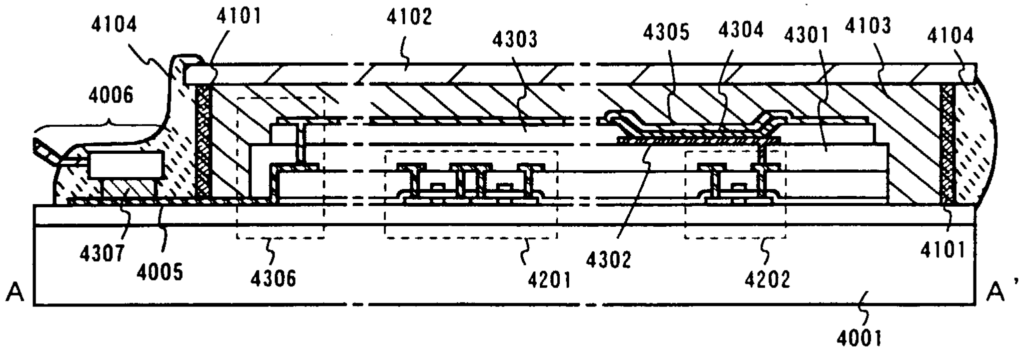


FIG.25B

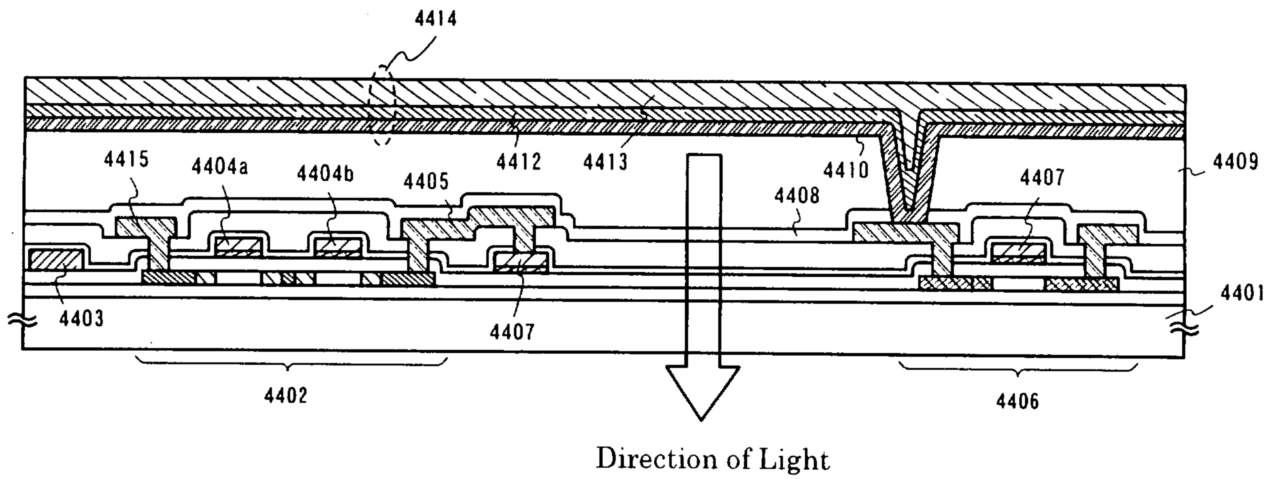

4414
4415
4404a
4404b
4405
4412
4413
4410
4408
4407
4409
4403
4407
4401
4402
4406
Direction of Light

FIG. 26

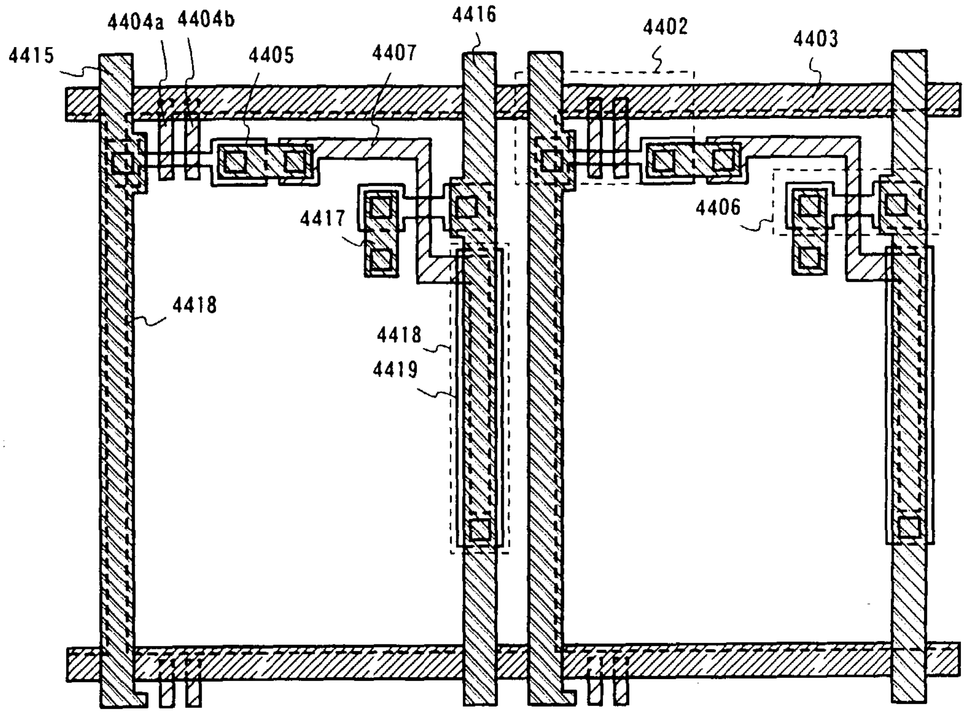


FIG. 27A

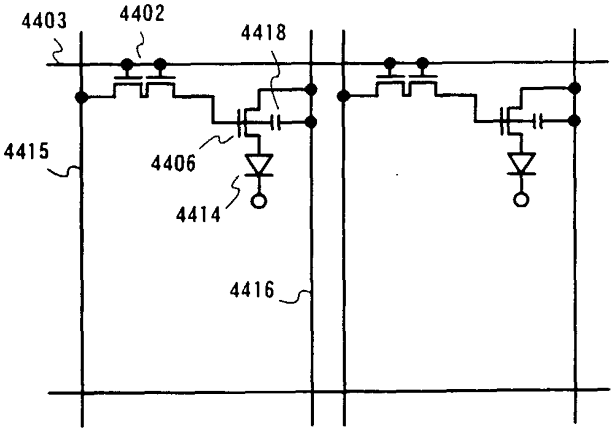


FIG. 27B

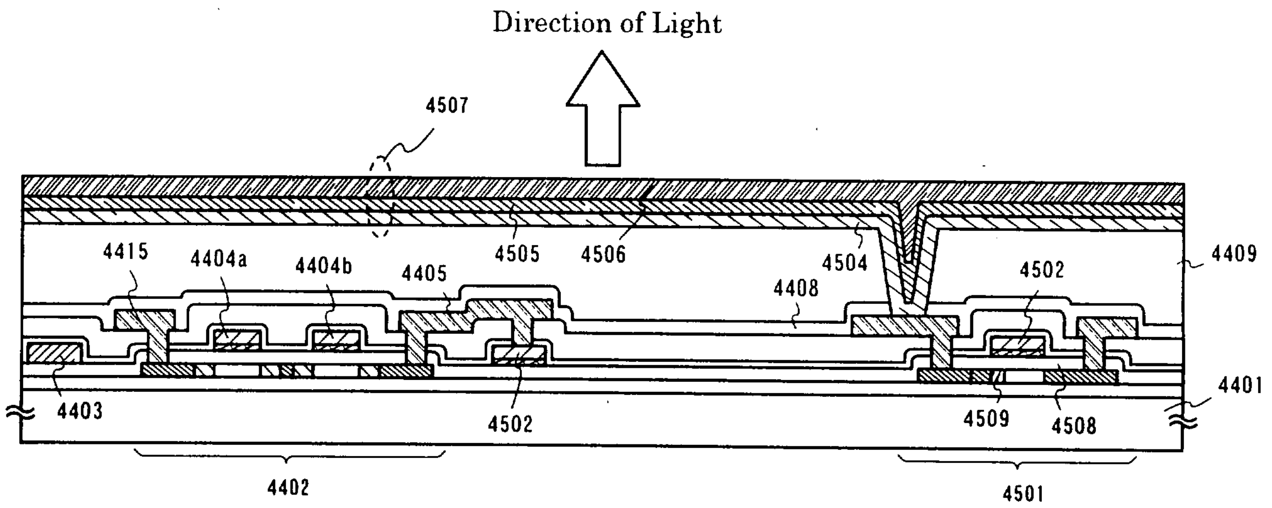

Direction of Light
4507
4415
4404a
4404b
4405
4505
4506
4504
4408
4502
4409
4401
4403
4502
4509
4508
4402
4501

FIG. 28

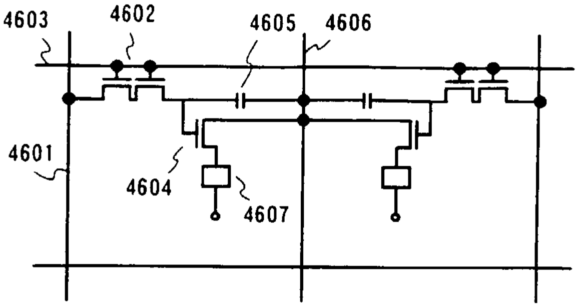


FIG. 29A

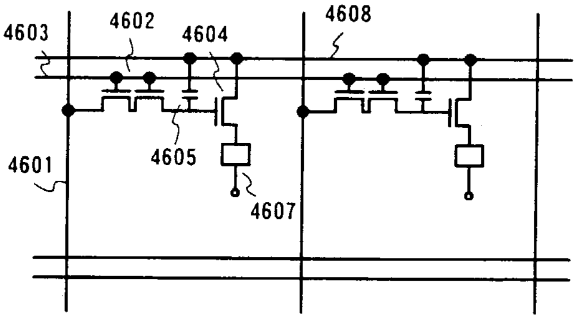


FIG. 29B

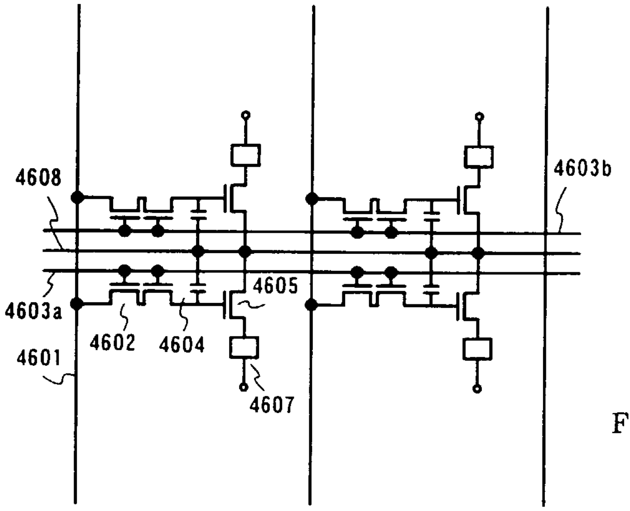


FIG. 29C

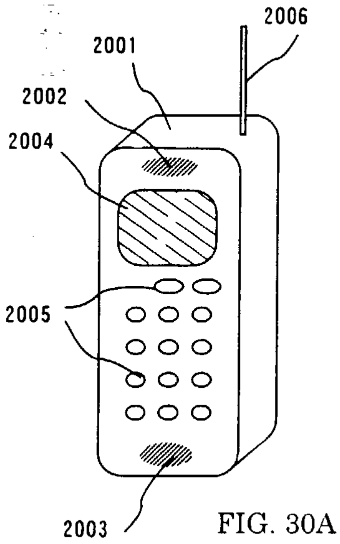


FIG. 30A

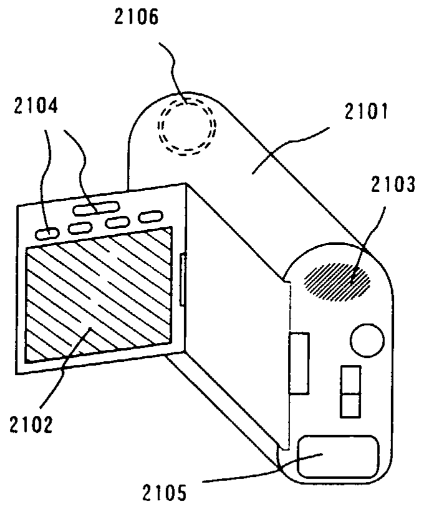


FIG. 30B

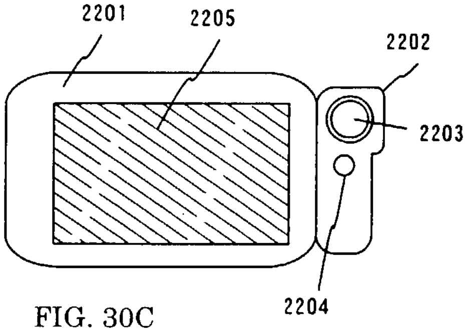


FIG. 30C

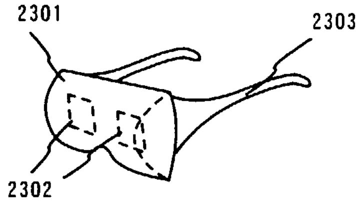


FIG. 30D

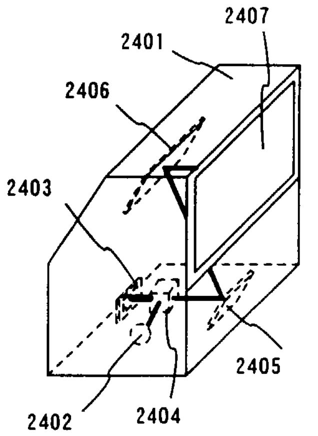


FIG. 30E

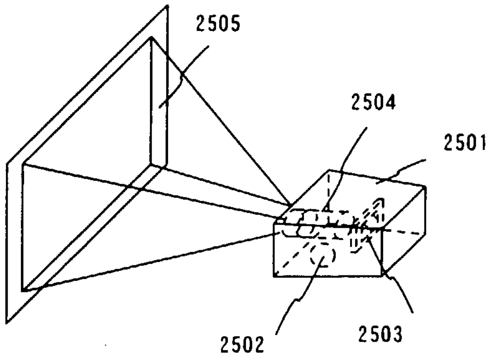


FIG. 30F

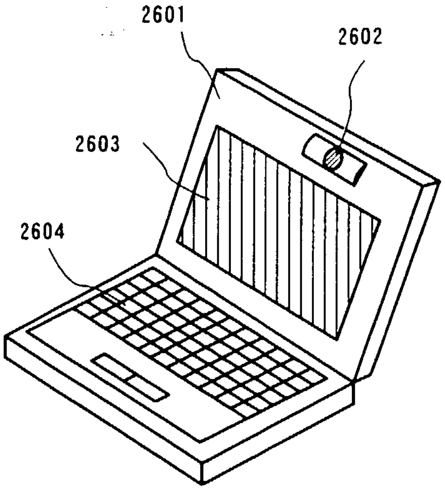


FIG. 31A

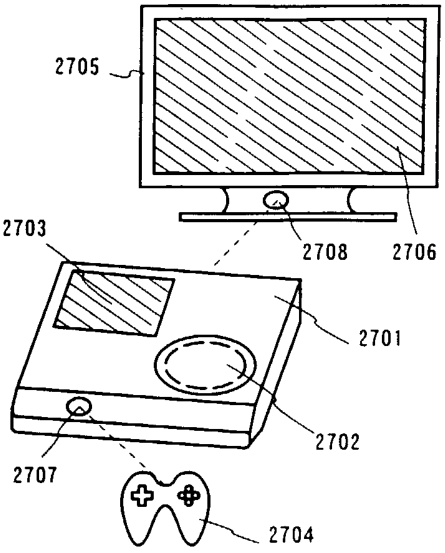


FIG. 31B

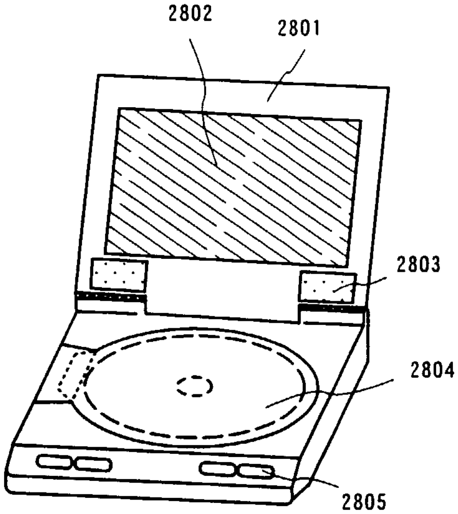


FIG. 31C

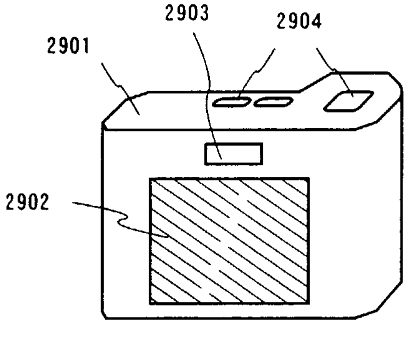


FIG. 31D

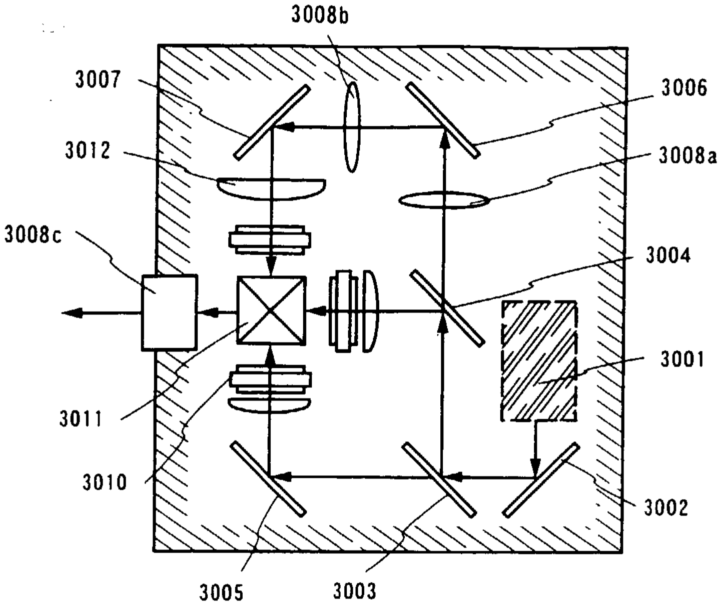


FIG. 32A

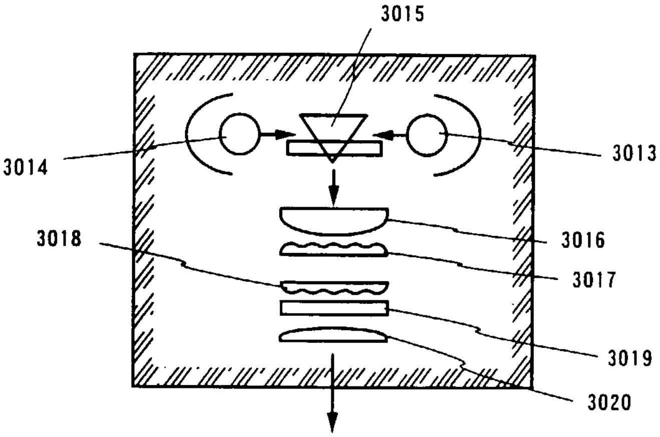


FIG. 32B

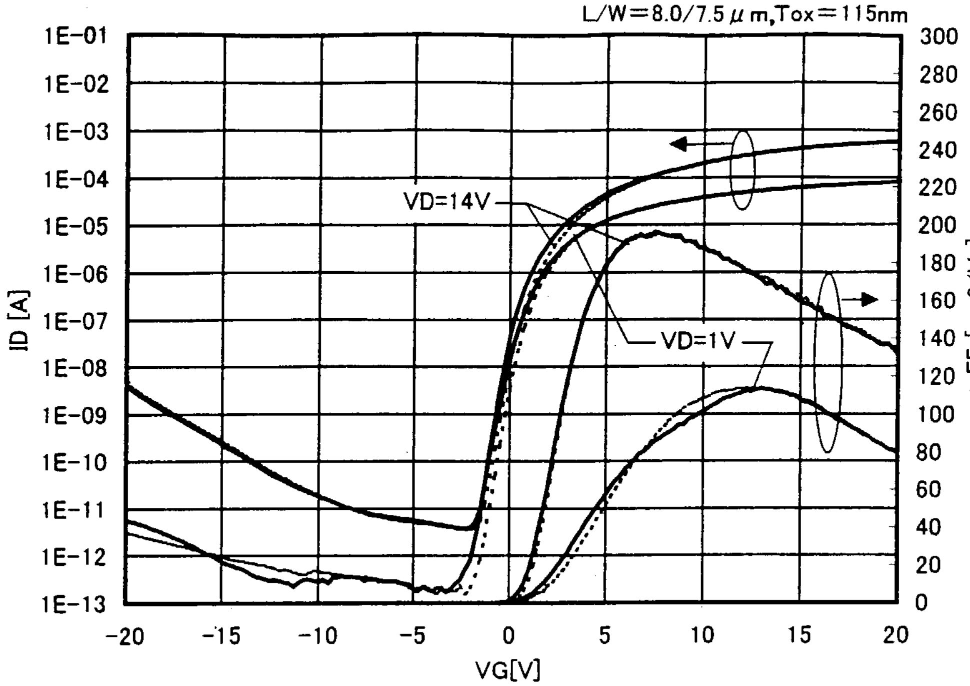
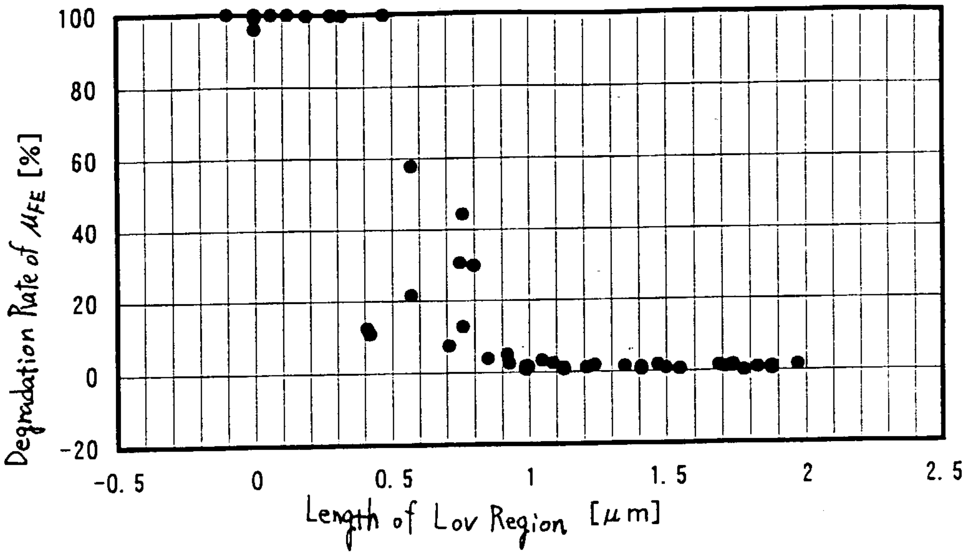

L/W=8.0/7.5 μ m,Tox=115nm
1E-01
1E-02
1E-03
1E-04
1E-05
1E-06
1E-07
1E-08
1E-09
1E-10
1E-11
1E-12
1E-13
ID [A]
300
280
260
240
220
200
180
160
140
120
100
80
60
40
20
0
μ FE [cm2/Vs]
VD=14V
VD=1V
-20
-15
-10
-5
0
5
10
15
20
VG[V]

FIG. 33



100
80
60
40
20
0
-20
-0. 5
0
0. 5
1
1. 5
2
2. 5
Degradation Rate of μ_{FE} [%]
Length of Lov Region [μm]

FIG. 34

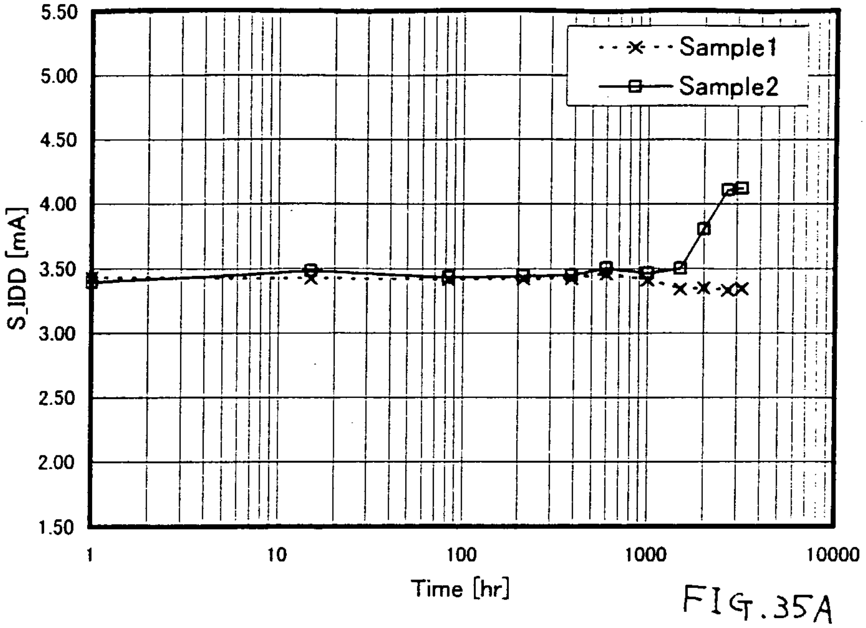


FIG.35A

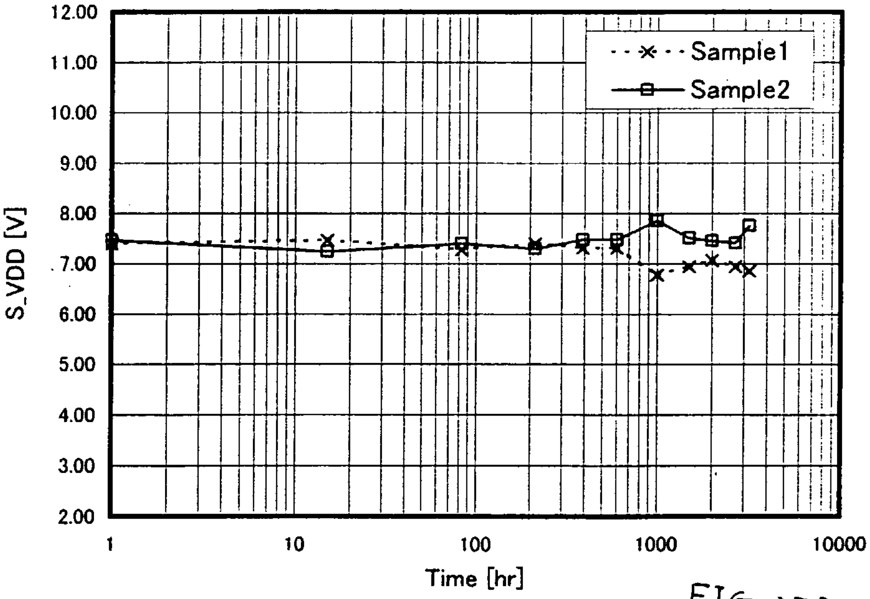


FIG.35B

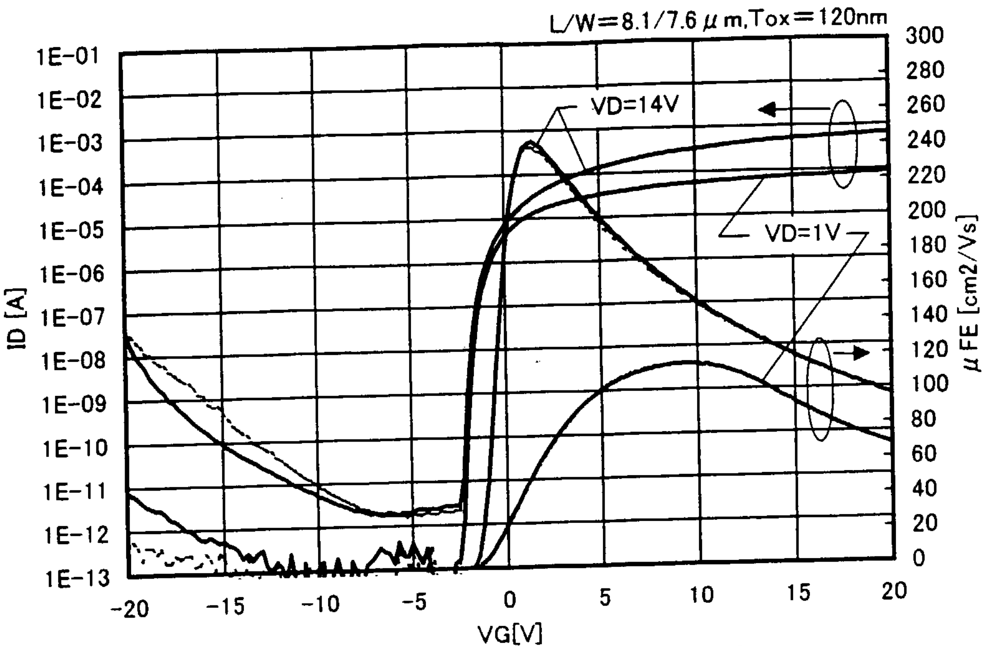

L/W=8.1/7.6 μm,Tox=120nm
1E-01
1E-02
1E-03
1E-04
1E-05
1E-06
1E-07
1E-08
1E-09
1E-10
1E-11
1E-12
1E-13
ID [A]
-20
-15
-10
-5
0
5
10
15
20
VG[V]
VD=14V
VD=1V
300
280
260
240
220
200
180
160
140
120
100
80
60
40
20
0
μFE [cm2/Vs]

FIG.36

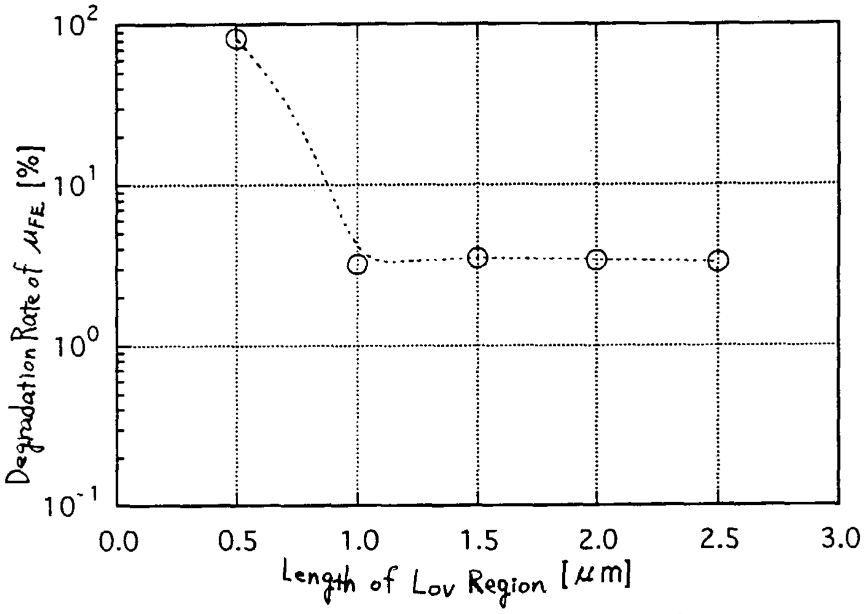

10^2
10^1
10^0
10^{-1}
0.0
0.5
1.0
1.5
2.0
2.5
3.0
Degradation Rate of μ_{FE} [%]
Length of Lov Region [μm]

FIG. 37

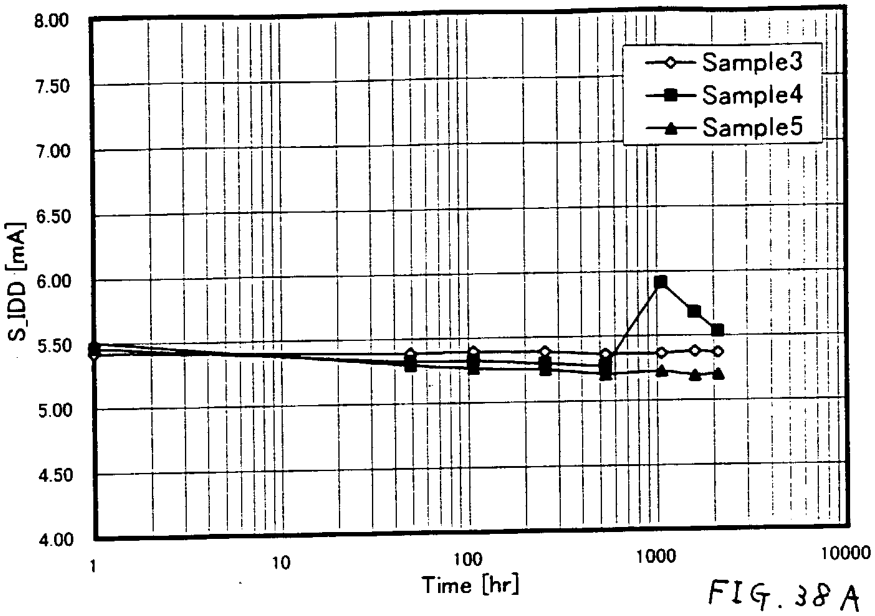


FIG. 38A

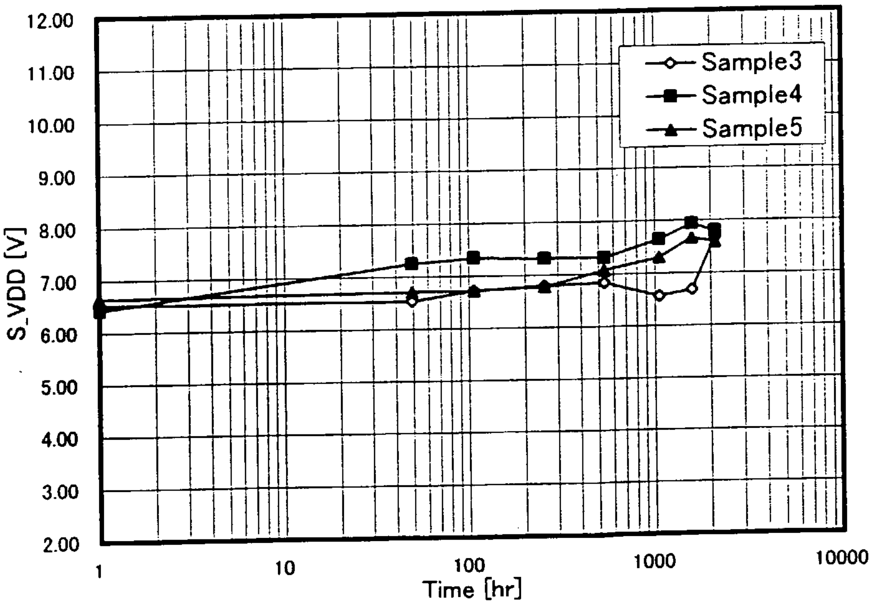


FIG. 38B

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/533,175	03/22/2000	2775	1228	0756-2125	21	34	5

22204
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FILING RECEIPT

OC000000005369579

Date Mailed: 08/31/2000

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Applicant(s)

Shunpei Yamazaki, Tokyo, JAPAN;
Jun Koyama, Kanagawa, JAPAN;

9/7/00

Continuing Data as Claimed by Applicant

Foreign Applications

If Required, Foreign Filing License Granted 06/12/2000

Title

Method for manufacturing an electrooptical device

Preliminary Class

345

Data entry by : MIDDLETON, MATTIE **Team :** OIPE **Date:** 08/31/2000

A METHOD FOR MANUFACTURING AN ELECTROOPTICAL DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a semiconductor device having a circuit comprising thin film transistors (hereinafter referred to as "TFTs") on a substrate having an insulating surface, and to a manufacturing method thereof. More specifically, the present invention relates to electro-optical devices (called also "electronic equipments") typified by a liquid crystal display device including a pixel section (pixel matrix circuit) and driving circuits disposed around the pixel section and formed on the same substrate and an EL (electro-luminescence) display device, and electrical devices (called also "electronic appliances") having the electro-optical device mounted thereto.

Note that, throughout this specification, the semiconductor device indicates general devices that can function by using semiconductor characteristics, and that electro-optical device, semiconductor circuit, and electronic equipment are all categorized as semiconductor devices.

2. Description of the Related Art

Development of a semiconductor device having a large area integrated circuit, that comprises TFTs formed on a substrate having an insulation surface, has been made progressively. An active matrix type liquid crystal display device, an EL display device and a close adhesion type image sensor are typical of such semiconductor devices. Particularly because TFTs using a polycrystalline silicon film (typically, a poly-Si film) as an active layer (the TFT will be hereinafter referred to as "poly-silicon TFT") have high electric field mobility, they can form a variety of functional circuits.

In the active matrix type liquid crystal display device, for example, an integrated circuit that includes a pixel section for displaying images for each functional block, a shift register circuit, a level shifter circuit, a buffer circuit each being based on a CMOS circuit and a sampling circuit, and so forth, is formed on one substrate. In the case of the close adhesion type image sensor, an integrated circuit such as a sample-and-hold circuit, a shift register circuit, a multiplexer circuit, and so forth, are formed by using the TFTs.

These driving circuits (which are also called "peripheral driving circuits") do not always have the same operating condition. Therefore, the characteristics required for the TFTs are naturally different to certain extents. The pixel section comprises a pixel TFT functioning as a switching device and an auxiliary storage capacitor, and a voltage is applied to a liquid crystal to drive it. Here, it is necessary to drive the liquid crystal by alternating current, and a system called "frame inversion driving" is widely applied. Therefore, one of the required characteristics of the TFT is that an OFF current value (a drain current value flowing through the TFT when it is in the OFF operation) must be sufficiently lowered. In a buffer circuit on the other hand, because a high driving voltage is applied, the TFT must have a high withstand voltage such that it does not undergo breakdown even when a high voltage is applied. In order to improve the current driving capacity, it is necessary to sufficiently secure the ON current value (the drain current value flowing through the TFT when it is in the ON operation).

However, the poly-silicon TFT involves the problem that its OFF current is likely to become high. Degradation such as the drop of the ON current value is observed in the poly-silicon TFT in the same way as in MOS transistors used for ICs, or the like. It is believed that the main cause is hot carrier injection, and the hot carriers generated by a high electric field in the proximity of the drain presumably invite this degradation.

An LDD (lightly doped drain) structure is known as a structure of the TFT for lowering the OFF current value. This structure forms an impurity region having a low concentration between a channel forming region and a source or drain region to which an impurity is doped in a high concentration. The low concentration impurity region is called the "LDD region".

A so-called "GOLD (gate-drain overlapped LDD) structure" is also known as a structure for preventing deterioration of the ON current value by hot carrier injection. Since the LDD region is so arranged as to overlap with a gate wiring through a gate insulation film in this structure, this structure is effective for preventing hot carrier injection in the proximity of the drain and for improving reliability. For example, Mutsuko Hatano, Hajime Akimoto and Takeshi Sakai, "IEDM97 Technical Digest", pp.523-526, 1997, discloses a GOLD structure using side walls formed from silicon. It has been confirmed that this structure provides by far higher reliability than the TFTs having other structures.

In an active matrix type liquid crystal display device, a TFT is disposed for each of dozens to millions of pixels and a pixel electrode is disposed for each TFT. An opposing electrode is provided on an opposing substrate side sandwiching a liquid crystal, and forms a kind of capacitors using the liquid crystal as a dielectric. The voltage to be applied to each pixel is controlled by the switching function of the TFT. As the charge to this capacitor is controlled, the liquid crystal is driven, and an image is displayed by controlling the quantity of transmitting rays of light.

However, the accumulated capacity of this capacitor decreases gradually due to a leakage current resulting from the OFF current, or the like. Consequently, the quantity of transmitting rays of light changes, thereby lowering the contrast of image display. Therefore, it has been customary to dispose a capacitance wiring, and to arrange another capacitor (called a "storage capacitor") in parallel with the capacitor using the liquid crystal as the dielectric in order to supplement the capacitance lost by the capacitor using the liquid crystal as the dielectric.

Nonetheless, the required characteristics of the pixel TFT of the pixel section are not always the same as the required characteristics of the TFT (hereinafter called the "driving TFT") of a logic circuit (called also the "driving circuit") such as the shift register circuit and the buffer circuit. For example, a large reverse bias voltage (a negative voltage in n-channel TFT) is applied to the gate wiring in the pixel TFT, but the TFT of the driving circuit is not fundamentally driven by the application of the reverse bias voltage. The operation speed of the former may be lower than 1/100 of the latter.

The GOLD structure has a high effect for preventing the degradation of the ON current value, it is true, but is not free from the problem that the OFF current value becomes greater than the ordinary LDD structures. Therefore, the GOLD structure cannot be said as an entirely preferable structure for the pixel TFT, in particular. On the contrary, the ordinary LDD structures have a high effect for restricting the OFF current value, but is not resistant to hot carrier injection, as is well known in the art.

For these reasons, it is not always preferred to constitute all the TFTs by the same structure in the semiconductor devices having a plurality of integrated circuits such as the active matrix type liquid crystal display device.

When a sufficient capacitance is secured by forming a storage capacitor using the capacitance wiring in the pixel section as represented by the prior art example described above, an aperture ratio (a ratio of an area capable of image display to an area of one pixel) must be sacrificed. Particularly in the case of a small high precision panel used for a projector type display device, the area per pixel is so small that the drop of the aperture ratio by the capacitance wiring becomes a serious problem.

SUMMARY OF THE INVENTION

In order to solve the problems described above, the present invention aims at improving operation performance and reliability of a semiconductor device by optimizing the structures of the TFT used for each circuit of the semiconductor device in accordance with the function of each circuit.

It is another object of the present invention to provide a structure for lowering the area of a holding capacitance provided to each pixel and for improving an aperture ratio in a semiconductor device having a pixel section.

In order to solve the problems above, the structure of the present invention is characterized by an electrooptical device comprising a pixel section and a driver circuit over a substrate is characterized in that:

a portion or all of an LDD region of n-channel TFT in the driver circuit overlaps with a gate electrode of the n-channel TFT by interposing a gate insulating film;

an LDD region of a pixel TFT in the pixel section is not overlapped with a gate electrode of the pixel TFT through a gate insulating film; and

a wiring of a laminate comprising a first electrode formed by a same layer and comprises a same material of the gate electrode of the pixel TFT and a second wiring having a lower resistivity than the first electrode is formed.

In addition to the above structure, a storage capacitor of the pixel section may be formed by a shielding film disposed over an organic resin film, an oxide of the shielding film and a pixel electrode. Because a storage capacitor can be formed in a very small area, an aperture ratio of the pixel can be increased.

Further, another structure of the present invention is characterized in that:

the driver circuit comprises a first n-channel TFT in which all of an LDD region overlaps with a gate electrode by interposing a gate insulating film; and a second n-channel TFT in which a portion of an LDD region overlaps with a gate electrode by interposing a gate insulating film;

an LDD region of the pixel TFT that forms the pixel section does not overlap with a gate electrode of the pixel TFT through a gate insulating film; and

a wiring of a laminate comprising a first electrode formed by a same layer and comprises a same material of the gate electrode of the pixel TFT and a second wiring having a lower resistivity than the first electrode is formed.

Needless to say, a storage capacitor of the pixel section may be formed by a shielding film disposed over an organic resin film, an oxide of the shielding film and a pixel electrode.

In the above structure, an n-type impurity element in an LDD region of n-channel TFT of the driver circuit may be preferably included at a concentration of 2 times to 10 times higher than that of an LDD region of the pixel TFT. In addition, an LDD region may be formed on one side of a channel forming region (preferably a drain region side) in the first n-channel TFT, and LDD regions may be formed on both sides of the channel forming region (both sides interposing a channel forming region) in the second n-channel TFT.

Further in the above structure, it is preferable to set the resistivity of the second wiring at 1/10 to 1/100 of the resistivity of the first wiring. In concrete, the resistivity of the first wiring may be set at 10 to 500 $\mu\Omega$ cm , and the resistivity of the second wiring may be set at 0.1 to 10 $\mu\Omega$ cm .

In order to satisfy these conditions, a wiring comprising tantalum, titanium, molybdenum, tungsten, chromium, niobium or silicon may be used as the first wiring, and a wiring comprising aluminum, copper or silver may be used as the second wiring.

Note that through the specification a wiring comprising tantalum, titanium, molybdenum, tungsten, chromium, niobium or silicon denotes a wiring selected from: tantalum wiring, titanium wiring, molybdenum wiring, tungsten wiring, chromium wiring, niobium wiring, silicon wiring, tantalum nitride wiring, titanium nitride wiring, molybdenum nitride wiring, tungsten nitride wiring, niobium nitride wiring and a wiring comprising alloy of 2 or more of the elements selected from tantalum, titanium, molybdenum, tungsten, chromium, niobium and silicon. In addition, a wiring in which these wirings are laminated, is also included.

Also through the specification, a wiring comprising aluminum, copper or silver denotes a wiring selected from: aluminum wiring, copper wiring, silver wiring, and a wiring comprising an alloy including 2 or more of the elements selected from aluminum, copper and silver. In addition, a wiring in which these wirings are laminated, is also included.

As in the structure above, the present invention is largely characterized in that a second wiring having lower resistivity than a first wiring is laminated on the first wiring comprising the same material and formed from the same layer as a gate electrode of the pixel TFT. It is possible to use such wiring for various ways, but it is preferable to use for wiring that requires to flow large electric current.

Specifically it is effective to use for a wiring to send electric signal to the driver circuit (hereinafter referred to as input-output signal wiring) and a gate wiring. As an input-output signal wiring, there are wirings to transmit clock signal, start pulse signal or a video signal.

In other words, an input-output signal wiring and a gate wiring (including gate electrode) are formed from a first wiring comprising the same material and formed from the same layer (namely formed at the same time) as a gate electrode of the pixel TFT (same is true of a gate electrode of the n-channel TFT). After finishing activation of the source regions and the drain regions, a second wiring that has a lower resistivity than the first wiring is laminated on the first wiring to form a wiring of low resistivity.

At this time it is preferred that the portions where the second wiring is laminated do not require a minute processing and have least resistivity as possible. Namely, portions that require minute processing such as a gate electrode and an internal wiring of the driver circuit may be formed from the first wiring, and portions where minute processing is not required may be formed by a wiring of a laminate of the first wiring and the second wiring.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

Figs. 1A to 1F are figures showing manufacturing processes of the pixel section and the driver circuit.

Figs. 2A to 2E are figures showing manufacturing processes of the pixel section and the driver circuit.

Figs 3A to 3D are figures showing manufacturing processes of the pixel section and the driver circuit.

Figs. 4A and 4B are figures showing manufacturing processes of the pixel section and the driver circuit.

Fig. 5 is a cross sectional structure of an active matrix liquid crystal display device.

Fig. 6 is a figure showing an LDD structure of n-channel TFT.

Fig. 7 is a perspective view of an active matrix liquid crystal display device.

Fig. 8 is a circuit block diagram of an active matrix liquid crystal display device.

Figs. 9A to 9D are figures showing structure from top view of pixel section.

Figs. 10A and 10B are a top view and a cross sectional view of pixel section respectively.

Fig. 11 is a cross sectional structure of an active matrix liquid crystal display device.

Figs. 12A to 12C are figures showing manufacturing process of a pixel section and a driver circuit.

Fig. 13 is a figure showing a structure of an active matrix EL display device.

Figs. 14A and 14B are a top view and a cross section, respectively, of an EL display device.

Fig. 15 is a figure showing a cross section of an EL display device.

Figs. 16A and 16B are figures of a top view and a circuit diagram of an EL display device.

Fig. 17 is a figure showing a cross section of an EL display device.

Figs. 18A to 18C are figures showing circuit structure of pixel section of an EL display device.

Figs. 19A to 19F are examples of electronic devices.

Figs. 20A to 20D are examples of electronic devices.

Figs. 21A and 21B are figures showing structures of an optical engine and a light source optical system, respectively.

Fig. 22 is a graph showing ID-VG curve and a field effect mobility of n-channel TFT.

Chart 1 shows a comparative data of sheet resistance in metal materials.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[Embodiment Mode]

The embodiment mode of the present invention is described in details by embodiments shown below.

[Embodiment 1]

An embodiment according to the present invention is described by using Figs. 1A to 4B. Here a method for fabricating TFTs of a pixel section and a driver circuit provided in its peripheral, at the same time, is described. Provided, for the simplicity of explanation, a

CMOS circuit which is a basic circuit for a shift register and buffer etc., and an n-channel TFT forming a sampling circuit are shown for the driver circuit.

In Fig. 1A, it is preferable to use a glass substrate or a quartz substrate for substrate 100. A silicon substrate, a metal substrate or a stainless substrate having an insulating film formed on the surface thereof can be used, too. If heat resistivity permits, plastic substrate may also be used.

A base film 101 that comprises a silicon-containing insulating film (the term “insulating film” generically represents a silicon oxide film, a silicon nitride film and a silicon nitride oxide film in this specification) is formed by plasma CVD or sputtering to a thickness of 100 to 400nm on the surface of the substrate 100 on which the TFTs are to be fabricated.

The term “silicon nitride oxide film” used in this specification represents an insulating film expressed by the general formula SiO_xN_y and containing silicon, oxygen and nitrogen in a predetermined proportion. In embodiment 1, a laminate film may be used as the base film 101, that comprises a silicon nitride oxide film with a thickness of 100 nm containing nitrogen at 20 to 50 atomic % (typically 20 to 30 atomic %), and a silicon nitride oxide film with a thickness of 200 nm containing nitrogen at 1 to 20 atomic % (typically 5 to 10 atomic %). The thickness is not necessarily limited to these values. The ratio of nitrogen and oxygen contained in a silicon nitride oxide film (ratio by atomic %) may be set 3:1 to 1:3 (typically 1:1). A silicon nitride oxide film may be fabricated from raw material gas of SiH_4, N_2O and NH_3.

The base film 101 is formed in order to prevent impurity contamination from the substrate, and does not necessarily be formed for the case of a quartz substrate being used.

A semiconductor film containing amorphous structure (amorphous silicon film in the present embodiment (not shown)) is formed on the base film 101 at a thickness of 30 to 120nm (preferably 50 to 70nm) by a known film formation method. As a semiconductor film containing amorphous structure, there are amorphous semiconductor film and microcrystalline semiconductor film and further, a compound semiconductor film containing amorphous structure such as amorphous silicon germanium film etc. may also be included.

A semiconductor film containing crystalline structure (crystalline silicon film in the embodiment 1) 102 is formed according to a technique disclosed in the Japanese Patent Application Laid-Open No. Hei 7-130652 (corresponding to U.S. Patent No. 5,643,826). The technique described in the gazette is a crystallization means that uses a catalytic element for promoting crystallization (one or plural of element selected from nickel, cobalt, germanium, tin, lead, palladium, iron and copper; typically nickel) in crystallizing the amorphous silicon film.

More concretely, heat-treatment is conducted under the condition where the catalytic element(s) is held on the surface of the amorphous silicon film to convert the amorphous silicon film to the crystalline silicon film. Although Embodiment 1 uses a technique described in the Embodiment 1 of the gazette, a technique described in Embodiment 2 may also be used. Though single crystal silicon film and polycrystalline silicon film are both included in crystalline silicon film, the crystalline silicon film formed in the present embodiment is a silicon film having crystal grain boundaries. (Fig. 1A)

Though it depends on hydrogen content in the amorphous silicon film, it is preferable to carry out dehydrogenation process by heating at 400 to 550°C for some hours to reduce the contained hydrogen amount at 5 atomic % or lower and conduct crystallization process. The amorphous silicon film may be fabricated by other fabricating methods such as sputtering or vapor deposition, but it is preferable to sufficiently reduce impurity elements such as oxygen or nitrogen contained in the film.

Because base film and amorphous silicon film can be fabricated by the same deposition method, they may be successively formed. Scattering of characteristics of the fabricated TFTs may be reduced by making it possible to prevent contamination of the surface by not exposing to the atmosphere after formation of the base film.

Next, a light generated from a laser light source (laser light) is irradiated onto the crystalline silicon film 102 (hereinafter referred to as laser anneal) and a crystalline silicon film 103 in which crystallinity is improved is formed. Though a pulse oscillation type or a continuous oscillation type excimer laser light is preferable for the laser light, a continuous oscillation type argon laser light may also be used as the laser light. The beam shape of the laser light may be linear, or it may be a rectangular shape. (Fig. 1B)

A light generated from a lamp (lamp radiation) may be irradiated (hereinafter referred to as lamp annealing) may be used in place of laser light. As a lamp radiation, lamp radiation generated from halogen lamp or infrared lamp may be used.

The process of conducting heat treatment (annealing) by laser light or lamp radiation is called a light annealing process. Because light annealing process can perform a high temperature heat treatment in a short time, effective heat treatment process may be carried out at high throughput even in the case of using a substrate with low heat resistance such as glass substrate etc. Needless to say, since the object is annealing, it can be substituted by a furnace annealing (it may also be called heat annealing) using electric furnace.

In the embodiment 1, laser annealing process was carried out by forming pulse oscillation type excimer laser light into a linear shape. The laser annealing conditions are: XeCl gas is used as excitation gas, treatment temperature is set at room temperature, pulse oscillation frequency is set at 30Hz, and laser energy density at 250 to 500mJ/cm^2 (typically 350 to 400mJ/cm^2).

Laser annealing process carried out at the above stated conditions has an effect of completely crystallizing the amorphous region remained after heat crystallization as well as reducing defects in the crystalline region already crystallized. Accordingly, the present process may be called a process for improving crystallinity of the semiconductor film, or a process for promoting crystallization of the semiconductor film. Such effects can be obtained by optimizing lamp annealing condition. This condition is referred to as the first light annealing in the present specification.

Next, a protecting film 104 is formed on crystalline silicon film 103 for the later impurity doping process. Silicon nitride oxide film or silicon oxide film at a thickness of

100 to 200nm (preferably 130 to 170nm) is used for the protecting film 104. This protecting film 104 has a meaning of not to expose the crystalline silicon film directly to plasma at impurity doping, and to make minute concentration control possible.

Then, a resist mask 105 is formed thereon, and impurity element imparting p-type (hereinafter referred to as p-type impurity element) is doped through protecting film 104. As a p-type impurity element, typically an element belonging to group 13 or more specifically boron or gallium may be used. This process (referred to as channel doping process) is a process for controlling threshold voltage of a TFT. Here, boron is doped by ion doping in which diborane (B_2H_6) is excited by plasma without mass separation. Needless to say, it is acceptable to use ion implantation in which mass separation is performed.

By this process, impurity region 106 including p-type impurity (boron in the present embodiment) at a concentration of 1×10^{15} to 1×10^{18}atoms/cm^3 (typically 5×10^{16} to 5×10^{17}atoms/cm^3) is formed. Note that through the specification, an impurity region containing p-type impurity region in the above stated concentration range is defined as a p-type impurity region (b) (provided, regions where impurity elements imparting n-type are intentionally doped are excluded). (Fig. 1C)

Next, resist mask 105 is removed and resist masks 107 to 110 are newly formed. Then impurity regions imparting n-type 111 to 113 are formed by doping impurity elements imparting n-type (hereinafter referred to as n-type impurity element). As an n-type impurity element, typically an element belonging to group 15 or more specifically phosphorus or arsenic may be used. (Fig. 1D)

These low concentration impurity regions 111 to 113 are impurity regions functions as LDD regions of the n-channel TFT of the later formed CMOS circuit and sampling circuit. In thus formed impurity regions, n-type impurity element is contained at a concentration of 2×10^{16} to 5×10^{19}atoms/cm^3 (typically 5×10^{17} to 5×10^{18}atoms/cm^3). In the present specification, an impurity region containing n-type impurity region in the above stated concentration range is defined as an n-type impurity region (b).

Here, phosphorus is doped by ion doping in which phosphine (PH_3) is excited by plasma without mass separation. Needless to say, ion implantation in which mass separation is performed may be used as well. In this process, phosphorus is doped into the crystalline silicon film through protecting film 107.

Next, protecting film 104 is removed, and irradiation process of laser light was conducted again. Here again excimer laser light of pulse oscillation type or continuous oscillation type is preferable, but argon laser light of continuous oscillation type may also be used. The beam shape of the laser light may be either of linear or rectangular shape. Provided, because activation of the doped impurity element is the object, it is preferable to irradiate with an energy at a level of not melting the crystalline silicon film. It is also possible to conduct laser annealing process with the protecting film 104 left thereon. (Fig. 1E)

In embodiment 1, laser annealing process was carried out by forming pulse oscillation type excimer laser light into a linear shape. The laser annealing conditions are: XeCl gas is used as excitation gas, treatment temperature is set at room temperature, pulse oscillation frequency is set at 30Hz, and laser energy density at 100 to 300mJ/cm^2 (typically 150 to 250mJ/cm^2).

The light annealing process carried out on the above stated conditions has an effect of recrystallizing the semiconductor film that was made into amorphous in impurity element doping as well as activating the impurity element imparting n-type or p-type that was doped. It is preferable that the above stated conditions make atomic arrangement coordinated without melting the semiconductor film and at the same time activate the impurity elements. The present process may be referred as a process of activating the impurity element imparting n-type or p-type by light annealing, a process for recrystallizing the semiconductor film or a process of simultaneously carrying out both of them. Such effect can be obtained by optimizing the lamp annealing condition as well. In the present specification, this condition is referred to as the second light annealing.

By this process, the boundary of n-type impurity regions (b) 111 to 113, that is, the junction area with the intrinsic regions (p-type impurity region (b) is also regarded as substantially intrinsic) that exist around n-type impurity region (b) become clear. This means that LDD region and channel formation region may form a very good junction when later finishing TFT.

On activation of the impurity elements by this laser light, activation by heat treatment may also be used at the same time. In case of conducting activation by heat treatment, heat treatment of approximately 450 to 550°C may be conducted considering the heat resistance of the substrate.

Next, unnecessary portions of the crystalline silicon film are removed to form island semiconductor layers (hereinafter referred to as active layers) 114 to 117. (Fig. 1F)

Next, gate insulating film 118 is formed to cover the active layers 114 to 117. Gate insulating film 118 may be formed into a thickness of 10 to 200nm, preferably into 50 to 150nm. In the present embodiment, a silicon nitride oxide film is formed into a thickness of 115nm by plasma CVD with raw materials of N_2O and SiH_4. (Fig. 2A)

Then, a conductive film, that will form a gate wiring (including gate electrode) and an input-output signal wiring, is formed. Note that the conductive film may be formed by a single layer, and it is preferable to form laminated films of double layers, or triple layers as occasion demands. In the present embodiment, laminated films comprising a first conductive film 119 and a second conductive film 120. (Fig. 2B)

As the first conductive film 119 and the second conductive film 120, a metal film comprising an element selected from tantalum (Ta), titanium (Ti), molybdenum (Mo), tungsten (W), chromium (Cr), niobium (Nb), and silicon (Si), a metal compound film composed of these element as its main component (typically tantalum nitride film, tungsten nitride film, titanium nitride film), an alloy film combining these elements (typically Mo-W alloy, Mo-Ta alloy, tungsten silicide film) or a laminate film of these thin films may be used.

The first conductive film 119 may be formed into 10 to 50nm (preferably 20 to 30nm) and the second conductive film 120 may be formed into 200 to 400nm (preferably 250 to 350nm). In embodiment 1, tantalum nitride (TaN) film of 50nm thick was used as the first conductive film 119 and tantalum (Ta) film of 350nm thick was used as the second conductive film 120.

Other than this, a laminate of tungsten nitride film and tungsten film, single layer of tantalum nitride film and a tungsten silicide film are also appropriate. In addition, when a silicon film at a thickness of approximately 2 to 20nm is formed under the first conductive film 119, close adhesion of conductive film formed on the silicon film is improved and oxidation of the conductive film can be prevented.

Further, it is effective to nitrificate by exposing the surface into plasma atmosphere using ammonia gas or nitrogen gas, in case of using a metal film for the second conductive film 120 like in embodiment 1. It is possible to prevent the oxidation of the surface of the metal film.

Gate wirings 121 to 124, a first wiring 11 that will later form an input-output signal wiring and a first wiring 12 that will later form a gate wiring are formed into 400nm thickness by etching the first conductive film 119 and the second conductive film 120 at a time. Gate electrodes 122 and 123 of n-channel TFT of driver circuit are formed to overlap a portion of n-type impurity region (b) 111 to 113 by interposing a gate insulating film. These overlapped portions will later become Lov regions. Note that the gate electrode 124 seems to be two electrodes in the cross sectional view, but in effect they are formed of one continuing pattern. (Fig. 2C)

Note that through the specification a wiring formed of a same layer as gate electrode and comprised of the same material is generically referred to as a first wiring. Further, an input-output signal wiring in this specification means generically an input signal wiring or an output signal wiring that transmits from an external input-output terminal (hereinafter referred to as terminal) such as an FPC (flexible print circuit), various signals such as a drive signal (start pulse signal, clock signal etc.) and an image signal into driver circuit of an electrooptical device.

In addition, in some cases terms "gate electrode" and "gate wiring" are used distinctively for the ease of explanation. In these cases a section where a gate wiring overlaps with an active layer is referred to as a gate electrode. Accordingly, no problem arises even when a gate electrode is referred to as a gate wiring.

Then, n-type impurity element (phosphorus in embodiment 1) is doped in a self-aligned manner using gate electrodes 121 to 124 and the first wirings 11 and 12 as masks. The concentration of phosphorus doped into thus formed impurity regions 125 to 130 are set at a 1/2 to 1/10 (specifically 1/3 to 1/4) of the n-type impurity region (b) (provided it is higher by 5 to 10 times than boron concentration added in the channel doping process, specifically 1×10^{16} to 5×10^{18} atoms/cm^3, typically 3×10^{17} to 3×10^{18} atoms/cm^3). In the present Specification, an impurity region containing n-type impurity element at the above stated concentration range is defined as n-type impurity region (c). (Fig. 2D)

Note that phosphorus is doped into all of the n-type impurity regions (b) at a concentration of 1×10^{16} to 5×10^{18} atoms/cm^3 except regions hidden by the gate wirings in this process however since it is at a very low concentration, there is no effect to the function as n-type impurity region (b). Further, although boron is already doped into n-type impurity regions (b) 127 to 130 at a concentration of 1×10^{15} to 5×10^{18} atoms/cm^3 in the channel doping process, because phosphorus is doped at a concentration of 5 to 10 times that of boron contained in the p-type impurity region (b), there is no effect to the function of n-type impurity region (b) also in this case.

Strictly speaking however, while concentration of phosphorus in portions of n-type impurity region (b) 111 to 113 that overlapped with gate wirings remains at 2×10^{16} to 5×10^{19} atoms/cm^3, portions that do not overlap with gate wirings are further added with phosphorus of 1×10^{16} to 5×10^{18} atoms/cm^3, and contain phosphorus at a slightly higher concentration.

Next, a gate insulating film 118 is etched in a self-aligned manner with gate electrodes 121 to 124 and first wiring 11 and 12 as masks. Dry etching is used for the etching process and CHF$_3$ gas is used as an etching gas. Note that the etching gas need not be limited to this material. Thus, gate insulating films 131 to 134 under the gate wirings are formed. (Fig. 2E)

By exposing the active layers in this manner, acceleration voltage in performing doping process of impurity elements can be kept low. Accordingly throughput is improved since the necessary dose amount is small. Needless to say, the impurity regions may also be formed by through doping without etching the gate insulating film.

Resist masks 135 to 138 are next formed to cover the gate wirings and impurity regions 139 to 147 containing phosphorus at a high concentration were formed by adding n-type impurity element (phosphorus in embodiment 1).. Again ion doping was conducted by utilizing phosphine (PH_3) and the phosphorus concentration in these regions are set at 1×10^{20} to 1×10^{21} atoms/cm^3 (specifically 2×10^{20} to 5×10^{21} atoms/cm^3). (Fig. 3A)

Note that in this Specification an impurity region containing n-type impurity element in the above stated concentration range is defined as n-type impurity region (a). Further, although phosphorus or boron, added in the preceding processes, are already contained in the impurity regions 139 to 147, influence of phosphorus or boron added in the preceding processes need not be considered since phosphorus is later added at a sufficiently high concentration. Therefore, it is acceptable to refer the impurity regions 139 to 147 to as n-type impurity region (a) in this Specification.

Resist masks 135 to 139 are then removed, and new resist mask 148 is formed. Then, p-type impurity element (boron in the present embodiment) is doped, and impurity regions 149 and 150 that include boron at a high concentration are formed. Here, boron is doped at a concentration of 3×10^{20} to 3×10^{21}atoms/cm^3 (typically 5×10^{20} to 1×10^{21}atoms/cm^3) by ion doping using diborane (B_2H_6). In the present specification, an impurity region that includes p-type impurity region in the above stated concentration range is defined as p-type impurity region (a). (Fig. 3B)

Phosphorus is doped in a portion of impurity regions 149 and 150 (n-type impurity regions (a) 139 and 140 stated above) at a concentration of 1×10^{20} to 1×10^{21} atoms/cm^3. However boron is doped at a concentration higher by at least 3 times here. Therefore, already formed n-type impurity regions are totally inverted to p-type, and function as p-type impurity regions. Accordingly, it is acceptable to define impurity regions 149 and 150 as p-type impurity regions (a).

After removing resist mask 148, a protection film 151 is formed. A protection film 151 may be formed from an insulating film comprising silicon, concretely a silicon nitride film, a silicon oxide film, a silicon oxide nitride film or a laminate combining these films. The film thickness may be set at 20 to 200nm (preferably 30 to 150nm). In embodiment 1, a silicon nitride film with 50nm thickness is used. This protection film is effective for preventing increase in resistivity due to oxidation of the first wirings 11 and 12 and gate electrodes 121 to 124, in the heat treatment process (activation process) performed next.

A heat treatment process is performed next in order to activate the impurity elements of n-type or p-type conductivity and which have been doped at their respective concentrations. Furnace annealing, laser annealing, rapid thermal annealing (RTA), or lamp annealing can be performed for this process. The activation process is performed by furnace annealing in embodiment 1. Heat treatment is performed in a nitrogen atmosphere at between 300 and 650°C for 3 to 12 hours, preferably from 400 to 550°C for 4 to 6 hours, at 450°C for 2 hours here. (Fig. 3C)

The catalytic element (nickel in embodiment 1) used in crystallization of an amorphous silicon film in embodiment 1 moved in the direction of the arrows and is captured in a region containing phosphorus at a high concentration (gettering) formed in the process of Fig. 3A. This is a phenomenon originated from gettering effect of a metal element by phosphorus. As a result, the concentration of nickel contained in later formed channel forming regions 152 to 156 is reduced below $1x10^{17}$ atoms/cm^3 (preferably to $1x10^{16}$ atoms/cm^3).

Conversely, the catalytic element precipitated at a high concentration in the regions which functioned as gettering sights of the catalytic element (regions where impurity regions 139 to 147 were formed in the process of Fig. 3A). The catalytic element existed in these regions at a concentration exceeding $5\text{x}10^{18}$ atoms/cm^3 (typically 1×10^{19} to 5×10^{20} atoms/cm^3).

Further, a hydrogenation process is performed on the active layers by performing heat treatment in an atmosphere containing 3 to 100% hydrogen at 300 to 550°C for 1 to 6 hours (350°C for 2 hours in embodiment 1). This is a process to terminate dangling bonds in the semiconductor layers by thermally activated hydrogen. Plasma hydrogenation (using hydrogen activated by plasma) may be performed as another hydrogenation means.

After completing the activation process, the protection film 151 is selectively removed. Here, attention should be paid not to remove the first wirings (including gate electrodes), gate insulating film, active layers, etc., at the same time with removing the protection film 151. Since silicon nitride film is used as the protection film 151 in this embodiment it may be easily removed by wet etching using a mixed etching species of hydrofluoric acid aqueous and ammonium fluoride solution. In addition, as a protection film that is easily removed, it is effective to use a silicon oxide film that is formed by applying solution.

While activation process is performed with the protection film 151 in embodiment 1, the activation process may be performed without a protection film. In such cases, it is preferable to reduce oxygen concentration as possible in the heat treatment atmosphere so as not to form oxide on the surfaces of gate electrodes 121 to 124, the first wiring 11 and 12. In concrete, the oxygen concentration is kept 1ppm or lower, preferably 0.1ppm or lower. The process of removing the protection film 151 can be omitted by doing so.

After removing the protection film 151, a film comprising aluminum or a material which has aluminum as its main component (hereinafter referred to as aluminum type thin film) is formed to form the second wirings 13 and 14 having lower resistivity than the first wirings. In embodiment 1, aluminum film containing 2 wt% of silicon is used as the aluminum type thin film. The second wiring 13 is formed on the first wiring 11 which later becomes an input-output signal wiring, and the second wiring 14 is formed on the first wiring 12. Note that it is preferable to fabricate the second wirings 13 and 14 inside of the first wirings 11 and 12 by 0 to 2 m. (Fig. 3D)

The first interlayer insulating film 157 is next formed into 500nm to 1.5 m. In embodiment 1 the first inter layer insulating film 157 if formed by silicon oxide film into 1 m thickness by plasma CVD. Needless to say, a laminate structure combining insulating films comprising silicon such as a laminate of a silicon nitride film and a silicon oxide film may also be adopted. Further, it is possible to use organic resin films such as polyimide, acrylic, polyamide, polyimide amide, BCB (benzocyclobutene) may also be adopted for the first interlayer insulating film.

Contact holes are then formed in order to reach the source regions or the drain regions of the respective TFTs, and source wirings 158 to 161, and drain wirings 162 to 165 are formed. Note that, although not shown in the figures, the drain wirings 162 and 163 are connected as the same drain wiring in order to form a CMOS circuit. Note that, although not shown in the figures, in embodiment 1 the electrodes are made with a three-layer structure laminate film of a 100 nm Ti film, a 300 nm aluminum film containing Ti, and a 150 nm Ti film formed successively by sputtering. Also note that a copper wiring and a titanium nitride wiring may be laminated as a source wiring or a drain wiring. (Fig. 4A)

A silicon nitride film, a silicon oxide film, or a silicon oxide nitride film is formed to a thickness of between 50 and 500 nm (typically 200 to 300 nm) next as a passivation film 166. A plasma treatment using a gas that contains hydrogen such as H_2 and NH_3 may be performed preceding formation of the film and heat treatment may be performed after the film formation. The preceding process provides excited hydrogen into the first interlayer insulating film. By performing a heat treatment to this state, the active layers are effectively hydrogenated because hydrogen added into the first interlayer insulating film is diffused in the layer underneath, as well as improving the film quality of passivation film 166.

Further, after forming the passivation film 166, an additional hydrogenation process may be performed. For example, it is good to perform heat treatment for 1 to 12 hours at between 300 and 450°C in an atmosphere including from 3 to 100% hydrogen. Or, a similar result can be obtained by using plasma hydrogenation. Note that openings may be formed here in the passivation film 166 at positions where contact holes will be formed later in order to connect the pixel electrode and the drain wirings.

A second interlayer insulating film 167 made from an organic resin is formed next with an approximately 1 μm thickness. Polyimide, acrylic, polyamide, polyimide amide, BCB (benzocyclobutane), etc., can be used as the organic resin. The following points can be given as the benefits of using an organic resin film: easy film deposition; the parasitic capacitance can be reduced because the specific dielectric constant is low; and superior levelness. Note that in addition to the above, other organic resin films, organic SiO compounds, etc. can be used. A thermal polymerization type polyimide is used here, and after application to the substrate, it is baked at 300°C to form the film.

Further, it is possible to provide a resin film colored by pigment etc. as a part of layer of the second interlayer insulating film 167 and use is as the color filter.

A shielding film 168 is formed next on the second interlayer insulating film 167 in the region that becomes the pixel section. A term "shielding film" is used through the specification to have a meaning of shielding light or electromagnetic wave. The shielding film 168 is a film of an element chosen from among aluminum (Al), titanium (Ti), and tantalum (Ta), chromium (Cr), tungsten (W) or a film with one of these as its principal constituent, formed to a thickness of between 100 and 300 nm. In embodiment 1 an aluminum film containing titanium at 1wt% is formed into 125nm thick.

Note that if an insulating film such as a silicon oxide film is formed to a thickness of 5 to 50 nm on the second interlayer insulating film 167, then the adhesiveness of the shielding film formed on top can be increased. Further, if plasma processing using CF_4 gas is performed on the surface of the second interlayer insulating film 167, which is formed by an organic resin, then the adhesiveness to the shielding film formed on this film can be increased by surface refinement.

Further, it is possible to form other connecting wirings, not only the shielding film, by using the film containing titanium. For example, a connecting wiring for connecting between circuits can be formed inside the driver circuit. However, in this case, before depositing the material that forms the shielding film or the connecting wiring, it is necessary to form contact holes, in advance, in the second interlayer insulating film 167.

Next, an oxide film 168 with a thickness from 20 to 100 nm (preferably between 30 and 50 nm) is formed on the surface of the shielding film 168 by anodic oxidation or plasma oxidation. An aluminum oxide film (alumina film) is formed here as the anodic oxide film 169 because an aluminum film, or a film with aluminum as its principal constituent, is used as the shielding film 168 in embodiment 1.

When performing anodic oxidation processing, a tartaric acid ethylene glycol solution with a sufficiently low alkaline ion concentration is first manufactured. This is a solution in which a 15% tartaric acid ammonium aqueous solution and an ethylene glycol solution are mixed in a 2:8 ratio. Aqueous ammonia is added thereto so that the pH is regulated to be 7±0.5. A platinum electrode is placed in the solution as a cathode, the substrate on which the shielding film 168 is formed is immersed in the solution, and a constant dc current (from several mA to several tens mA) is applied with the shielding film 168 as an anode.

The voltage between the cathode and the anode in the solution changes along with time in accordance with the oxide film growth. The voltage is increased at an increase rate of 100V/min under a constant current, and the anodic oxidation process is stopped when the voltage becomes 45 V. Thus the anodic oxide film 169 can be formed with a thickness of approximately 50nm on the surface of the shielding film 168. As a result, the thickness of the shielding film 168 will be 90nm. Note that the numerical values shown here for the anodic oxidation process are only examples, and that they may naturally be changed to the most suitable values depending upon the size of the element being manufactured, etc.

Further, the structure used here has the insulating film being formed only on the surface of the shielding film, but the insulating film may also be formed by a gas phase method, such as plasma CVD, thermal CVD, or sputtering. In that case, it is preferable to make the film thickness from 20 to 100 nm (more preferably between 30 and 50 nm). Furthermore, a silicon oxide film, a silicon nitride film, a silicon oxide nitride film, a DLC (diamond like carbon) film, or an organic resin film may also be used. Further, a combined laminate film of these may be used.

Contact holes are formed next in the second interlayer insulating film 167 and in the passivation film 166 in order to reach the drain wiring 165, and the pixel electrode 170 is formed. Note that pixel electrodes 170 and 171 are each separate pixel electrodes for adjoining pixels. A transparent conductive film may be used for the pixel electrodes 170 and 171 for the case of a transmission type liquid crystal display device, while a metallic film may be used for a reflective type liquid crystal display device. A compound film of indium oxide and tin oxide (referred to as ITO film) with a thickness of 110 nm is formed here by sputtering because a transmission type liquid crystal display device is used here.

Further, a storage capacitor 172 is formed at this point where the pixel electrode 170 and the shielding film 168 overlap through the anodic oxide film 169. In this case it is preferable to set the shielding film 168 at floating state (electrically isolated state) or a constant electric potential, more preferably at a common electric potential (median electric potential of image signals sent as data).

Thus, the active matrix substrate, containing the CMOS circuit, which becomes a driver circuit, and the pixel matrix circuit on the same substrate, is completed. Note that in Fig. 4B a p-channel TFT 301, and n-channel TFTs 302 and 303 are formed in the driver circuit, and that a pixel TFT 304 is formed from an n-channel TFT in the pixel matrix circuit.

Note that the process order of embodiment 1 may be properly altered. Whatever the order may be, the basic function of the active matrix substrate does not differ as long as the structure of finally formed TFT is one shown in Fig. 4B, and the effect of the present invention is not impaired.

A channel forming region 201, a source region 202 and a drain region 203 are each formed by a p-type impurity region (a) in the p-channel TFT 301 of the driver circuit. Note that a region that contains phosphorus at a concentration of 1×10^{20} to 1×10^{21} atoms/cm^3 exists in a portion of a source region or a drain region in effect. Further in that region the catalytic element gettered in the process of Fig. 3B exists at a concentration exceeding 5×10^{18} atoms/cm^3 (typically 1×10^{19} to 5×10^{20} atoms/cm^3).

Further, a channel forming region 204, a source region 205, and a drain region 206 are formed in the n-channel TFT 302, and a region overlapping with the gate wiring by interposing a gate insulating film (such region is referred to as Lov region. 'ov' means overlap) 207 is formed in one side of the channel forming region (drain region side). Here, Lov region 207 contains phosphorus at a concentration of 2×10^{16} to 5×10^{19} atoms/cm^3, and is formed to completely overlap with the gate wiring.

An Lov region is disposed only on one side of the channel forming region 204 (only on the drain region side) in Fig. 4B, in order to reduce resistive constituents as possible. However, it is acceptable to provide Lov regions by sandwiching the channel forming region 204.

A channel forming region 208, a source region 209, and a drain region 210 are formed in the n-channel TFT 303. LDD regions 211 and 212 are formed in both sides of the channel forming region. Note that the regions overlapping with the gate wiring by interposing an insulating film (Lov regions) and the regions that are not overlapped with the gate wiring (such region is referred to as Loff regions. 'off' means offset) are realized because a portion of the LDD regions 211 and 212 are placed so as to overlap with the gate wiring in this structure.

A cross sectional view shown in Fig. 6 is an enlarged diagram showing n-channel

TFT 303 shown in Fig. 4B in the state of being manufactured to the process of Fig. 3C. As shown here, LDD region 211 is further classified into Lov region 211a and Loff region 211b. Phosphorus is contained in the Lov region 211a at a concentration of 2×10^{16} to 5×10^{19} atoms/cm^3, whereas it is contained at a concentration 1 to 2 times as much (typically 1.2 to 1.5 times) in the Loff region 211b.

Further, channel forming regions 213 and 214, a source region 215, a drain region 216, Loff regions 217 to 220, and an n-type impurity region (a) 221 contacting the Loff regions 218 and 219 are formed in the pixel TFT 304. The source region 215, and the drain region 216 are each formed n-type impurity region (a) at this point, and the Loff regions 217 to 220 are formed by n-type impurity region (c).

The structure of the TFTs forming each of the circuits of the pixel circuit and the driver circuits can be optimized to correspond to the required circuit specifications, and the operation performance of the semiconductor device and its reliability can be increased in embodiment 1. Specifically, the LDD region placement in an n-channel TFT is made to differ depending upon the circuit specifications, and by using an Lov region or an Loff region properly, TFT structures with fast operating speeds and which place great importance on measures to counter hot carriers, and TFT structures that place great importance on low off current operation, can be realized on the same substrate.

For the case of an active matrix type liquid crystal display device, for example, the n-channel TFT 302 is suitable for driver circuits that place great importance on high speed, such as a shift register circuit, a frequency divider circuit (a signal divider circuit), a level shifter circuit, and a buffer circuit. In other words, by placing the Lov region in only one side (the drain region side) of the channel forming region, this becomes a structure that reduces the resistive constituents as much while placing great importance on hot carrier countermeasures. This is because, for the case of the above circuit group, the source region and the drain region functions do not change, and the carrier (electron) movement direction is constant. However, if necessary, Lov regions can be placed in both sides of the channel forming region.

Further, the n-channel TFT 303 is suitable for a sampling circuit (also referred to as a transfer gate) which places emphasis on both hot carrier countermeasures and low off current operation. In other words, hot carrier countermeasures can be realized by placement of the Lov region, and in addition, low off current operation is realized by placement of the Loff region. Furthermore, the functions of the source region and the drain region of a sampling circuit reverse, and the carrier movement direction changes by 180°; therefore a structure that has linear symmetry with the center of the gate wiring must be used. Note that it is possible to only form the Lov region, depending upon the circumstances.

Further, the n-channel TFT 304 is suitable for a pixel circuit or a sampling circuit (sample hold circuit) which place great importance on low off current operation. Namely, the Lov region, which is a cause of an increase in the off current value, is not employed, only the Loff region is used, allowing low off current operation to be realized. Furthermore, by utilizing an LDD region with a concentration lower than that of the driver circuit LDD region as the Loff region, although the on current value will fall a little, it is a thorough measure for lowering the off current value. Additionally, it has been confirmed that an n-type impurity region (a) 221 is extremely effective in lowering the off current value.

Further, the length (width) of the Lov region 207 of the n-channel TFT 302 may be between 0.1 and 3.0 μm, typically from 0.2 to 1.5 μm, for a channel length of 3 to 7 μm. Further, the length (width) of the Lov regions 211a and 212a of the n-channel TFT 303 may be from 0.1 to 3.0 μm, typically between 0.2 and 1.5 μm, and the length (width) of the Loff regions 211b and 212b may be from 1.0 to 3.5 μm, typically between 1.5 and 2.0 μm. Moreover, the length (width) of the Loff regions 217 to 220 formed in the pixel TFT 304 may be from 0.5 to 3.5 μm, typically between 2.0 and 2.5 μm.

An input-output signal wiring 305 formed from a laminate structure of the first wiring 11 and the second wiring 13 comprising aluminum, and a gate wiring 306 formed from a laminate structure of the first wiring 12 and the second wiring 14 are formed on the active matrix substrate of embodiment 1. Here, the reason for employing such laminate structure will be explained in the following.

A wiring formed in a long distance such as an input-output signal wiring and a gate wiring is required to have a low resistivity. Specifically in making an active matrix substrate of over diagonal 4 inches, resistive constituents of this long wiring will greatly affect the circuit design. Accordingly, it is desired that the resistivity of the wiring formed in the active matrix substrate be as small as possible.

Therefore in embodiment 1 a measure is taken to reduce the wiring resistivity by laminating a wiring having resistivity of 0.1 to 10 μΩ cm like as the second wirings 13 and 14 over a wiring having resistivity of approximately 10 to 500 μΩ cm such as the first wirings 11 and 12. In other words, a laminate wiring is employed in which the second wiring having resistivity of 0.1 to 10 μΩ cm (typically from 1 to 5 μ Ω cm) is laminated onto the first wiring having resistivity of 10 to 500 μΩ cm (typically 10 to 30 μΩ cm). In this case, it is preferable that the resistivity of the second wiring is 1/10 to 1/100 times of resistivity of the first wiring.

Note that the embodiment 1 is characterized in that it uses such structure to a specific sections such as an input-output signal wiring and a portion of the gate wiring. There is a fear that the wiring using above stated laminate structure has a comparatively broad wiring width such as 6 to 8 μ m in patterning precision. In such cases it is inappropriate to use them into a gate electrodes that require minute fabrication, or into a connection wiring inside the driver circuit that is integrated in high density.

Further, since the wiring resistivity of a short wiring that connect TFTs inside the driver circuit or of a gate electrode need not be concerned, the function is sufficiently obtained even only with the first wiring. Namely, the wiring formed from the above stated laminate structure may preferably used for a wiring that does not require minute processing, and it is preferable to use only the first wiring in which minute processing is possible for the wiring that requires minute processing even if the resistivity is sacrificed more or less.

The use of a wiring formed from the above stated laminate structure for the input-output signal wiring 305 and the gate wiring (except regions that function as gate electrodes) 306 resides in such reason. Needless to say, the laminate structure may be used without any problem even for the wiring inside the driver circuit and for the gate electrode if the laminate structure may be used (if minute processing is possible).

Another characteristic of the present invention is that the p-channel TFT 301 is formed in self-aligned manner, and n-channel TFTs 302 to 304 are formed in non self-aligned manner.

By using alumina film which has high dielectric constant of 7 to 9 for the dielectric of the storage capacitor in this embodiment, it became possible to reduce the area in which a required capacitor. Further, by using the shielding film formed over pixel TFT as one of the electrodes for the storage capacitor as in embodiment 1, aperture ratio in the image display section of the active matrix liquid crystal display device can be improved.

The structure of the storage capacitor of the present invention is not necessarily limited to the one shown in embodiment 1. For example, the storage capacitor described in Japanese Patent Application Laid-Open No. Hei 9-316567 or Japanese Patent Application Laid-Open No. Hei 10-254097 may be used.

[Embodiment 2]

A process of manufacturing an active matrix type liquid crystal display device from an active matrix substrate is next explained. As shown in Fig. 5, an alignment film 401 is formed for the substrate in the state of Fig. 4B. In the present embodiment, a polyimide film is used for the alignment film. An opposing electrode 403 comprising transparent conductive film and an alignment film 404 are formed on an opposing substrate 402. Color filter or a shielding film may be formed on the opposing substrate if necessary.

After forming the alignment films, a rubbing process is performed to give the liquid crystal molecules a certain fixed pre-tilt angle, so that they are aligned. The active matrix substrate, on which a pixel circuit and driver circuits are formed, and the opposing substrate are stuck together through a sealing material, spacers, or a resin film provided by patterning (not shown in the figures) in accordance with a known cell assembly process. A liquid crystal material 405 is next injected between both substrates, and the cell is completely sealed by a sealant (not shown in the figures). A known liquid crystal material may be used as the liquid crystal material. Thus the active matrix type liquid crystal display device shown in Fig. 5 is completed.

The structure of the active matrix liquid crystal display device is next described by referring to the perspective view of Fig. 7. In order to correspond Fig. 7 to cross sectional view of Figs. 1A to 4B, common reference numerals are used. The active matrix substrate comprises a pixel section 701, scanning (gate) signal driver circuit 702, image (source) signal driver circuit 703 formed over a glass substrate 100. A pixel TFT 304 of the pixel section is an n-channel TFT, and driver circuits disposed to surround the pixel circuit are basically formed from CMOS circuits. Scanning signal driver circuit 702 and image signal driver circuit 703 are respectively connected to the pixel section 701 through gate wiring 306 and source wiring 161. A terminal 705 connected to FPC 704 and the driver circuit are connected through input-output signal wiring 305.

[Embodiment 3]

Fig. 8 shows an example of circuit structure of the active matrix substrate shown in embodiment 2. The active matrix substrate of embodiment 3 has a image signal driver circuit 801, a scanning signal driver circuit (A) 807, a scanning signal driver circuit (B) 811, a pre-charge circuit 812, and a pixel section 806. Through the Specification, driver circuit is a generic name including image signal driver circuit 801 and a scanning signal driver circuit 807.

The image signal driver circuit 801 is provided with a shift register 802, a level shifter 803, a buffer 804, and a sampling circuit 805. Further, the scanning signal driver circuit (A) 807 is provided with a shift register 808, a level shifter 809, and a buffer 810. The scanning signal driver circuit (B) 811 has a similar structure.

The driver voltages for the shift register 802 and 808 is between 5 and 16 V here (typically 10 V), and the structure shown by reference numeral 302 in Fig. 4B is suitable for n-channel TFTs used in the CMOS circuits forming the shift registers.

Furthermore, the driver voltage becomes high at between 14 and 16 V for the level shifter 803 and 809, and the buffer 804 and 810, but similar to the shift registers, CMOS circuits containing the n-channel TFT 302 shown in Fig. 4B are suitable. Note that using a multi-gate structure, such as a double gate structure and a triple gate structure for the gate wiring is effective in increasing reliability in each circuit.

Further, the sampling circuit 805 has a driver voltage of between 14 and 16 V, but the source region and the drain region are inverted and it is necessary to reduce the off current value, so CMOS circuits containing the n-channel TFT 303 of Fig. 4B are suitable. Note that only the n-channel TFT is shown in Fig. 4B, but in practice the n-channel TFT and a p-channel TFT are combined when forming the sampling circuit.

Further, the pixel section 806 has a driver voltage of between 14 and 16 V, but it is necessary to reduce the off current value even lower than that of the sampling circuit 805. Therefore it is preferable to use a structure in which Lov region is not disposed, and it is preferable to use n-channel TFT 304 of Fig. 4B for the pixel TFT.

Note that the structure of embodiment 3 can be easily realized by manufacturing a TFT according to manufacturing method shown in embodiment 1. Though the embodiment 3 shows only the structures of pixel section and driver circuit, it is possible to form a signal divider circuit, a frequency divider circuit, D/A converter circuit, operational amplifier circuit, γ compensation circuit, and further signal processing circuits (they may also be referred to as logic circuits) such as a memory and a micro processor over a same substrate by following the manufacturing method of embodiment 1.

As stated above, the present invention enables to materialize a semiconductor device comprising a pixel section and a driver circuit for driving the pixel section over a substrate, such as a semiconductor device having a driver circuit and a pixel circuit over a same substrate.

[Embodiment 4]

In embodiment 4 pixel structures of the pixel section that may be fabricated according to manufacturing process of embodiment 1, are described by referring to Fig. 9. Note that pixel TFTs of double gate structure are shown in all of the examples in embodiment 4 but other multi-gate structures such as a triple gate structure may be used or a single gate structure may be used.

In Fig. 9A, 901 is an active layer; 902, gate wiring comprising the first wiring 902a and the second wiring 902b; 903, gate electrode formed from only the first wiring 902a; and 904, source wiring.

In Fig. 9B, 905 is an active layer; 906, gate wiring comprising the first wiring 906a and the second wiring 906b; 907, gate electrode formed from only the first wiring 906a; and 908, source wiring.

In Fig. 9C, 909 is an active layer; 910, gate wiring comprising the first wiring 910a and the second wiring 910b; 911, gate electrode formed from only the first wiring 910a; and 912, source wiring.

In Fig. 9D, 913 is an active layer; 914, gate wiring comprising the first wiring 914a and the second wiring 914b; 915, gate electrode formed from only the first wiring 914a; and 916, source wiring.

As shown above, the structure of the present invention can be used for any pixel structure. Note that the structure of embodiment 4 can be realized in accordance with embodiment 1, and can be combined with any of the structure of embodiment 2 and 3.

[Embodiment 5]

In embodiment 5 a pixel structure of the pixel section that can be fabricated in accordance with the manufacturing process of embodiment 1 is explained by using Fig. 10. Needless to say, while embodiment 5 shows an example of a triple gate structured pixel TFT, it may be a double gate structure or a single gate structure.

A cross sectional diagram along A-A' line in the top view shown in Fig. 10A corresponds to Fig. 10B. In Fig. 10A: 21 is an active layer; 22, gate wiring comprising first wiring 22a and second wiring 22b; 23, gate electrode formed from only first wiring 22a (reference numeral is applied onto only one of the 3 gate electrodes); 24, capacitance wiring comprising first wiring 24a and second wiring 24b.

The first wiring 24a that forms the capacitance wiring is formed so as to largely overlap with a portion of the active layer 21. There is an insulating film (dielectric of storage capacitor) 33 that was formed at the same time with the gate insulating film (the same layer and comprised of the same material), in between the first wiring 24a and the active layer 21, and there is formed a storage capacitor 25.

In addition, 26 is source wiring; 27, drain wiring; 28, contact section between source wiring and active layer; 29, contact section between drain wiring and active layer; 30, pixel electrode (transparent conductive film in embodiment 5); 31, contact section between pixel electrode and drain wiring; and 32, image display region.

Embodiment 5 is characterized by using the laminated wiring of the first wiring and the second wiring that is used for input-output signal wiring and gate wiring, also for capacitance wiring. By doing so the electric potential of the capacitance wiring can be more stabilized, and accurate expression of gray scale is made possible in case of liquid crystal display device.

Note that the structure of embodiment 5 can be realized in accordance with embodiment 1, and can be combined with any of the structure of embodiment 2 to 4.

[Embodiment 6]

In embodiment 6 an active matrix liquid crystal display device having a pixel section of a structure different from that of embodiment 1 is described by using Fig. 11. Note that the basic structure is the same as Fig. 5, and description is made by concentration on only the parts that differ.

The structure of pixel TFT (n-channel TFT) 310 that form the pixel section differ from embodiment 1 in the structure of Fig. 11. In concrete, embodiment 6 differ in that offset regions 47 to 50 are formed between channel forming regions 41 and 42 and LDD regions formed by n-type impurity region (c) 43 to 46.

Note that an offset region designates a region that is a semiconductor layer of the same constitution with a channel forming region, and do not overlap with a gate electrode, as shown by 47 to 50. These offset regions 47 to 50 function simply as a resistant, and are very effective in reducing off current value.

In order to realize such structure, an insulating film comprising silicon may be formed into 20 to 200nm thickness (preferably 25 to 150nm) to cover gate wiring etc. prior to doping of n-type impurity element in the process of Fig. 2D of embodiment 1, for example.

Impurity elements are doped in the state in which an insulating film comprising silicon is formed in the side wall of gate electrode 124, and an offset region is formed with that section functioned as a mask. Accordingly the length of the offset region thus formed almost coincide with the thickness of the insulating film comprising silicon, and become 20 to 200nm (preferably 25 to 150nm).

The insulating film comprising silicon has already been described in embodiment 1, but it is preferable to use the same material as the gate insulating film in embodiment 6 so that it can be removed at the same time with the gate insulating film in the process of Fig. 2E.

Note that the structure of embodiment 6 can be realized by alternating a part of embodiment 1, and can be combined with any of the structure of embodiment 2 to 5.

[Embodiment 7]

In embodiment 7 a case of manufacturing an active matrix substrate by a manufacturing process different from embodiment 1 is described by using Fig. 12A to 12C.

First, processes up to Fig. 3C are performed in accordance with the manufacturing process of embodiment 1. Note however that while embodiment 1 used a 50nm thick silicon nitride film as the protection film, embodiment 7 uses a 300nm thick silicon oxide nitride film 51. (Fig. 12A)

Contact holes are opened in the silicon oxide nitride film 51 on first electrode 11 that will become input-output signal wiring and first electrode 12 that will become gate wiring. Second wirings 53 and 54 having low resistivity are formed by a film formed from aluminum as its principal component (aluminum film added with 2wt% of silicon in embodiment 7). (Fig. 12B)

Thus an active matrix substrate having a driver circuit and a pixel section and structured by Fig. 12C is completed. In Fig. 12C, p-channel TFT 320, n-channel TFTs 321 and 322 are formed in the driver circuit, and a pixel TFT 323 formed by n-channel TFT is formed in the pixel section. Further, input-output signal wiring 324 and gate wiring 325 are formed.

The functions of these TFTs 320 to 323, input-output signal wiring 324 and gate wiring 325 are as described in embodiment 1, therefore the description is omitted here. The different points with the active matrix substrate shown in Fig. 4B of embodiment 1 are:

that the protection film 51 is remained, and that the structure of input-output signal wiring 324 and gate wiring 325 differed. Therefore, in regard to the function and the effect, those of similar to embodiment 1 can be obtained.

Note that it is needless to say that an active matrix liquid crystal display device is completed by combining embodiment 7 with embodiment 2, and that it is possible to freely combine with any structure of embodiments 3 to 6.

[Embodiment 8]

In the structure shown in embodiment 1, any low resistive material may be used as the second wiring. In concrete, copper or a film having copper as its main component (hereinafter referred to as copper type thin film), silver or a film having silver as its main component (hereinafter referred to as silver type thin film), or a laminate film combining these can be used other than aluminum or a film having aluminum as its main component (hereinafter referred to as aluminum type thin film) shown in embodiment 1.

Moreover, a film formed from a material such as titanium, titanium nitride, tantalum, tantalum nitride, tungsten, tungsten nitride, molybdenum, niobium, etc., may be laminated onto the above stated aluminum type thin film, copper type thin film or aluminum type thin film. The laminating order may be either upper or lower, and a structure in which the second wiring is sandwiched may also be employed. These films are specifically effective in the case of using aluminum type thin film as the second wiring, and can prevent generation of hillocks etc.

Further, above stated aluminum type thin film, copper type thin film or aluminum type thin film are materials that are very easily oxidized and cause insulation defect. Therefore by laminating above stated thin film of titanium etc. on the upper surface of the second wiring the electric contact with other wirings may become easier.

Note that the structure of embodiment 8 can be freely combined with any structure of embodiment 2 to 7 in addition to embodiment 1.

[Embodiment 9]

While embodiment 1 showed an example of using catalytic element that promotes crystallization as a method of forming the semiconductor film including crystalline structure, embodiment 9 shows a case of forming the semiconductor film including crystalline structure by thermal crystallization or by laser crystallization without using the catalytic element.

In case of using thermal crystallization, heat treatment at 600 to 650°C for 15 to 24 hours may be performed after forming a semiconductor film including amorphous structure. Namely, crystallization proceeds from natural nucleus formation by performing heat treatment at a temperature exceeding 600°C.

In case of laser crystallization, laser annealing process may be performed in the first annealing condition shown in embodiment 1 after forming a semiconductor including amorphous structure. By doing so, a semiconductor that include crystalline structure can be formed in a short time. Needless to say, a lamp annealing may be performed in place of the laser annealing.

As shown above, the semiconductor film including crystalline structure used in the present invention can be formed by using any publicly known means. Note that the structure of embodiment 9 can be freely combined with the structures of embodiment 1 to 8.

[Embodiment 10]

A case of forming an active matrix substrate from a different manufacturing process from that of embodiment 1 is described in embodiment 10.

In embodiment 1, a technique in which crystallization process is performed by using the technique disclosed in Japanese Patent Application Laid-Open Hei 7-130652 and then gettering the catalyst element used in the crystallization into source and drain regions at the same time with activation of source and drain regions, was used.

However it is also possible to use the technique disclosed in Japanese Patent Application Laid-Open Hei 10-270363 (corresponding to U.S. Patent Application Serial No. 09/050,182) for the processes of crystallization through gettering. In the case of using the technology disclosed in this gazette, after performing crystallization process using catalyst element, a region containing an element belonging to periodic table group 15 (typically phosphorus) is selectively formed and the catalyst element is gettered into the region.

Further as another method, it is possible to use the technique disclosed in Japanese Patent Application Laid-Open No. Hei 10-247735 (corresponding to U.S. Patent Application Serial No. 09/034,041) for the processes from crystallization process through gettering process.

As described above, the semiconductor film including crystallization structure used in the present invention may be formed from various methods from public domain. Note that the structure of embodiment 10 can be freely combined with the structures of embodiments 1 to 8.

[Embodiment 11]

In the present invention, wiring resistance is reduced by applying a laminated structure comprising the first wiring and the second wiring to gate wirings and /or capacitor wirings as shown in Fig. 10. Here, Fig. 1 shows a case of using the laminated layer having the first wiring comprising TaN/Ta layer (laminated layer comprising tantalum nitride layer and tantalum or a tungsten layer as, and the second wiring comprising Al-Nd layer (aluminum layer added neodymium).

Incidentally, while forming the first and the second wiring in this embodiment, hest treatment is performed in nitrogen atmosphere containing oxygen at a concentration of 1 ppm or less at 500°C fro 4 hours after forming the first wiring, and then the second wiring is formed on the first wiring. After that, we measured the sheet resistance.

As shown by Chart 1, although the sheet resistance in case of using a single layer comprising TaN/TaN layer is 8 Ω/□, the sheet resistance in case of laminating the Al-Nd layer thereon is reduced to 0.16 Ω/□. Moreover, this feature means that a good electric contact is formed in spite of performing a heat treatment under the condition of exposing the first wiring.

[Embodiment 12]

Fig. 22 shows a graph of relationship between drain current (ID) and gate voltage (VG) of the n-channel TFT 302 fabricated by the process steps according to the Embodiment 1 (Hereinafter, ID-VG curve), and relationship between field effect mobility (μ_{FE}) and the gate voltage (VG) of the n-channel TFT. Here, a source voltage (VS) is 0V and a drain voltage (VD) is 1V or 14V. Incidentally, the n-channel TFT has a channel length (L) of 7.2 μm, a channel width (W) of 8.0 μm and a thickness of a gate insulating film (Tox) of 120 nm.

Fig. 22 shows the ID-VG curve and the field effect mobility in which the bold lines represent the characteristic before a stress test and the dotted lines represent the characteristic after the stress test. This graph proves that there is little changes in the ID-VG curve before and after the stress test and the degradation owing to hot carriers is restrained. Incidentally, the stress test here is performed under the condition that a source voltage at 0V, a drain voltage at 20V and a gate voltage at 4V are applied for 60 seconds at a room temperature, in order to promote the degradation owing to the hot carriers.

[Embodiment 13]

It is possible to use the present invention when forming an interlayer insulating film on a conventional MOSFET, and then forming a TFT on that. In other words, it is possible to realize a semiconductor device with a three dimensional structure. Further, it is possible to use an SOI substrate such as SIMOX, Smart-Cut (a trademark of SOITEC corporation), or ELTRAN (a trademark of Cannon, Inc.)

Note that it is possible to freely combine the structure of embodiment 11 with the structure of any of embodiments 1 to 10.

[Embodiment 14]

It is possible to use a variety of liquid crystal materials in a liquid crystal display device manufactured in accordance with the present invention. The following can be given as examples of such materials: a TN liquid crystal; PDLC (polymer diffusion type liquid crystal); an FLC (ferroelectric liquid crystal); an AFLC (antiferroelectric liquid crystal); and a mixture of an FLC and an AFLC.

For example, the liquid crystal materials disclosed in: Furue, H, et al., "Characteristics and Driving Scheme of Polymer-stabilized Monostable FLCD Exhibiting Fast Response Time and High Contrast Ratio with Gray-scale Capability," SID, 1998; in Yoshida, T., et al., "A Full-color Thresholdless Antiferroelectric LCD Exhibiting Wide Viewing Angle with Fast Response Time," SID 97 Digest, 841, 1997; S. Inui et al., "Thresholdless antiferroelectricity in liquid crystals and its application to displays, 671-673, J. Mater. Chem. 6(4), 1996; and in US Patent Number 5,594,569 can be used.

In particular, among an antiferroelectric liquid crystal material with no threshold value (thresholdless antiferroelectric LCD: abbreviated TL-AFLC) that shows electrooptical response characteristic in which transmittance is continuously varied against electric field, is used, there are some that show V-shaped (or U-shaped) electrooptical response characteristic, and even liquid crystals whose operating voltage is approximately ±2.5 V are found. Accordingly there are some cases where power supply voltage for the pixel section is on the order of 5 to 8 V and that indicates a possibility of driving the driver circuit and the pixel circuit with the same power supply voltage. Namely, the entire liquid crystal display device can be made low power consumption.

Further, ferroelectric liquid crystals and anti-ferroelectric liquid crystals possess an advantage in that they have a high response time compared to TN liquid crystals. Since TFTs used in the present invention can achieve TFTs whose operation speed is very fast, it is possible to realize a liquid crystal display device having fast image response speed in which fast response speed of ferroelectric liquid crystal and antiferroelectric liquid crystal is sufficiently utilized.

Further, thresholdless antiferroelectric mixed liquid crystal has large spontaneous polarization in general, and the dielectric constant of liquid crystal itself is large. Therefore, comparatively large storage capacitor is required in the pixel in case of using thresholdless antiferroelectric mixed liquid crystal for a liquid crystal display device. It is preferable to use thresholdless antiferroelectric mixed liquid crystal having small spontaneous polarity. From this point of view, the storage capacitor shown in Fig. 4B of embodiment 1 is preferable because it can store a large capacitance in a small area.

It is needless to say that the use of liquid crystal display device of embodiment 12 for display of electronic devices such as personal computer etc. is effective.

The structure of the present invention can be freely combined with any structure of embodiment 1 to 10 and 13.

[Embodiment 15]

It is possible to apply the present invention to an active matrix type EL display. An example of this is shown in Fig. 13.

Fig. 13 is a circuit diagram of an active matrix type EL display. Reference numeral 81 denotes a display region, and an x-direction (source side) driver circuit 82 and a y-direction (gate side) driver circuit 83 are disposed in the peripheral. Further, each pixel in the display region 81 has switching TFT 84, a capacitance 85, a current controlling TFT 86, and an EL element 87, and the switching TFT 84 is connected to x-direction signal lines (source signal lines) 88a (or 88b) and to y-direction signal lines (gate signal lines) 89a (or 89b, 89c). Furthermore, power supply lines 90a and 90b are connected to the current controlling TFT 86.

In an active matrix EL display of the embodiment 15, an x-direction driver circuit 82 and a y-direction driver circuit 83 are formed by combining p-channel TFT 301 and n-channel TFT 302 or 303 of Fig. 4B. N-channel TFT 304 of Fig. 4B is used for switching TFT 84 and p-channel TFT 301 is used for current controlling TFT 86. Needless to say, the combination of TFT need not be limited to the above.

Any structure of embodiments 1 to 10, 13 and 14 to the active matrix EL display of embodiment 15.

[Embodiment 16]

An explanation of the example of the manufacture of an active matrix type EL (electro-luminescence) display device using the present invention is given in embodiment 16. Fig. 14A is a top view of an EL display device using the present invention, and Fig. 14B is a cross sectional diagram of the display.

In Fig. 14A, reference numeral 4001 denotes a substrate, 4002 denotes a pixel section, 4003 denotes a source side driver circuit, and 4004 denotes a gate side driver circuit. Each of the drive circuits is lead to an FPC (flexible print circuit) 4006 through wiring 4005, and thus connected to external equipment.

First sealing material 4101, cover material 4102, fillers 4103 and second sealing material 4104 are provided to surround the pixel section 4002, source side driver circuit 4003 and gate side driver circuit 4004.

Fig. 14B corresponds to a diagram of cross section at A-A' of Fig. 14A. A driver circuit TFT (an n-channel TFT and a p-channel TFT are shown here) 4201 that comprises a source side driver circuit 4003 and a current control TFT (TFT that controls the current to the EL) that comprises a pixel section 4002 are formed over the substrate 4001.

TFTs of the same structures as p-channel TFT 301 and n-channel TFT 302 of Fig. 4B are used for driver TFT 4201 and TFT of the same structure as p-channel TFT 301 of

Fig. 4B is used for current control TFT 4202 in embodiment 14. A storage capacitor (not shown) connected to the gate of current control TFT 4020 is provided in pixel section 4002.

An interlayer insulating film (a planarization film) 4301 made of resin material is formed over driver TFT 4201 and pixel TFT 4202. Pixel electrode (anode) 4302 is formed thereon that is connected to the drain of pixel TFT 4202. A transparent conductive film having a large work function is used as the pixel electrode 4302. A compound of indium oxide and tin oxide (called ITO), or a compound of indium oxide and zinc oxide can be used as the transparent conductive film.

An insulating film 4303 is formed on pixel electrode 4302, and an opening is formed in insulating film 4303 at an area over pixel electrode 4302. EL (electro-luminescence) layer 4304 is formed on pixel electrode 4302 in the opening section. A publicly known organic EL material or inorganic EL material can be used for the EL layer 4304. There are monomer type material and polymer type material in the organic material, and either can be used.

The formation method of EL layer 4304 may apply publicly known evaporation technique or coating technique. The structure of EL layer may be a single layer structure or a laminate structure in which hole injection layer, hole transport layer, illumination layer, electron transport layer and electron injection layer are freely combined.

A cathode 4305 comprising a conductive film having light shielding property (typically a conductive film whose principal component is aluminum, copper or silver, or a laminate film of these and other conductive film) is formed over EL layer 4304. It is preferable to remove as much as possible of the moisture and oxygen existing in the interface between the cathode 4305 and the EL layer 4304. Therefore, it is necessary to form these films continuously in a vacuum, or to form the EL layer 4304 in a nitrogen atmosphere or in a noble gas and then form cathode 4305 keeping out the contact of oxygen and moisture. In embodiment 14 deposition described above is enabled by using deposition apparatus of multi-chamber method (cluster-tool method).

Cathode 4305 is connected to wiring 4005 in the region shown as 4306. Wiring 4005 is a wiring for applying a determined voltage to the cathode 4305 and is connected to FPC 4006 through anisotropic conductive film 4307.

As described above, EL elements comprising pixel electrode (anode) 4302, EL layer 4304 and cathode 4305 are formed. EL elements are surrounded by a first sealing material and a cover material 4012 stacked to substrate 4001 by first sealing material 4101, and sealed with fillers 4103.

As the cover material 4102, glass plate, metal plate (typically stainless plate), ceramics plate, FRP (fiberglass-reinforced plastics) plate, PVF (polyvinyl fluoride) film, Myler film, polyester film or acrylic film can be used. Further, a sheet having a structure in which aluminum foil is sandwiched by PVF film or Myler film.

Provided, the cover material need to be transparent in case that radiation from EL elements are directed to the direction toward cover material. In such cases, transparent substances such as glass plate, plastic plate, polyester film or acrylic film are used.

A ultraviolet ray curing resin or a thermosetting resin can be used as filler 4103, and PVC (polyvinyl chloride), acrylic, polyimide, epoxy resin, silicone resin, PVB (polyvinyl butyral), or EVA (ethylene vinyl acetate) can be used. If a drying agent (preferably barium oxide) is formed on the inside of the filler 4103, deterioration of EL elements can be prevented.

Further, spacers may be included within the filler 4103. When the spacers are formed of from barium oxide, it is possible to give the ability to absorb moisture to the spacers themselves. In addition, it is effective to provide a resin film over cathode 4305, as a buffer layer that releases pressure from the spacers in case of disposing the spacers.

The wiring 4005 is electrically connected to the FPC 4006 through anisotropic conductive film 4307. Wiring 4005 transmits signals that are sent to pixel section 4002, source side driver circuit 4003 and gate side driver circuit 4004 from FPC 4006, and is electrically connected to an external device by FPC 4006.

In embodiment 16 a structure that thoroughly shields the EL elements from external atmosphere is employed in which second sealing material 4104 is provided so as to cover the exposed portions of first sealing material 4101 and a part of FPC 4006. Thus an EL display device having a cross sectional structure of Fig. 14B is complete. Note that EL display device of embodiment 16 may be fabricated in combination with any structure of embodiments 1to 10 and 13 to 15.

A more detailed structure on a cross section of pixel section is shown in Fig. 15, a top view if shown in Fig. 16A, and circuit diagram is shown in Fig. 16B. Common reference numerals are used in Figs. 15, 16A and 16B, so that the figures may be compared with each other.

In Fig. 15, switching TFT 4402 disposed over substrate 4401 comprises an n-channel TFT 304 of Fig. 4B. Accordingly, the description of n-channel TFT 304 may be referred, regarding the description of the structure. The wiring shown by 4403 is a gate wiring that electrically connects gate electrodes 4404a and 4404b of switching TFT 4402.

While embodiment 16 uses a double gate structure in which 2 channel forming regions are formed, a single gate structure in which a channel forming region is formed or a triple gate structure in which 3 channel forming regions are formed may also be used.

The drain wiring 4405 of switching TFT 4402 is electrically connected to gate electrode 4407 of current control TFT 4406. Note that current control TFT is comprised of a p-channel TFT 301 of Fig. 4B. Accordingly, the description of p-channel TFT 301 may be referred, as to the structure. Note that while embodiment 16 uses a double gate structure, a single gate structure or a triple gate structure may also be used.

A first passivation film 4408 is disposed over the switching TFT 4402 and the current control TFT 4406, and a planarization film 4409 comprising resin is formed on top. It is very important to flatten by using the planarization film 4409, the step due to the TFTs.

Since an EL layer formed later is extremely thin, there are cases in which defective luminescence is caused due to the existence of the step. Therefore, it is preferable to planarize before forming pixel electrode so as to form an EL layer on a planarized surface as possible.

The reference numeral 4410 denotes a pixel electrode (anode of EL element) comprising a transparent conductive film, and is electrically connected to the drain wiring 4411 of current control TFT 4406. A compound comprising indium oxide and tin oxide or a compound comprising indium oxide and zinc oxide can be used as pixel electrode 4410.

An EL layer 4412 is formed on pixel electrode 4410. Note that while Fig. 15 shows only 1 pixel, EL layers corresponding to each colors of R (red), G (green) and B (blue) are each formed properly in embodiment 14. A monomer type organic EL material is formed by evaporation in embodiment 14. In concrete, a laminate structure is formed from a copper phthalocyanine (CuPc) film of 20nm disposed as a hole injection layer, and tris-8-quinolinolate aluminum complex (Alq_3) film formed thereon into 70nm thickness as a luminescent layer. A luminescent color may be controlled by adding fluorescent dye such as quinacridon, or DCM1 into Alq_3.

However, the above example is one example of the organic EL materials that can be used as luminescence layers, and it is not necessary to limit to these materials. An EL layer (a layer for luminescence and for performing carrier motion for luminescence) may be formed by freely combining luminescence layer, charge transport layer, or charge injection layer. For example, an example using monomer type materials as luminescence layers is shown in embodiment 16, but polymer type organic EL materials may also be used. Further, it is possible to use inorganic materials such as silicon carbide, etc., as charge transport layer and charge injection layer. Publicly known materials can be used for these organic EL materials and inorganic materials.

A cathode 4413 comprising a conductive film having light shielding property is next formed on EL layer 4412. In the case of embodiment 16, an alloy film of aluminum and lithium is used as the conductive film having light shielding property. Needless to say, a publicly known MgAg film (alloy film of magnesium and silver) may also be used. As the cathode material, a conductive film comprising an element belonging to periodic table group 1 or 2, or a conductive film added with at least one of these elements, may be used.

EL element 4414 is completed at the point when this cathode 4413 is formed. Note that an EL element 4414 formed here represents a capacitor comprising pixel electrode (anode) 4410, EL layer 4412 and cathode 4413.

The top structure of the pixel in embodiment 16 is next described by using Fig. 16A. Source region of switching TFT 4402 is connected to source wiring 4415 and drain region is connected to drain wiring 4405. Further, drain wiring 4405 is electrically connected to gate electrode 4407 of current control TFT 4406. Source region of current control TFT 4406 is electrically connected to current supply line 4416 and drain region is electrically connected to drain wiring 4417. Drain wiring 4417 is electrically connected to pixel electrode (anode) 4418 shown by dotted line.

Here, a storage capacitor is formed in the region shown by 4419. Storage capacitor 4419 is formed from a semiconductor film 4420 electrically connected to current supply line 4416, a gate insulating film formed of the same layer as gate insulating film (not shown) and gate electrode 4407. Further, it is possible to use a capacitance formed from gate electrode 4407, a layer formed from the same layer as the first interlayer insulating film (not shown) and current supply line 4416, for a storage capacitor.

In fabricating an EL display device of embodiment 16, the structures of embodiment 1 to 10 and 13 to 15may be freely combined.

[Embodiment 17]

In embodiment 17 an EL display device comprising a pixel structure differing from embodiment 16 is described. Fig. 17 is used for explanation. Note that the description of embodiment 16 may be referred regarding parts where the same reference numerals as Fig. 15 are given.

In Fig. 17 a TFT having the same structure as n-channel TFT 302 of Fig. 4B as current control TFT 4501. Needless to say, gate electrode 4502 of current control TFT 4501 is connected to drain wiring 4405 of switching TFT 4402. Drain wiring 4503 of current control TFT 4501 is electrically connected to pixel electrode 4504.

In embodiment 17 pixel electrode 4504 is formed by using a conductive film having light shielding property, and functions as a cathode of EL element. An alloy film of aluminum and lithium is used in concrete, but a conductive film comprising an element belonging to periodic table group 1 or 2, or a conductive film added with such element may be used here.

EL film 4505 is formed on top of pixel electrode 4504. Note that though Fig. 17 shows only 1 pixel, EL layer corresponding to G (green) is formed in embodiment 15 by evaporation method or coating method (preferably spin coating). In concrete, it is a laminate structure comprising a lithium fluoride (LiF) film of 20nm thickness provided as electron injection layer and a PPV (poly-p-phenylene vinylene) of 70nm thickness provided thereon as luminescence layer.

An anode 4506 comprising transparent conductive film is next disposed on EL layer 4505. In embodiment 17, a compound comprising indium oxide and tin oxide or a compound comprising indium oxide and zinc oxide is used.

On completing formation of anode 4506, an EL element 4507 is finished. Note that EL element 4507 represents here a capacitor formed from pixel electrode (cathode) 4504, EL layer 4505 and anode 4506.

Here that current control TFT 4501 has a structure of present invention has a very important meaning. Since current control TFT 4501 is an element for controlling current amount that flow in EL element 4507, a lot of current flow there and the element has a great danger of deterioration by heat or hot carriers. The structure of present invention is therefore effective, in which an LDD region 4509 is disposed so as to overlap the gate electrode 4502 by interposing gate insulating film 4508 on the drain side of current control TFT 4501.

In addition, the current control TFT 4501 of embodiment 17 forms a parasitic capacitance, which is referred to as gate capacitor, in between gate electrode 4502 and LDD region 4509. It is possible to provide the same function as storage capacitor 4418 shown in Figs. 16A and 16B by adjusting this gate capacitor. Specifically in case of driving the EL display device by digital driving method, it is possible to use the gate capacitor for storage capacitor because the capacitance of storage capacitor is small compared to the case of driving by analog driving method.

Note that in fabrication of EL display device of embodiment 17 the structures of embodiments 1to 11 and 13 to 15 may freely be combined.

[Embodiment 18]

In embodiment 18, examples of pixel structures that can be used for pixel section of EL display device shown in Embodiments 16 and 17 are shown in Figs. 18A to 18C. Note that in embodiment 16, reference numeral 4601 denotes a source wiring of a switching TFT 4602, 4603a and 4603b denotes a gate wiring of the switching TFT 4602, 4604 denotes a current control TFT, 4605 denotes a capacitor, 4606 and 4608 denote current supply lines, and 4607 denotes an EL element.

Fig. 18A is an example of a case in which the current supply line 4606 is shared between two pixels. Namely, this is characterized in that two pixels are formed having linear symmetry around the current supply line 4606. In this case the number of power supply lines can be reduced, so the pixel section can be made higher definition.

Fig. 18B is an example of a case in which the current supply line 4608 is formed parallel to the gate wiring 4603a and 4603b. Note that Fig. 18B has a structure in which the current supply line 4608 and the gate wiring 4603a and 4603b are formed so as not to overlap. However in case these are wirings formed on different layers, they can be provided so as to overlap by interposing an insulating film. In this case, the area used exclusively by the current supply line 4608 and the gate wiring 4603a and 4603b can be shared, so the pixel section can be made even higher definition.

Furthermore, Fig. 18C is characterized in that the current supply line 4608 is formed parallel to gate wiring 4603a and 4603b, similar to the structure of Fig. 18B, and in addition, two pixels are formed to have linear symmetry around the current supply line 4608. It is also effective to form the current supply line 4608 to overlap one of gate wiring 4603a or 4603b. In this case the number of power supply lines can be reduced, so the pixel section can be made higher definition.

[Embodiment 19]

Electrooptical device or semiconductor circuit formed in accordance with the present invention can be used as display section or signal processing circuit of electric machines. The following can be given as examples of this type of electric machines: video cameras; digital cameras; projectors; projection TVs; goggle type displays (head mounted displays); navigation systems; sound reproduction devices; notebook type personal computers; game machines; portable information terminals (such as mobile computers, portable telephones, portable game machines or electronic notebook etc.); image reproduction devices having recording media; etc. Some examples of these are shown in Figs. 19A to 19F, 20A to 20D and 21A to 21B.

Fig. 19A is a portable telephone, and comprises a main body 2001, a voice output section 2002, a voice input section 2003, a display section 2004, operation switches 2005, and an antenna 2006 etc. The electrooptical device of the present invention can be applied to the display section 2004, and semiconductor circuit of the present invention can be applied to the voice output section 2002, to the voice input section 2003, and to CPU or memory etc.

Fig. 19B is a video camera, and comprises a main body 2101, a display section 2102, a voice input section 2103, operation switches 2104, a battery 2105, and an image receiving section 2106. The electrooptical device of the present invention can be applied to the display section 2102 and semiconductor circuit of the present invention can be used for voice input section 2103, CPU or memory etc.

Fig. 19C is a mobile computer, and comprises a main body 2201, a camera section 2202, an image receiving section 2203, operation switches 2204, and a display section 2205. The electrooptical device of the present invention can be applied to the display section 2205 and semiconductor circuit of the present invention can be used for CPU or memory etc.

Fig. 19D is a goggle type display, and comprises a main body 2301, display section 2302, and arm sections 2303. The electrooptical device of the present invention can be applied to the display section 2302 and semiconductor circuit of the present invention can be used for CPU or memory etc.

Fig. 19E is a rear type projector (projection TV), and comprises a main body 2401, a light source 2402, liquid crystal display device 2403, polarizing beam splitter 2404, reflectors 2405 and 2406, a screen 2407. The present invention can be applied to the liquid crystal display device 2403 and semiconductor circuit of the present invention can be used for CPU or memory etc.

Fig. 19F is a front type projector, and comprises a main body 2501, a light source 2502, a liquid crystal display device 2503, an optical system 2504 and a screen 2505. The present invention can be applied to the liquid crystal display device 2503 and semiconductor circuit of the present invention can be used for CPU or memory etc.

Fig. 20A is a personal computer, and comprises a main body 2601, an image input section 2602, a display section 2603, and a keyboard 2604. The electrooptical device of the present invention can be applied to the display section 2603 and semiconductor circuit of the present invention can be used for CPU or memory etc.

Fig. 20B is an electronic game machine and comprises a main body 2701, a recording medium 2702, a display section 2703 and a controller 2704. Voice or image outputted from this electronic game machine is reproduced by a display comprising an exterior cover 2705 and display section 2706. Wire communication, wireless communication or optical communication may be used as a communication means between controller 2704 and main body 2701 or between electronic game machine and display. In embodiment 17, the structure in which infrared radiation is detected by sensors 2707 and 2708 is employed.

Fig 20C is a player that uses a recording medium on which a program is recorded (hereinafter referred to as a recording medium), and comprises a main body 2801, a display section 2802, a speaker section 2803, a recording medium 2804, and operation switches 2805. Note that music appreciation, film appreciation, games, and the use of the Internet can be performed with this device using a DVD (digital versatile disk), a CD, etc., as a recording medium. The electrooptical device of the present invention can be applied to the display section 2802 and semiconductor circuit of the present invention can be used for CPU or memory etc.

Fig. 20D is a digital camera, and comprises a main body 2901, a display device 2902, a viewfinder 2903, operation switches 2904, and an image receiving section (not shown in the figure). The electrooptical device of the present invention can be applied to the display section 2902 and semiconductor circuit of the present invention can be used for CPU or memory etc.

The optical engine shown in Fig. 21A comprises an optical light source system 3001, mirrors 3002 and 3005 to 3007, dichroic mirrors 3003 and 3004, optical lenses 3008a to 3008c, a prism 3011, a liquid crystal display device 3010, and an optical projection system 3012. The optical projection system 3012 is an optical system provided with a projection lens. Embodiment 17 shows an example of triple stage, but there are no special limits and a single stage is acceptable, for example. Further, the operator may set optical systems such as optical lenses, film having polarizing function, film to regulate the phase difference, IR films, etc., suitably within the optical path shown by an arrow in Fig. 21A.

As shown in Fig. 21B, the optical light source system 3001 comprises light sources 3013 and 3014, composing prism 3015, collimator lenses 3016 and 3020, lens arrays 3017 and 3018, polarizing conversion element 3019. Note that the optical light source shown in Fig. 21B used 2 light sources, but it may be 1 or 3 or more. Further, it is acceptable to suitably place optical lenses, film having polarizing function, film to regulate the phase difference, IR films, etc.

As shown above, the applicable range of the present invention is very large, an it is possible to apply to electric machines of various area. Further, the electric machine of embodiment 19 can be realized by utilizing structures of any combination of embodiments 1 to 10, and 13 to 18.

By using the present invention, it becomes possible to dispose circuits having appropriate performance corresponding to specification required by the circuit over a substrate. The operation performance and reliability of an electrooptical device can be greatly improved.

Further, a storage capacitor having a large capacity in a small area can be formed in the pixel section of an electrooptical device typified by a liquid crystal display device. Accordingly, it is possible to keep a sufficient storage capacitor without decreasing aperture ratio (portion of effective display area against pixel area).

Moreover, the operation performance and reliability of electric machines having such electrooptical device as a display section.

What is claimed is:

1. An electrooptical device having a pixel section and a driver circuit over a substrate, said electrooptical device comprising:

an n-channel TFT of said driver circuit having at least one LDD region that a portion of, or all of said LDD region overlaps a gate electrode of said n-channel TFT of said driver circuit with a gate insulating film interposed therebetween;

a pixel TFT of said pixel section having at least one LDD region that does not overlap said gate electrode of said pixel TFT with said gate insulating film interposed therebetween; and

a wiring comprising a first wiring having a same material and formed in a same layer as said gate electrode of said pixel TFT and a second wiring having a lower resistivity than said first wiring;

wherein said first wiring and said second wiring are laminated.

2. An electrooptical device according to claim 1 wherein an n-type impurity element is contained in said LDD region of said n-channel TFT of said driver circuit at concentration higher by 2 to 10 times than said LDD region of said n-channel TFT of said pixel TFT.

3. An electrooptical device according to claim 1 wherein an n-type impurity element is contained in a concentration range of 2×10^{16} to 5×10^{19} atoms/cm^3 in said LDD region of said n-channel TFT of said driver circuit, and in a concentration range of 1×10^{16} to 5×10^{18} atoms/cm^3 in said LDD region of said pixel TFT.

4. An electrooptical device according to claim 1 wherein said wiring is an input-output signal wiring or a gate wiring.

5. An electrooptical device according to claim 1 wherein a resistivity of said second wiring is 1/10 to 1/100 of a resistivity of said first wiring.

6. An electrooptical device according to claim 1 wherein a resistivity of said first wiring is from 10 to 500μΩcm, and a resistivity of said second wiring is from 0.1 to 10μΩcm.

7. An electrooptical device according to claim 1 wherein said first wiring comprises an element selected from the group consisting of tantalum, titanium, molybdenum, tungsten, chromium, niobium and silicon, and the second wiring comprises an element selected from the group consisting of aluminum, copper and silver.

8. An electrooptical device according to claim 1 wherein an offset region exists between a channel forming region and said LDD region of said pixel TFT.

9. An electrooptical device according to claim 1 wherein said electrooptical device is a display device selected from the group consisting of a liquid crystal display device and an electroluminescence display device.

10. An electrooptical device according to claim 9 wherein said display device is incorporated into an electronic apparatus selected from the groups consisting of a potable phone, a video camera, a mobile computer, a goggle-type display, a front-type projector, a rear-type projector, a personal computer, a game player, a recording medium and a digital camera.

11. An electrooptical device comprising a pixel section and a driver circuit over a substrate, said electrooptical device comprising:

said driver circuit having a first n-channel TFT in which all of an LDD region overlaps a gate electrode with a gate insulating film interposed therebetween, and a second n-channel TFT in which a portion of an LDD region overlaps said gate electrode with said gate insulating film interposed therebetween;

said pixel section having a pixel TFT in which an LDD region does not overlap said gate electrode of said pixel TFT with said gate insulating film interposed therebetween; and

a wiring comprising a first wiring having a same material and formed in a same layer as said gate electrode of said pixel TFT and a second wiring having a lower resistivity than said first wiring;

wherein said first wiring and said second wiring are laminated.

12. An electrooptical device according to claim 11 wherein an n-type impurity element is contained in said LDD region of said first n-channel TFT and/or said LDD region of said second n-channel TFT of said driver circuit at concentration higher by 2 to 10 times than said LDD region of said n-channel TFT of said pixel TFT.

13. An electrooptical device according to claim 11 wherein an n-type impurity element is contained in a concentration range of 2×10^{16} to 5×10^{19} atoms/cm^3 in said LDD region of said first n-channel TFT and said LDD region of said second n-channel TFT of said driver circuit, and in a concentration range of 1×10^{16} to 5×10^{18} atoms/cm^3 in said LDD region of said pixel TFT.

14. An electrooptical device according to claim 11 wherein said wiring is an input-output signal wiring or a gate wiring.

15. An electrooptical device according to claim 11 wherein a resistivity of said second wiring is 1/10 to 1/100 of a resistivity of said first wiring.

16. An electrooptical device according to claim 11 wherein a resistivity of said first wiring is from 10 to 500 $\mu\Omega$ cm, and a resistivity of said second wiring is from 0.1 to 10 $\mu\Omega$ cm.

17. An electrooptical device according to claim 11 wherein said first wiring comprises an element selected from the group consisting of tantalum, titanium, molybdenum, tungsten, chromium, niobium and silicon, and said second wiring comprises an element selected from the group consisting of aluminum, copper and silver.

18. An electrooptical device according to claim 11 wherein an offset region exists between a channel forming region and said LDD region of said pixel TFT.

19. An electrooptical device according to claim 11, wherein said electrooptical device is a display device selected from the group consisting of a liquid crystal display device and an electroluminescence display device.

20. An electrooptical device according to claim 19, wherein said display device is incorporated into an electronic apparatus selected from the group consisting of a potable phone, a video camera, a mobile computer, a goggle-type display, a front-type projector, a rear-type projector, a personal computer, a game player, a recording medium and a digital camera.

21. A method of manufacturing an electrooptical device that comprises a pixel section and a driver circuit over a substrate, said method comprising the steps of:

forming a semiconductor film containing crystalline structure over said substrate;

forming p-type impurity region (b) by doping a p-type impurity element into said semiconductor film;

forming n-type impurity region (b) by doping an n-type impurity element into a region of said semiconductor film, where an n-channel TFT of the driver circuit is formed;

forming an active layer by patterning said semiconductor film;

forming a gate insulating film over said active layer;

forming a conductive film over said gate insulating film;

forming a first wiring by patterning said conductive film;

forming n-type impurity region (c) by doping an n-type impurity element into said active layer by using said first wiring as a mask;

forming n-type impurity region (a) by doping an n-type impurity element into said active layer of said n-channel TFT;

forming p-type impurity region (a) by doping a p-type impurity element into said active layer of a p-channel TFT;

activating impurity elements doped into said p-type impurity region (a), said p-type impurity region (b), said n-type impurity region (a), said n-type impurity region (b) and said n-type impurity region (c), and

laminating a second wiring over the first wiring.

22. A method according to claim 21 wherein a resistivity of said second wiring is 1/10 to 1/100 of a resistivity of said first wiring.

23. A method according to claim 21 wherein a resistivity of said first wiring is from 10 to 500$\mu\Omega$cm, and a resistivity of said second wiring is from 0.1 to 10$\mu\Omega$cm.

24. A method according to claim 21 wherein said first wiring comprises an element selected from the group consisting of tantalum, titanium, molybdenum, tungsten, chromium, niobium and silicon, and said second wiring comprises an element selected from the group consisting of aluminum, copper and silver.

25. A method of manufacturing an electrooptical device having a pixel section and a driver circuit over a substrate, said method comprising the steps of:

forming a semiconductor film containing crystalline structure over said substrate;

performing a first light annealing onto said semiconductor film;

forming p-type impurity region (b) by doping a p-type impurity element into said semiconductor film;

forming n-type impurity region (b) by doping an n-type impurity element into a region of said semiconductor film, where an n-channel TFT of the driver circuit is formed;

performing a second light annealing onto said semiconductor film;

forming an active layer by patterning said semiconductor film;

forming a gate insulating film over said active layer;

forming a conductive film over said gate insulating film;

forming a first wiring by patterning said conductive film;

forming n-type impurity region (c) by doping an n-type impurity element into said active layer by using said first wiring as a mask;

etching said gate insulating film by using said first wiring as a mask;

forming n-type impurity region (a) by doping said n-type impurity element into said active layer of said n-channel TFT;

forming p-type impurity region (a) by doping said p-type impurity element into said active layer of a p-channel TFT;

activating impurity elements doped into said p-type impurity region (a), said p-type impurity region (b), said n-type impurity region (a), said n-type impurity region (b) and said n-type impurity region (c), and

laminating a second wiring over said first wiring.

26. A method according to claim 25 wherein a resistivity of said second wiring is 1/10 to 1/100 of a resistivity of said first wiring.

27. A method according to claim 25 wherein a resistivity of said first wiring is from 10 to 500$\mu\Omega$cm, and a resistivity of said second wiring is from 0.1 to 10$\mu\Omega$cm.

28. A method according to claim 25 wherein said first wiring comprises an element

selected from the group consisting of tantalum, titanium, molybdenum, tungsten, chromium, niobium and silicon, and said second wiring comprises an element selected from the group consisting of aluminum, copper and silver.

29. An electrooptical device having a pixel section and a driver circuit over a substrate, said electrooptical device comprising:

a laminated wiring comprising a first wiring and a second wiring

wherein said first wiring has a same material and formed in a same layer as a gate electrode of a pixel TFT in said pixel section

wherein said second wiring has a lower resistivity than said first wiring.

30. An electrooptical device according to claim 29 wherein said laminated wiring is an input-output signal wiring or a gate wiring.

31. An electrooptical device according to claim 29 wherein a resistivity of said second wiring is 1/10 to 1/100 of a resistivity of said first wiring.

32. An electrooptical device according to claim 29 wherein a resistivity of said first wiring is from 10 to 500 $\mu\Omega$ cm, and a resistivity of said second wiring is from 0.1 to 10 $\mu\Omega$ cm.

33. An electrooptical device according to claim 29 wherein said first wiring comprises an element selected from the group consisting of tantalum, titanium, molybdenum, tungsten, chromium, niobium and silicon, and the second wiring comprises an element selected from the group consisting of aluminum, copper and silver.

34. An electrooptical device according to claim 29 wherein said electrooptical device is a display device selected from the group consisting of a liquid crystal display device and an

electroluminescence display device.

35. An electrooptical device according to claim 34 wherein said display device is incorporated into an electronic apparatus selected from the groups consisting of a potable phone, a video camera, a mobile computer, a goggle-type display, a front-type projector, a rear-type projector, a personal computer, a game player, a recording medium and a digital camera.

Metal Material	Thickness (nm)	Sheet Resistance (Ω/□)
TaN/Ta	50/350	1.58
W	400	0.36
Al-Nd	250	0.19
TaN/Ta + Al-Nd	50/350 + 250	0.16
W + Al-Nd	400 + 250	0.12

Chart 1

Abstract of the Disclosure

An object of the present invention is to provide an electrooptical device having high operation performance and reliability, and a method of manufacturing the electrooptical device.

Lov region 207 is disposed in n-channel TFT 302 that comprises a driver circuit, and a TFT structure which is resistant to hot carriers is realized. Loff regions 217 to 220 are disposed in n-channel TFT 304 that comprises a pixel section, and a TFT structure of low off current is realized. An input-output signal wiring 305 and gate wiring 306 are formed by laminating a first wiring and a second wiring having lower resistivity than the first wiring, and wiring resistivity is steeply reduced.

Fig. 1A

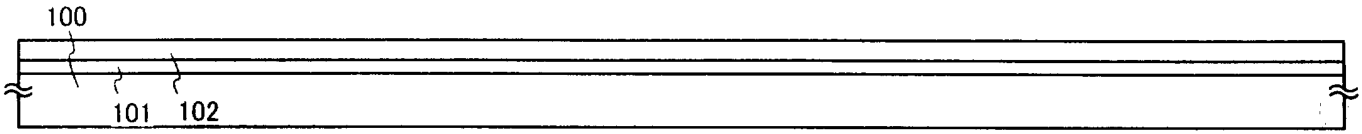


Fig. 1B

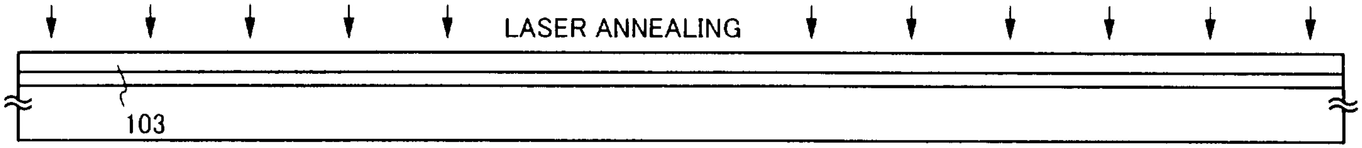


Fig. 1C

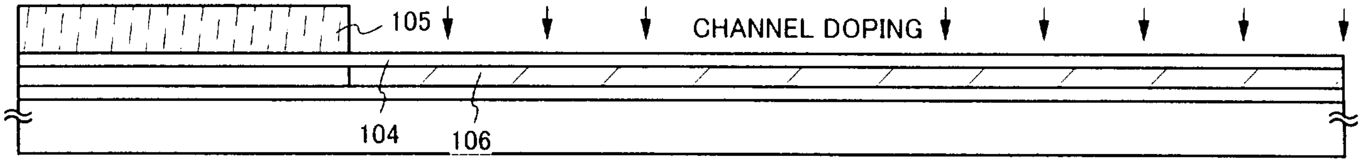


Fig. 1D

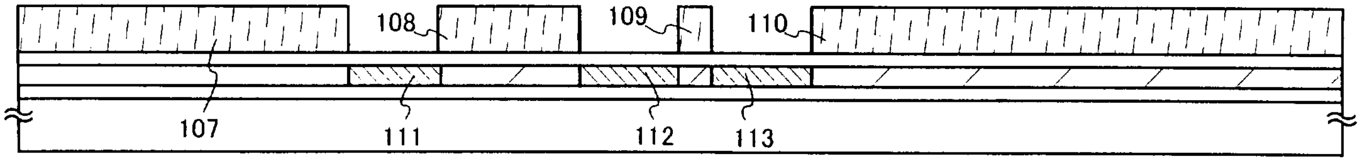


Fig. 1E

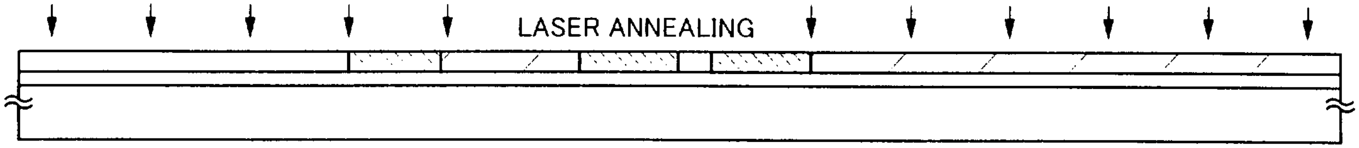


Fig. 1F

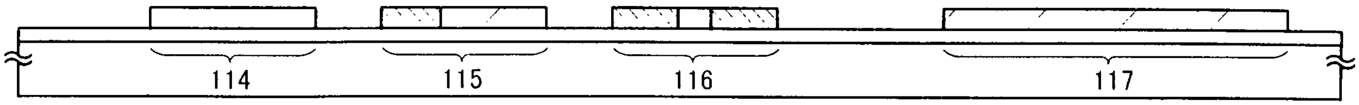


Fig. 2A

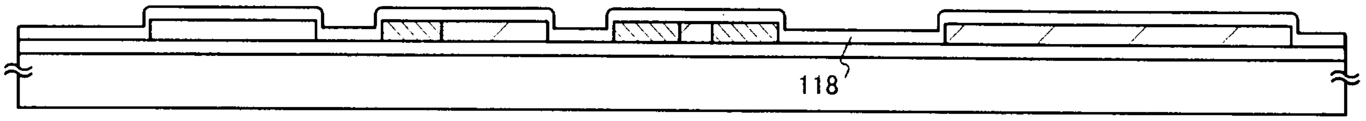


Fig. 2B

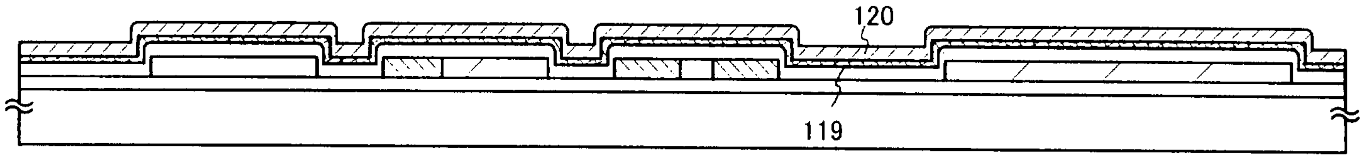


Fig. 2C

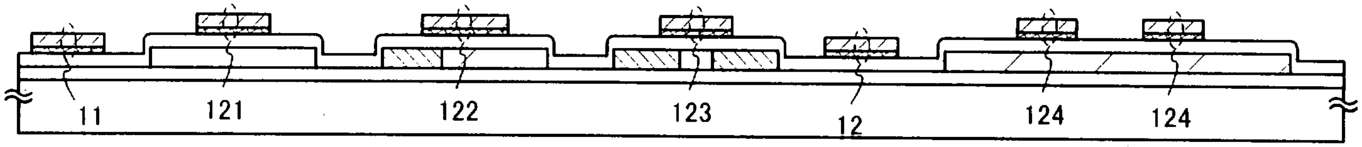


Fig. 2D

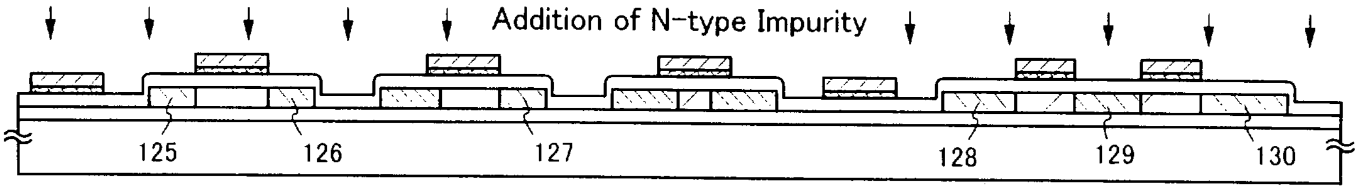


Fig. 2E

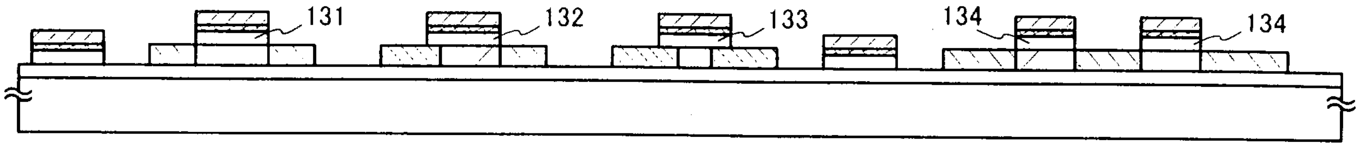


Fig. 3A

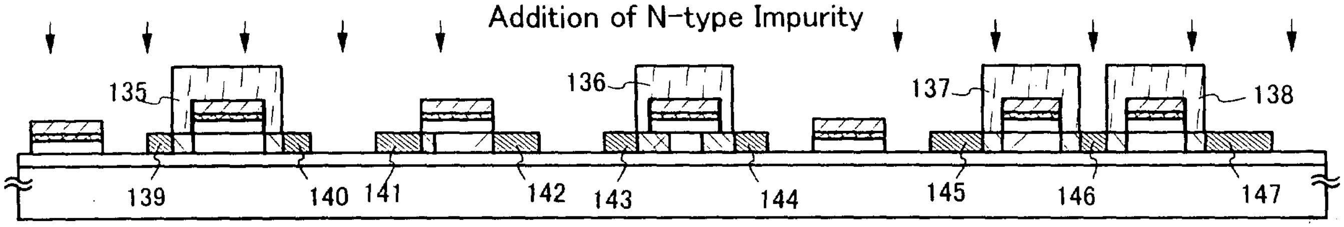


Fig. 3B

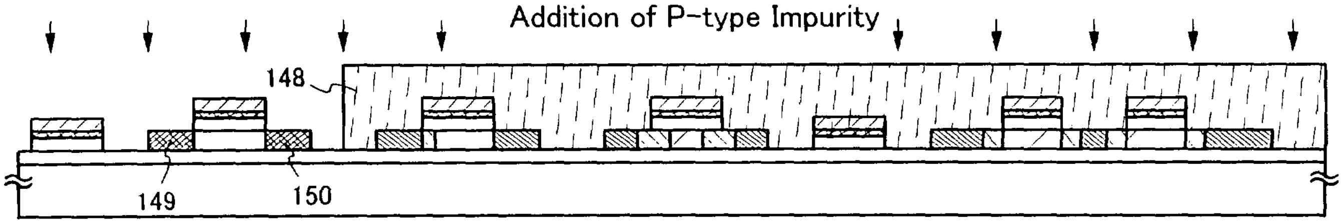


Fig. 3C

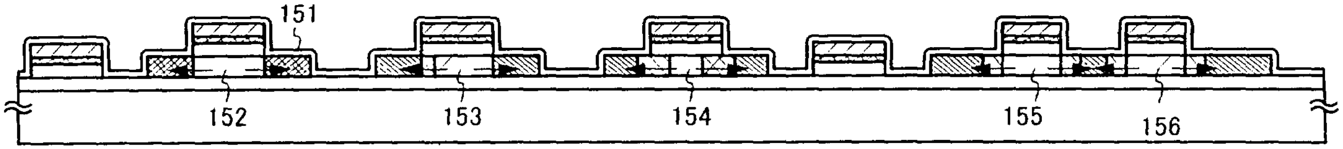


Fig. 3D

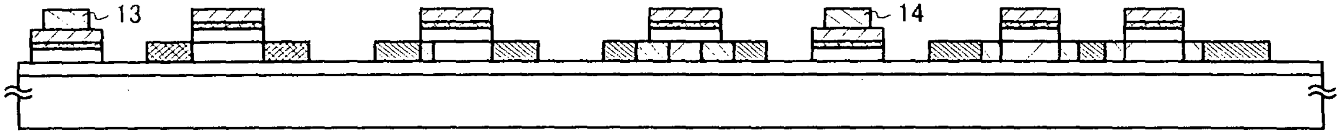
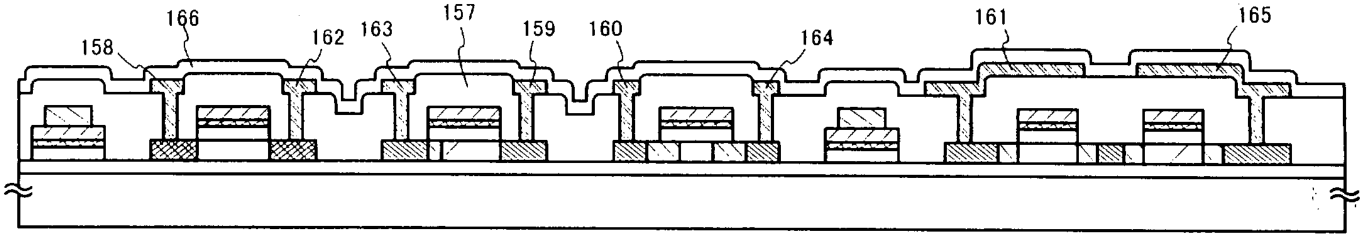


Fig. 4A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158
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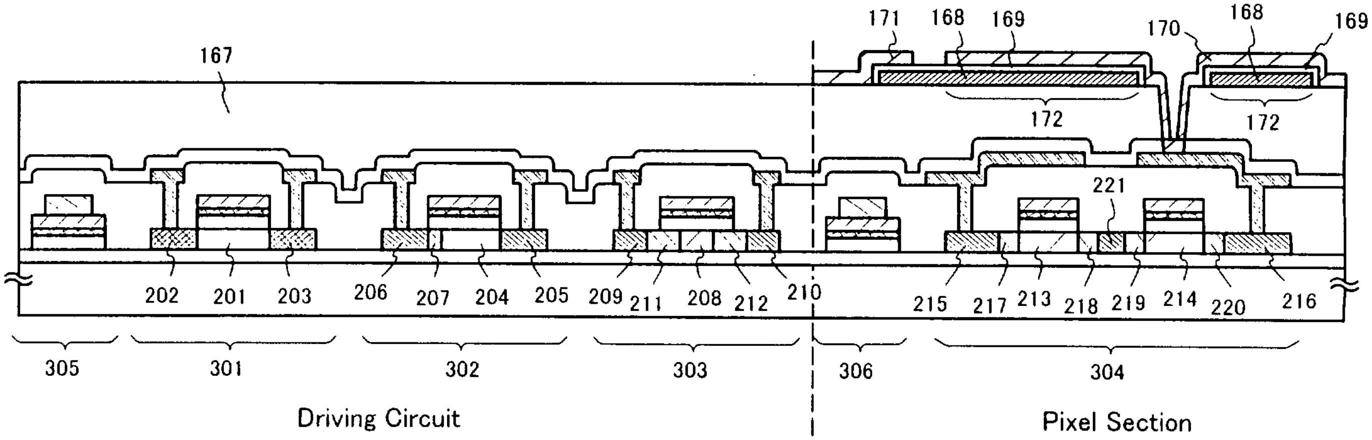
161
165

Fig. 4B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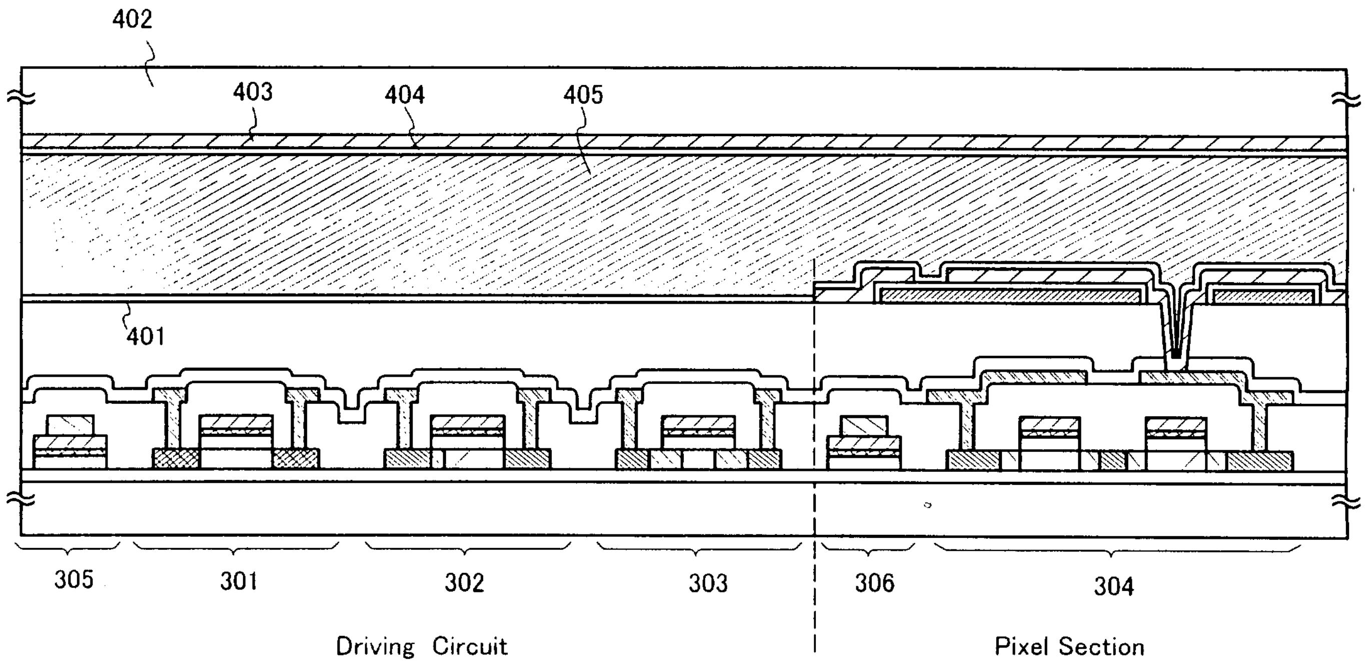
220
216
305
301
302
303
306
304
Driving Circuit
Pixel Section


402
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401
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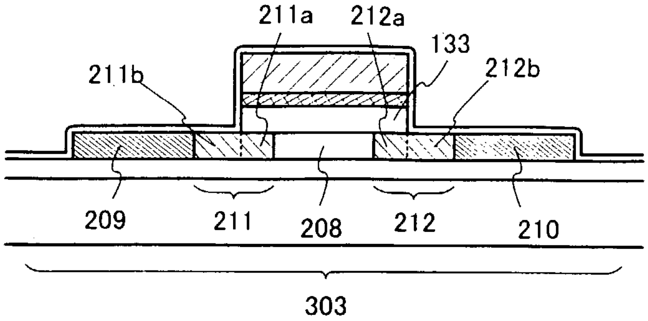
302
303
306
304
Driving Circuit
Pixel Section

Fig. 5



211a
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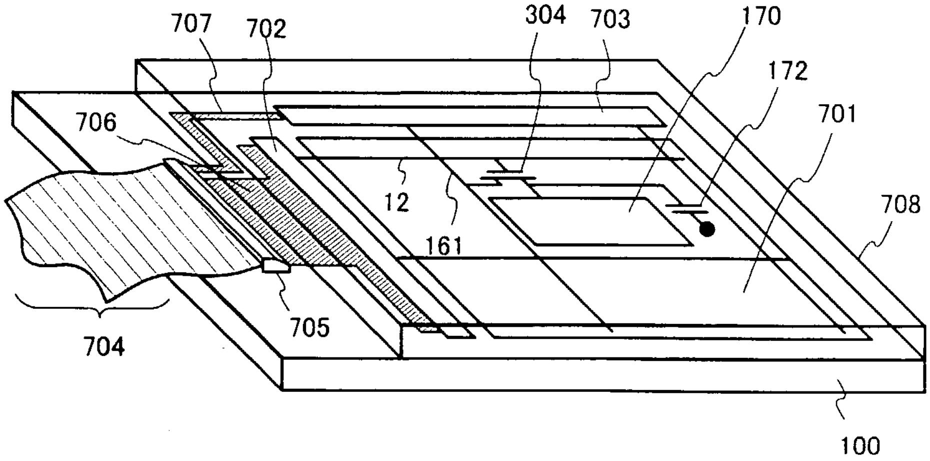
133
211b
212b
209
211
208
212
210
303

Fig. 6



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703
170
172
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12
708
161
704
705
100

Fig. 7

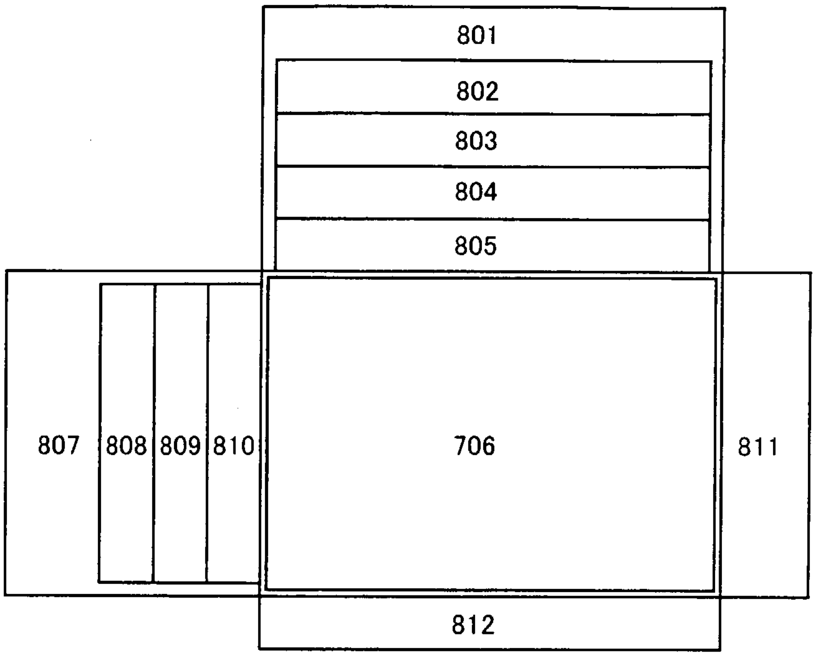


Fig. 8

Fig. 9A

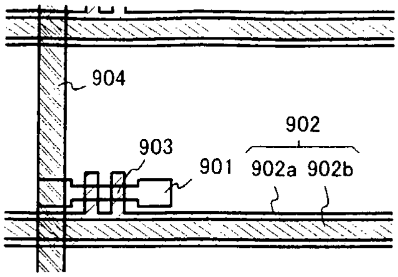


Fig. 9B

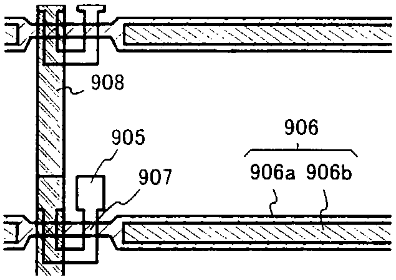


Fig. 9C

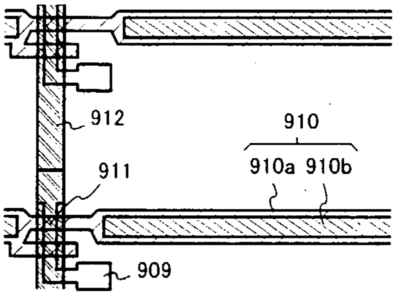
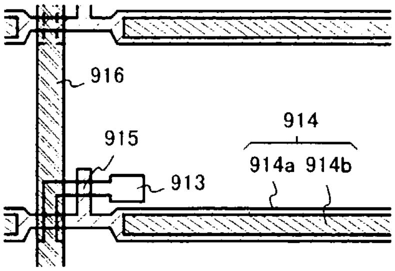


Fig. 9D



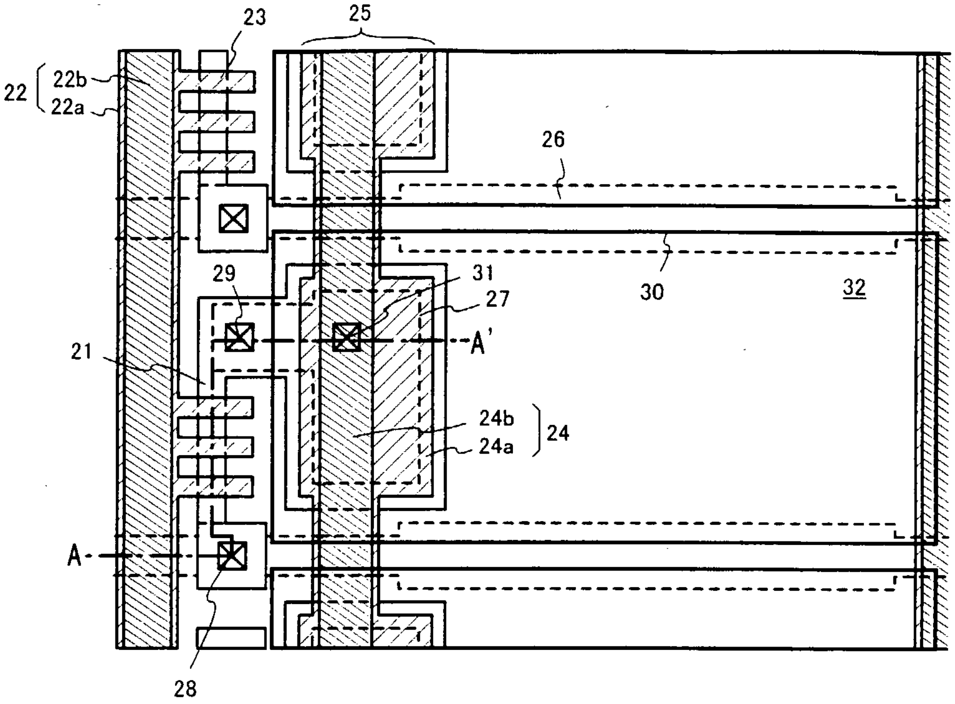


Fig. 10A

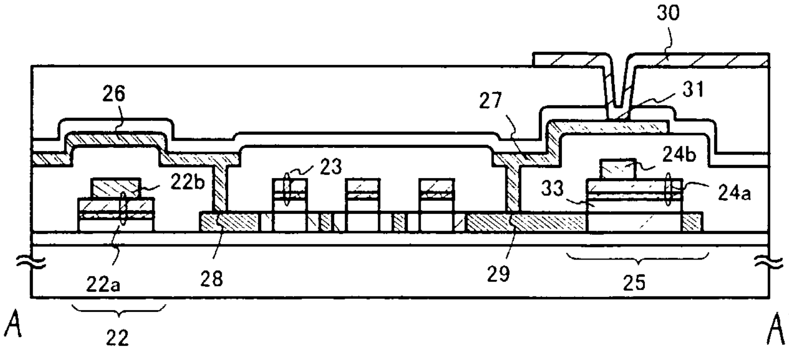
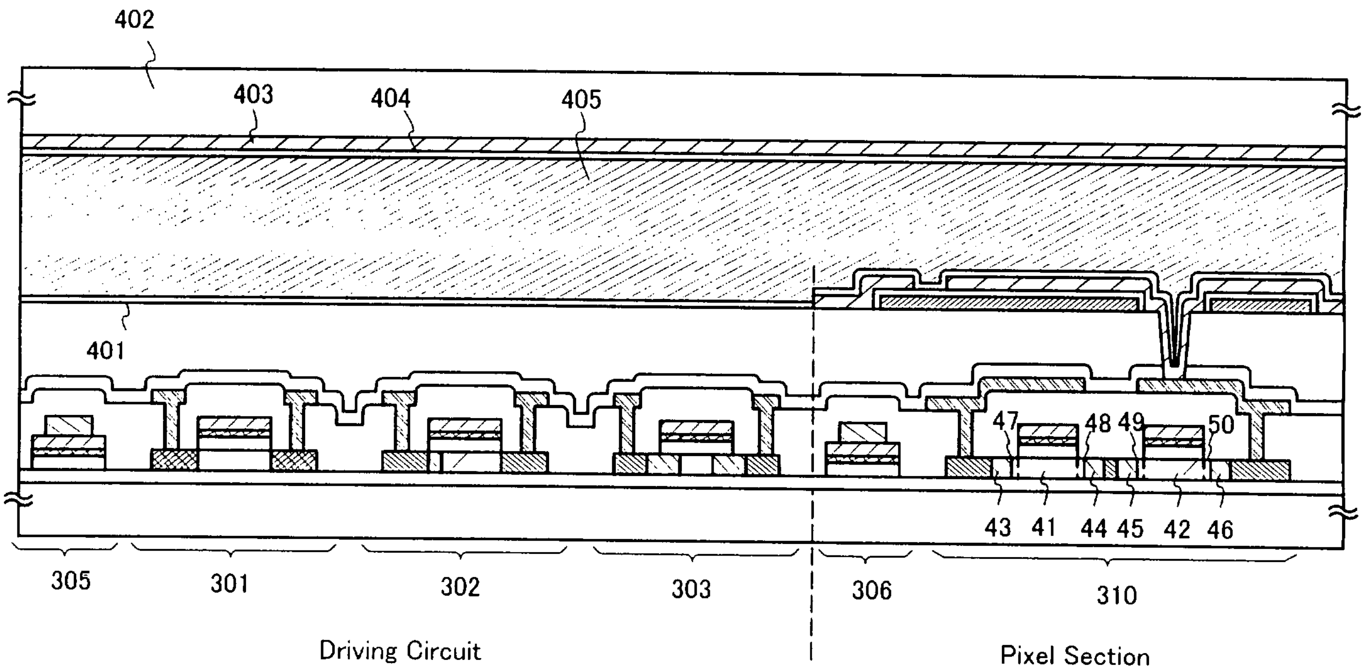


Fig. 10B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306
310
Driving Circuit
Pixel Section

Fig. 11

Fig. 12A

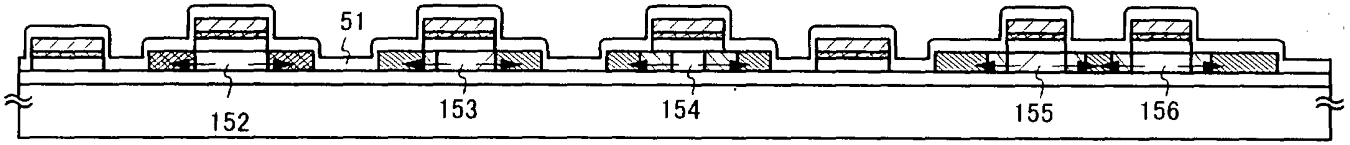


Fig. 12B

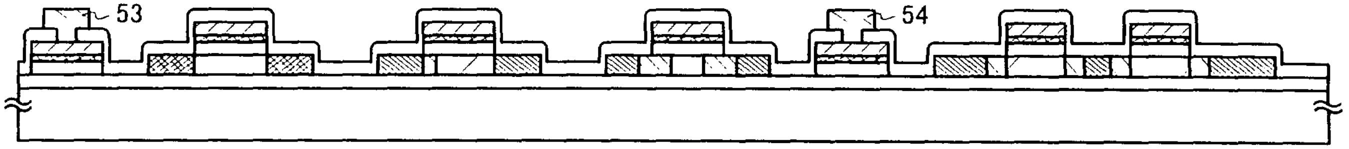
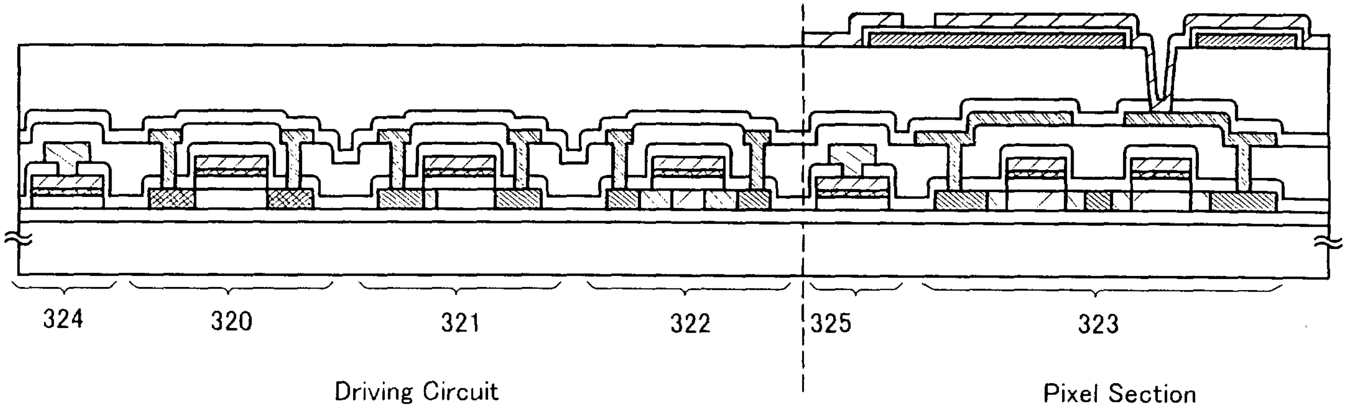


Fig. 12C



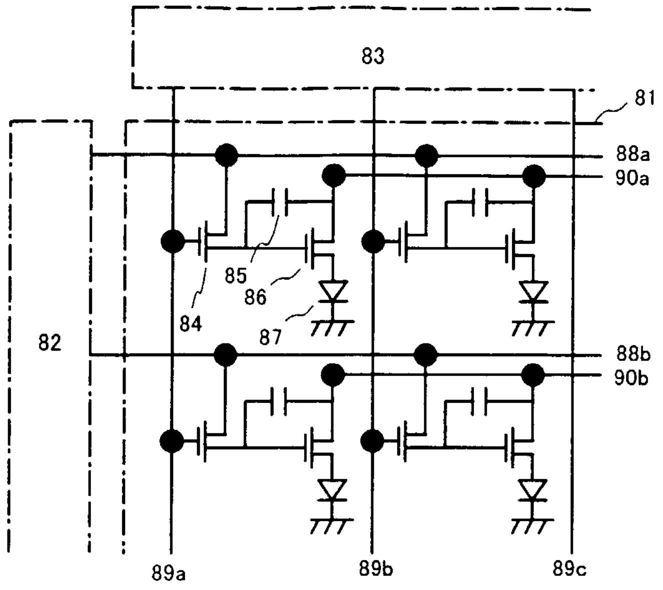


Fig. 13

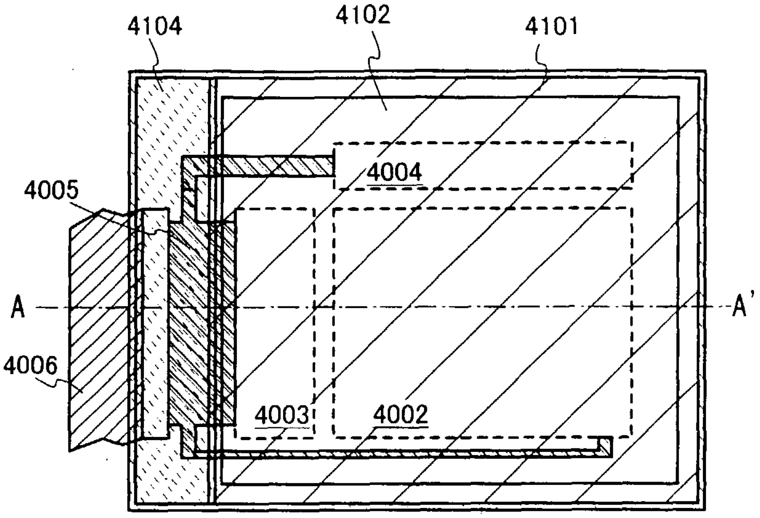


Fig. 14A

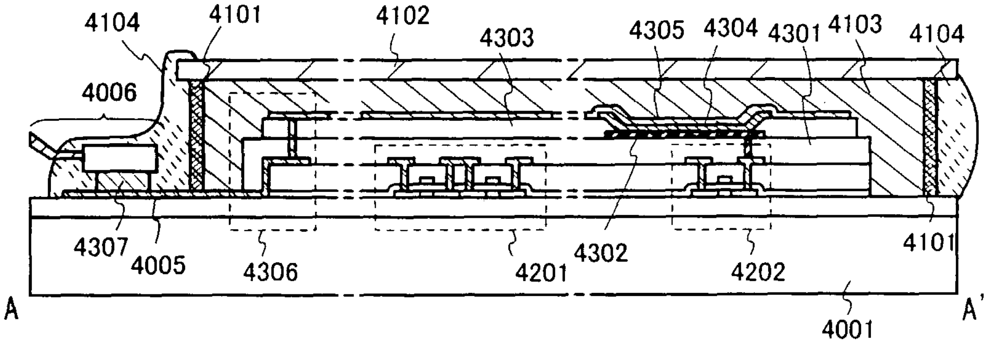
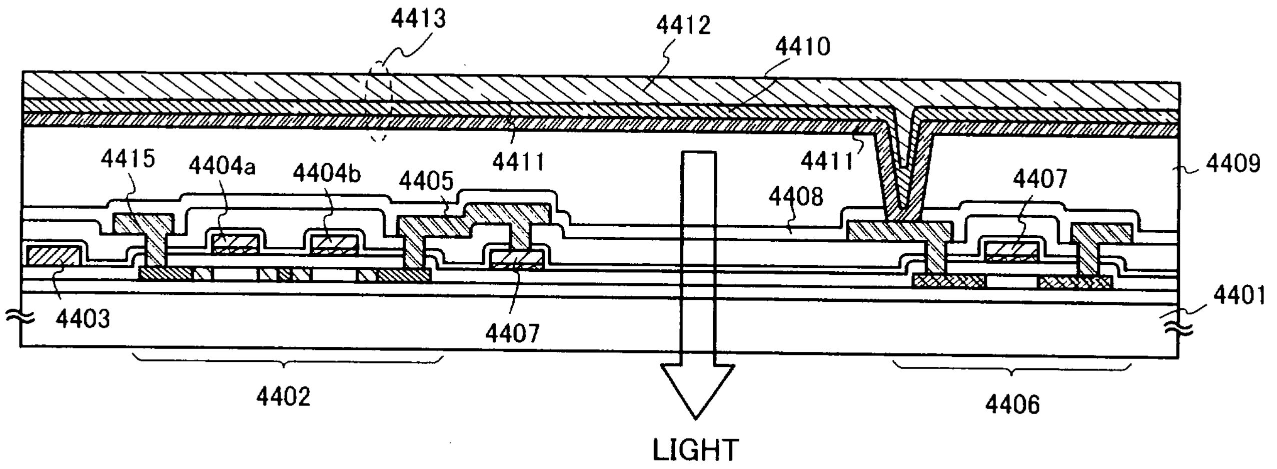


Fig. 14B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4410
4415
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4404b
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4411
4411
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4407
4409
4403
4407
4401
4402
4406
LIGHT

Fig. 15

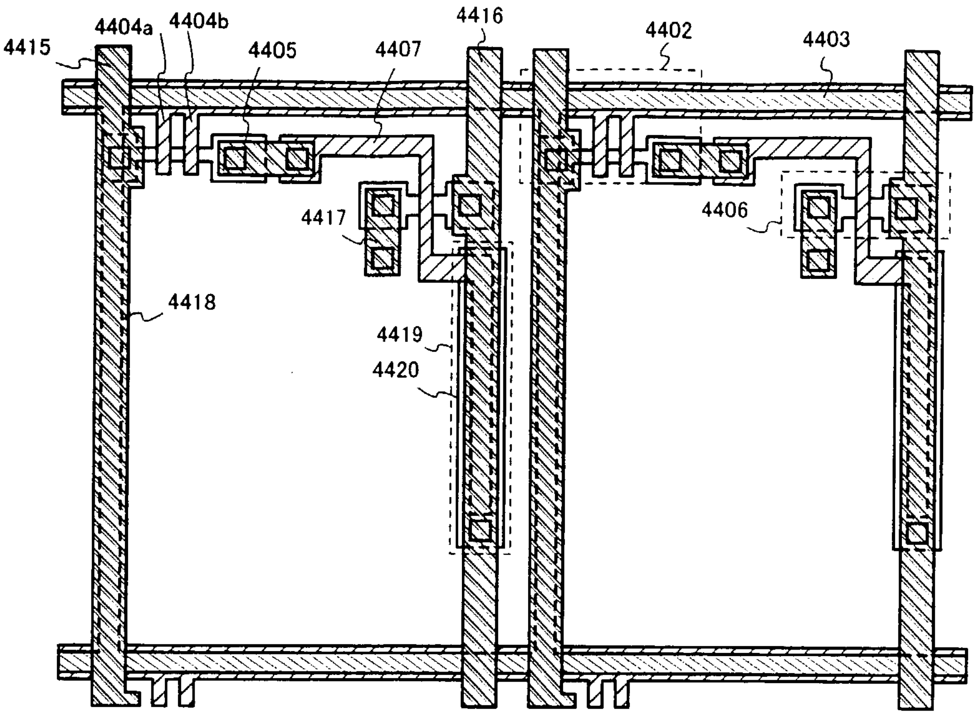


Fig. 16A

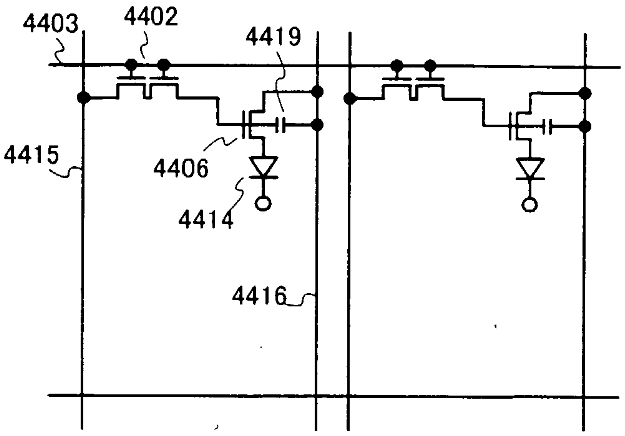
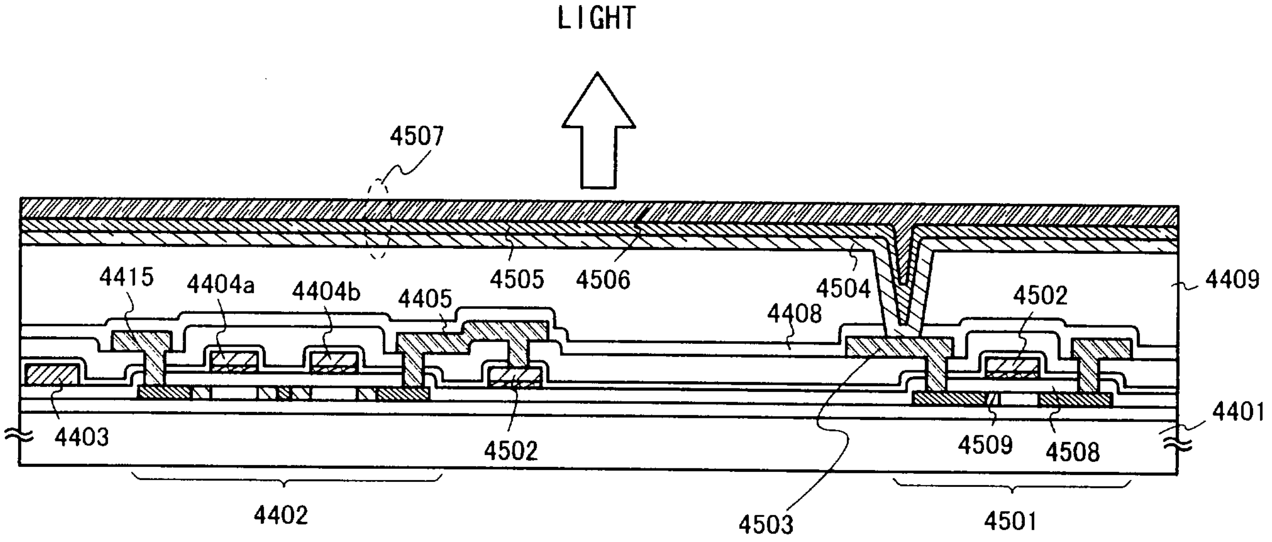


Fig. 16B


LIGHT
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4404b
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4503
4501

Fig. 17

Fig. 18A

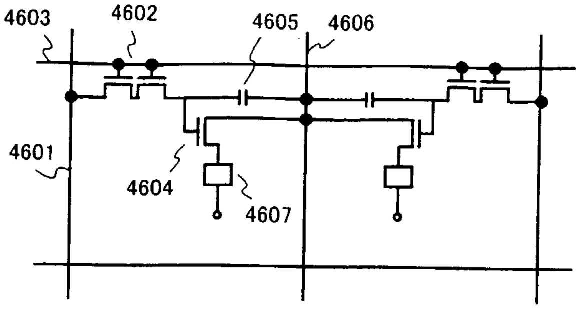


Fig. 18B

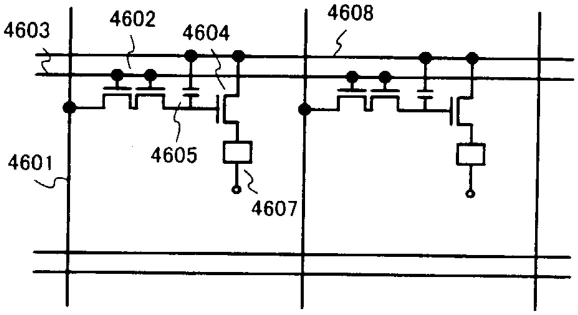
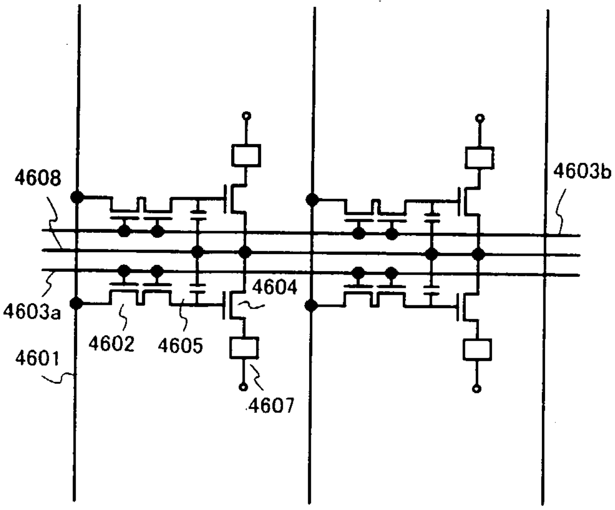


Fig. 18C



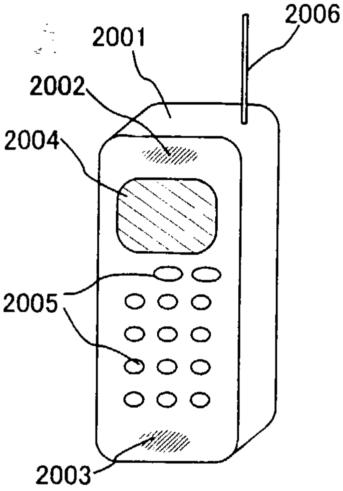


Fig. 19A

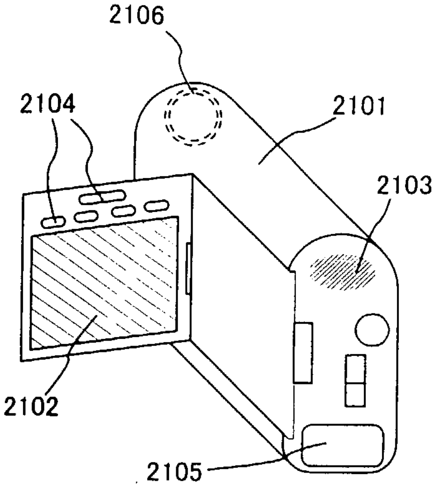


Fig. 19B

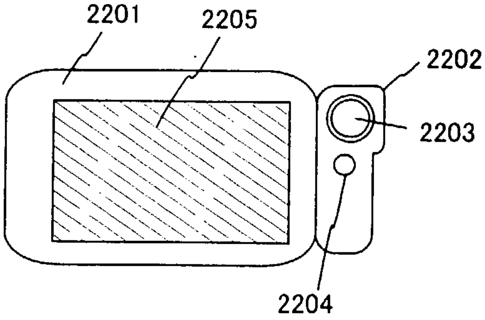


Fig. 19C

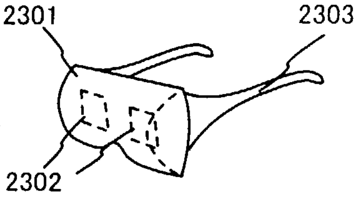


Fig. 19D

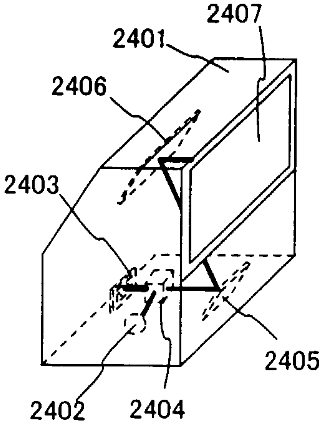


Fig. 19E

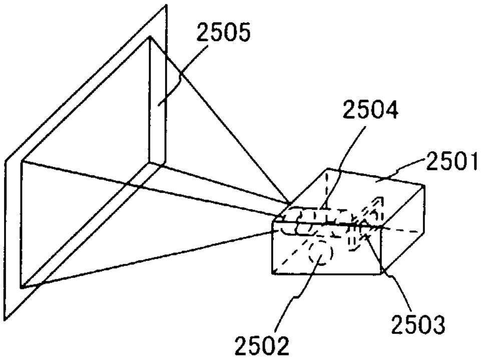


Fig. 19F

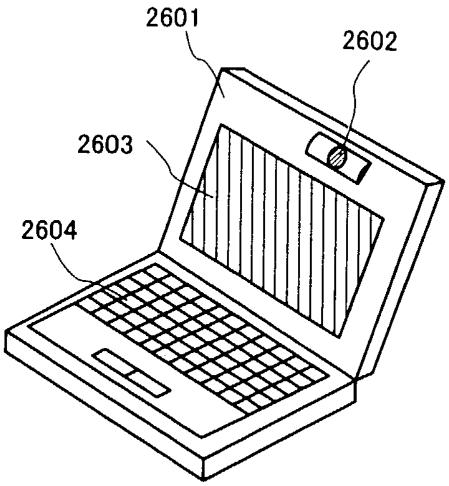


Fig. 20A

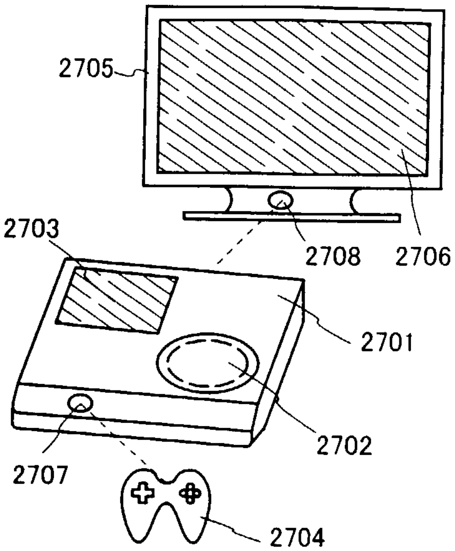


Fig. 20B

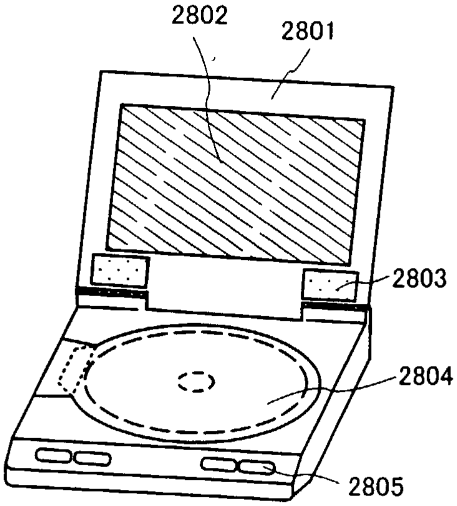


Fig. 20C

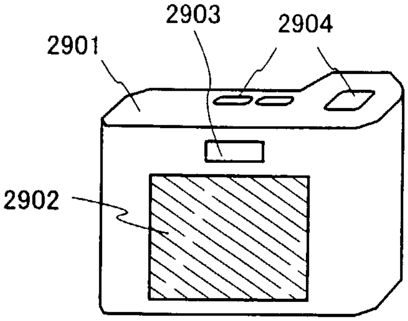


Fig. 20D

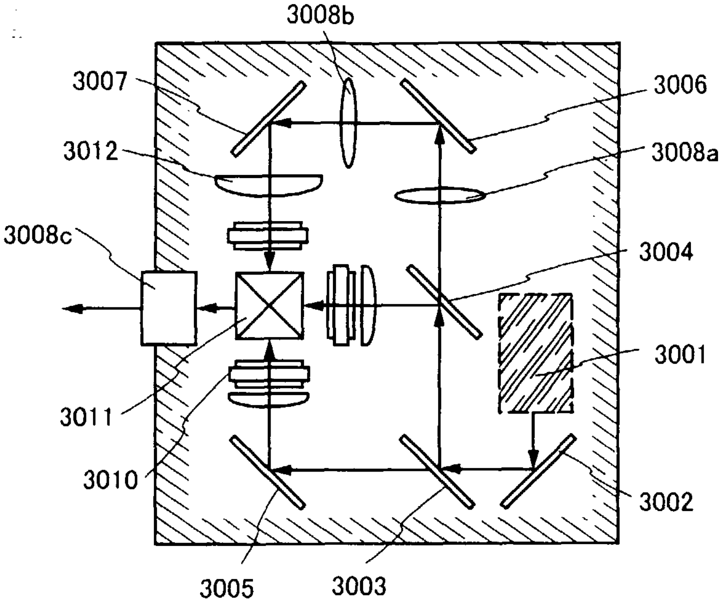


Fig. 21A

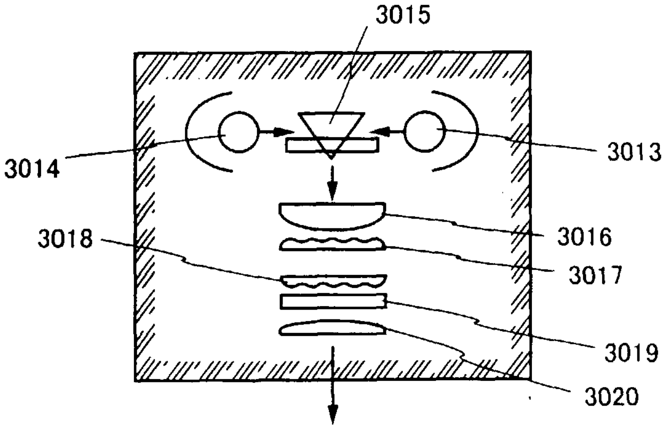


Fig. 21B

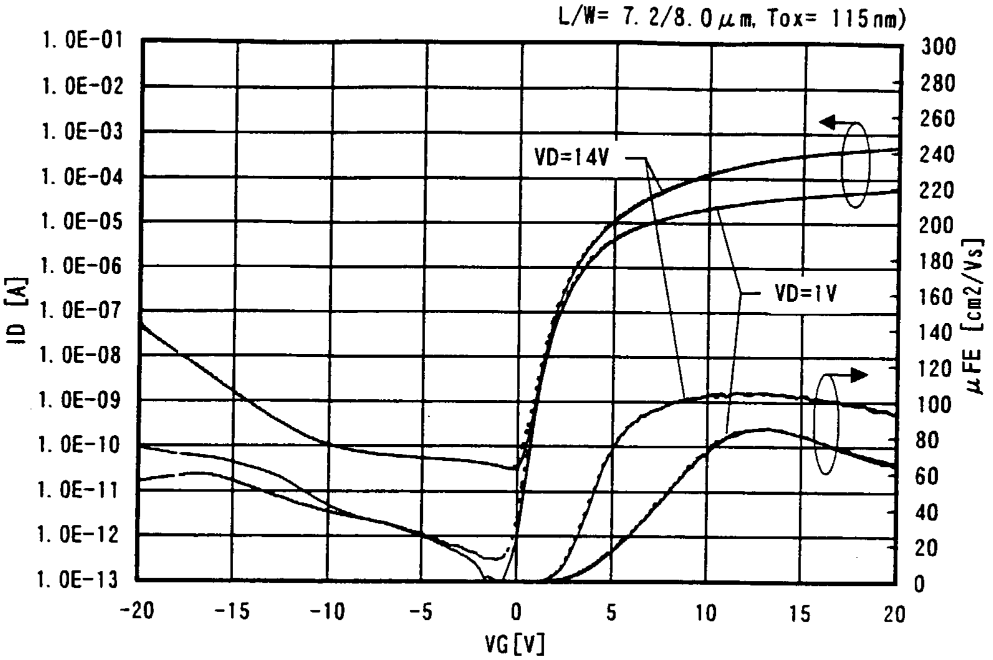

L/W= 7.2/8.0 μm, Tox= 115nm)
1.0E-01
1.0E-02
1.0E-03
1.0E-04
1.0E-05
1.0E-06
1.0E-07
1.0E-08
1.0E-09
1.0E-10
1.0E-11
1.0E-12
1.0E-13
ID [A]
300
280
260
240
220
200
180
160
140
120
100
80
60
40
20
0
μFE [cm2/Vs]
VD=14V
VD=1V
-20
-15
-10
-5
0
5
10
15
20
VG[V]

Fig. 22

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Continuing Data as Claimed by Applicant

Foreign Applications

JAPAN 11-191097 07/06/1999

If Required, Foreign Filing License Granted 09/08/2000

Title

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Preliminary Class

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Name Nathan Wollack
(typed or printed)
Signature Nathan Wollack

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a semiconductor device having a circuit comprising thin film transistors (hereinafter referred to as "TFT") over a substrate having an insulating surface, and a fabrication method thereof. Specifically, the present invention provides a technology that will be appropriately used for an electro-optical device typified by a liquid crystal display device having a pixel section and a driving circuit disposed in the periphery the pixel section, and for an electronic appliance incorporating such an electro-optical device. Note that the term "semiconductor device" used herein represents those devices which operate by utilizing semiconductor characteristics, and embraces within its scope the electro-optical devices as well as the electronic appliances incorporating the electro-optical device that are described above.

2. Description of the Related Art

A technology that uses TFTs for constituting switching devices and active electric circuits has been developed in the electro-optical device typified by an active matrix liquid crystal display device. In the TFTs, a semiconductor film is grown over a substrate of a glass or the like by a vapor phase growth method, and the semiconductor film is used as an active layer. Silicon or a material consisting of silicon as the principal component such as silicon-germanium has been used appropriately for the semiconductor film. An amorphous silicon film and a crystalline silicon film represented by a polycrystalline silicon film can be obtained depending on the deposition method of the silicon semiconductor film.

The TFT using the amorphous silicon film for the active layer cannot essentially acquire field effect mobility of greater than several $cm^2/Vsec$ because of its electro-physical factors resulting from the amorphous structure, and so forth. Therefore, though it can be used as a switching element (pixel TFT) for driving a liquid crystal disposed at each pixel of a pixel section in an active matrix type liquid crystal device, the amorphous silicon film cannot form a driving circuit for effecting image display. For this reason, a technology of packaging a driver IC, etc, by using a TAB (Tape Automated Bonding) system or a COG (Chip on Glass) system has been employed.

On the other hand, the TFT using the crystalline silicon film for the active layer can acquire high field effect mobility and can form various functional circuits over the same glass substrate. The crystalline silicon film makes it possible to fabricate a shift register circuit, a level shifter circuit, a buffer circuit, a sampling circuit, and the like, each comprising a CMOS circuit including n-channel TFTs and p-channel TFTs in the driving circuit besides the pixel TFTs. To achieve the reduction of weight and thickness in the liquid crystal display device on the basis of such a technology, it became clear that the TFT using the crystalline semiconductor film, that can integrally form the driving circuit on the same substrate besides the pixel unit, for the active layer, is suitable.

Though the active layer using the crystalline silicon film is superior from the aspect of performance of the TFT, the fabrication steps become complicated and the number of process steps increases to form the TFT that can cope with various circuits besides the pixel TFTs. The increase of the number of process steps in turn results in the increase of the production cost and lowers also the production yield.

For example, the operating condition of the circuits are not always the same for the pixel TFT and the TFT of the driving circuit, and the characteristics required for each TFT are different. The pixel TFT comprises an n-channel TFT, applies the voltage and drives a liquid crystal as a switching device. Since the liquid crystal is driven by the alternating current, a system called "frame inversion driving" has been used widely. In this method, one of the characteristics required for the pixel TFT is to restrict an OFF current value (a drain current that flows when the TFT is under the OFF operation) to a sufficiently low level to limit power consumption low. On the other hand, a high driving voltage is applied to a buffer circuit of a control circuit so that the withstand voltage must be increased in order that the TFT is not broken even when a high voltage is applied thereto. To improve a current driving capacity, a sufficient ON current value (the drain current that flows when the TFT is under the ON operation) must be secured.

A lightly doped drain (LDD) structure is known as a TFT structure for reducing the OFF current value. This structure disposes an impurity region, to which an impurity element is added in a concentration lower than that of a source or drain region, between a channel formation region and the source or drain region that is formed by adding an impurity element in a high concentration. This impurity region is called the "LDD region". Further, there is known a so-called GOLD (gate-drain overlapped LDD) structure in which a LDD region is disposed so as to overlap a gate electrode by interposing a gate insulating film, as a means for preventing degradation of ON current value due to hot carriers. It is known that the high electric field in the proximity of the drain is released and the hot carrier injection is prevented by applying such a structure, and it is effective in preventing degrading phenomenon.

As described above, the required characteristics are not always the same between the pixel TFT and the TFT used for the driving circuit such as the shift register circuit or the buffer circuit. For example, a large reverse bias (a negative voltage in the case of the n-channel TFT) is applied to the gate of the pixel TFT, but the TFT of the driving circuit does not basically operate under the reverse bias state. As to the operation speed, too, the operation speed of the pixel TFT may not be higher than 1/100 of that of the TFT of the control circuit. Further, though GOLD structure has a high effect of preventing degradation of ON current value, on the other hand there was a problem that OFF current value becomes large as compared to ordinary LDD structure. Accordingly it was not a preferable structure for applying to the pixel TFT. On the contrary, ordinary LDD structure had a high effect for preventing OFF current value but it did not have effect of releasing electric field in the proximity of the drain and preventing degradation by hot carrier injection. As described above it was not always preferable to fabricate all the TFTs in a same structure, in a semiconductor device having a plurality of integrated circuits that have different operating condition as an active matrix liquid crystal display device. Such problems became apparent specifically in crystalline silicon TFTs as the characteristics enhanced and the performance required for an active matrix liquid crystal display device increased.

To stabilize the operation of these circuits fabricated by using the n- and p-channel TFTs, the threshold voltage and sub-threshold constant (S value) of the TFTs must be kept within predetermined ranges. For this purpose, the TFT must be examined from the aspects of both structure and material.

The present invention contemplates to provide a technology that solves these problems. In electro-optical devices and semiconductor devices typified by an active matrix liquid crystal device fabricated by using TFTs, the present invention is directed to improve the operation characteristics and reliability of the semiconductor devices and at the same time lower the power consumption, by optimizing the structures of the TFTs employed in various circuits in accordance with the functions of the respective circuits, thereby reducing the production cost and improving the production yield by reducing the number of process steps.

To accomplish the reduction of the production cost and the improvement of the production yield by reducing the number of process steps, the number of photo-masks used for the fabrication of the TFT must be reduced. In photolithography, the photo-mask is used for forming a resist pattern over the substrate as the mask in the etching process. Therefore, when one photo-mask is used, additional process steps such as resist removing, washing, drying, etc, are necessary before and after the step that uses the photo-mask in addition to the process steps of the film formation and etching. In the photolithography step, too, complicated process steps such as the application of the resist, pre-baking, exposure, development, post-baking, etc, are necessary.

To solve the problem described above, the present invention provides a semiconductor device having, over the same substrate, pixel TFTs disposed in a pixel section and a driving circuit including p-channel TFTs and n-channel TFTs and disposed round the pixel section, wherein: the p-channel TFT of the driving circuit comprises a channel forming region and a p-type impurity region having a fourth concentration, which forms a source region or a drain region; the n-channel TFT of the driving circuit comprises a channel forming region, an n-type impurity region having a first concentration, which is disposed in contact with the channel forming region and forms an LDD regions that overlap the gate electrode and that do not overlap the gate electrode, and an n-type impurity region of the third concentration, which is disposed outside the n-type impurity region having the first concentration and forms a source region or a drain region; the pixel TFT comprises a channel forming region, an n-type impurity region of the second concentration which is disposed in contact with the channel forming region and forms a LDD region, and an n-type impurity region of the third concentration which is disposed in the outside of the n-type impurity region of the second concentration and forms a source region or a drain region; and a pixel electrode disposed in the pixel section has a light reflecting surface and is formed over an interlayer insulating film made of an organic insulating material, and is connected to the pixel TFT through a hole formed in at least a protective insulating film made of an inorganic insulating material disposed over a gate electrode of said pixel TFT, and the interlayer insulating film formed on the insulating film in close contact therewith.

Another constitution of the present invention provides a semiconductor device having, on the same substrate, pixel TFTs disposed in a pixel section and a driving circuit comprising a p-channel TFT and an n-channel TFT which is disposed in the peripheral of the pixel section, wherein: the p-channel TFT of the driving circuit comprises a channel forming region and a p-type impurity region having a fourth concentration which forms a source region or a drain region; the n-channel TFT of the driving circuit comprises a channel forming region, an n-type impurity region having a first concentration which is disposed in contact with the channel forming region and forms a LDD region that partly overlap a gate electrode, and an n-type impurity region having a third concentration which is disposed outside the n-type impurity region having the first concentration and forms a source region or a drain region; the pixel TFT comprises a channel forming region, an n-type impurity region having the second concentration which is disposed in contact with the channel forming region and forms a LDD region, and an n-type impurity region having the third concentration which is disposed on the outside of the n-type impurity region having the second concentration and forms a source region or a drain region; and a pixel electrode disposed in the pixel section has a light transmitting surface and formed over an interlayer insulating film made of an organic insulating material, and is connected to a conductive metal lead wiring connected to the pixel TFT, through a hole formed at least in a protective insulating film made of an inorganic insulating material and disposed above a gate electrode of said pixel TFT and the interlayer insulating film formed on the insulating film in close contact therewith.

Another constitution of the present invention provides a semiconductor device having a liquid crystal sandwiched between a pair of substrates, wherein, in one of said substrates having a pixel TFT disposed in a pixel section and a driving circuits in which p-channel TFTs and n-channel TFTs are disposed in the periphery of the pixel section: the p-channel TFT of the driving circuit comprises a channel forming region and a p-type impurity region having a fourth concentration which forms a source region or a drain region; the n-channel TFT of said driving circuit comprises a channel forming region, an n-type impurity region having a first concentration which is disposed in contact with the channel forming region and forms a LDD region which partly overlaps a gate electrode, and an n-type impurity region having a third concentration disposed outside said n-type impurity region having the first concentration and forms a source region or a drain region; the pixel TFT comprises a channel forming region, an n-type impurity region having the second concentration which is disposed in contact with the channel forming region and forms a LDD region, and an n-type impurity region having the third concentration which is disposed on the outside of the n-type impurity region having the second concentration and forms a source region or a drain region; a pixel electrode disposed in the pixel section has a light reflecting surface and is formed over an interlayer insulating film made of an organic insulating material, and is connected to the pixel TFT through a hole formed in at least a protective insulating film made of an inorganic insulating material disposed over a gate electrode of said pixel TFT, and the interlayer insulating film formed on the insulating film in close contact therewith; and this one substrate is bonded to the other substrate having a transparent conductive film formed thereon through at least one columnar spacer formed in superposition with the hole.

Another constitution of the present invention provides a semiconductor device having a liquid crystal sandwiched between a pair of substrates, wherein, in one of the substrates comprising pixel TFTs of a pixel section and a driving circuit comprising p-channel TFTs and n-channel TFTs formed in the peripheral of the pixel section: the p-channel TFT of the driving circuit comprises a channel forming region and a p-type impurity region having a fourth concentration which forms a source region or a drain region; the n-channel TFT of the driving circuit comprises a channel forming region, an n-type impurity region having a first concentration, disposed in contact with the channel forming region and forms a LDD region that partly overlap a gate electrode, and an n-type impurity region having a third concentration disposed outside the n-type impurity region having the first concentration and forms a source region or a drain region; the pixel TFT comprises a channel forming region, an n-type impurity region having the second concentration which is disposed in contact with the channel forming region and forms a LDD region, and an n-type impurity region having the third concentration which is disposed on the outside of the n-type impurity region having the second concentration and forms a source region or a drain region; a pixel electrode disposed in the pixel section has a light transmitting property and is formed over an interlayer insulating film made of an organic insulating material and is connected to a conductive metal lead wiring connected to the pixel TFT through a hole formed in at least a protective insulating film made of an inorganic insulating material and disposed over a gate electrode and in the interlayer insulating film formed on the insulating film in close contact therewith; and the substrate is bonded to the other substrate having a transparent conductive film formed thereon, through at least one columnar spacer formed in superposition with the hole.

An offset region may be formed between the channel forming region and the p-type impurity region having the fourth concentration which forms a source region or a drain region in the p-channel TFT of the driving circuit, in the constitutions of the invention described above. Such p-channel TFT can be appropriately used as an analog switch.

Further, in the above aspect of the present invention, the semiconductor device is characterized in that a gate electrode of the pixel TFT of the pixel portion and the gate electrodes of the p-channel TFT and the n-channel TFT in the periphery of the pixel portion is formed of a heat-resistant conductive material, and gate wirings extending from the driver circuit to be connected to the gate electrodes are formed of a low-resistant conductive material. Preferably the heat-resistant conductive material is an element selected from the group consisting of tantalum (Ta), titanium (Ti), molybdenum (Mo), and tungsten (W); or a compound containing the above elements; or a compound of a combination of the above elements; or a nitride containing the above elements; or a silicide containing the above elements.

Still further, in the above aspect of the present invention, the semiconductor device is characterized in that the columnar spacer is formed on the p-channel TFT and the n-channel TFT of the driver circuit, or that the columnar spacer is formed at least covering the source wiring or the drain wiring of the p-channel TFT and the n-channel TFT of the driver circuit.

In order to solve the above problems, according to one aspect of the present invention, there is provided a method of manufacturing a semiconductor device having a pixel TFT formed in a pixel portion and a driver circuit, provided with a p-channel TFT and a n-channel TFT, formed in the periphery of the pixel portion on the same substrate, characterized by comprising the steps of: forming a base film in contact with the substrate; forming a plurality of island semiconductor layers on the base film; forming a first concentration n-type impurity region in a selected region of the island semiconductor layer for forming an LDD region of which a portion overlaps with a gate electrode of the n-channel TFT of the driver circuit; forming a second concentration n-type impurity region in a selected region of the island semiconductor layer for forming an LDD region of the pixel TFT; forming a third concentration n-type impurity region in the selected region of the island semiconductor layer for forming a source region or a drain region of the n-channel TFT of the driver circuit and the pixel TFT; forming a fourth concentration p-type impurity region in a selected region of the island semiconductor layer for forming a source region or a drain region of the p-channel TFT of the driver circuit; forming a protective insulating film made of an inorganic insulating material over a gate electrode of the n-channel TFT of the driver circuit, the pixel TFT, and the p-channel TFT; forming an interlayer insulating film made of an organic insulating material, in contact with the protective insulating film; and forming a pixel electrode having a light reflective surface and connected to the pixel TFT, on the interlayer insulating film.

Further, according to another aspect of the present invention, there is provided a method of manufacturing a semiconductor device having a pixel TFT formed in a pixel portion and a driver circuit, provided with a p-channel TFT and a n-channel TFT, formed in the periphery of the pixel portion on the same substrate, characterized by comprising the steps of: forming a base film over the substrate; forming a plurality of island semiconductor layers over the base film; forming a first concentration n-type impurity region in a selected region of the island-like semiconductor layer for forming an LDD region of which a portion overlaps with a gate electrode of the n-channel TFT of the driver circuit; forming a second concentration n-type impurity region in a selected region of the island semiconductor layer for forming an LDD region of the pixel TFT; forming a third concentration n-type impurity region in the selected region of the island semiconductor layer for forming a source region or a drain region of the n-channel TFT of the driver circuit and the pixel TFT; forming a fourth concentration p-type impurity region in a selected region of the island semiconductor layer for forming a source region or a drain region of the p-channel TFT of the driver circuit; forming a protective insulating film made of an inorganic insulating material over a gate electrode of the n-channel TFT of the driver circuit, the pixel TFT, and the p-channel TFT ; forming an interlayer insulating film made of an organic insulating material in contact with the protective insulating film; forming a conductive metal wiring to be connected to the pixel TFT; and forming a pixel electrode made from a transparent conductive film to be connected to the conductive metal wiring, on the interlayer insulating film.

Further, according to still another aspect of the present invention, there is provided a method of manufacturing a semiconductor device having liquid crystal between a pair of substrates, characterized in that: a pixel TFT formed in a pixel portion and a driver circuit provided with a p-channel TFT and an n-channel TFT formed in the periphery of the pixel portion are formed on one substrate by the steps comprising: forming a base film over the substrate; forming a plurality of island semiconductor layers over the base film; forming a first concentration n-type impurity region in a selected region of the island semiconductor layer for forming an LDD region of which a portion overlaps with a gate electrode of the n-channel TFT of the driver circuit; forming a second concentration n-type impurity region in a selected region of the island semiconductor layer for forming an LDD region of the pixel TFT; forming a third concentration n-type impurity region in the selected region of the island semiconductor layer for forming a source region or a drain region of the n-channel TFT of the driver circuit and the pixel TFT; forming a fourth concentration p-type impurity region in a selected region of the island semiconductor layer for forming a source region or a drain region of the p-channel TFT of the driver circuit; forming a protective insulating film made of an inorganic insulating material over a gate electrode of the n-channel TFT of the driver circuit, the pixel TFT, and the p-channel TFT; forming an interlayer insulating film made of an organic insulating material in contact with the protective insulating film; and forming a pixel electrode having a light reflective surface to be connected to the pixel TFT via an opening provided in the interlayer insulating film and the protective insulating film, on the interlayer insulating film, and the other substrate is formed by at least a step comprising forming a transparent conductive film; and that the method comprises a step of sticking the one substrate and the other substrate together via at least one of the column-shape spacers formed overlapping the opening.

Further, according to yet another aspect of the present invention, there is provided a method of manufacturing a semiconductor device having liquid crystal between a pair of substrates, characterized in that: a pixel TFT formed in a pixel portion and a driver circuit provided with a p-channel TFT and an n-channel TFT formed in the periphery of the pixel portion are formed on one substrate by the steps comprising: forming a base film over the substrate; forming a plurality of island semiconductor layers over the base film; forming a first concentration n-type impurity region in a selected region of the island semiconductor layer for forming an LDD region of which a portion overlaps with a gate electrode of the n-channel TFT of the driver circuit; forming a second concentration n-type impurity region in a selected region of the island semiconductor layer for forming an LDD region of the pixel TFT; forming a third concentration n-type impurity region in the selected region of the island semiconductor layer for forming a source region or a drain region of the n-channel TFT of the driver circuit and the pixel TFT; forming a fourth concentration p-type impurity region in a selected region of the island-like semiconductor layer for forming a source region or a drain region of the p-channel TFT of the driver circuit; forming a protective insulating film made of an inorganic insulating material over a gate electrode of the n-channel TFT of the driver circuit, the pixel TFT, and the p-channel TFT; forming an interlayer insulating film made of an organic insulating material in contact with the protection insulating film; a step of forming a conductive metal wiring to be connected to the pixel TFT via an opening provided in the interlayer insulating film and the protection insulating film; and forming a pixel electrode, on the interlayer insulating film, made from a transparent conductive film to be connected to the conductive metal wiring, and the other substrate is formed by at least a step comprising forming a transparent conductive film; and that the method comprises a step of sticking the one substrate and the other substrate together via at least one of the column-shape spacers formed overlapping the opening.

In the above method of manufacturing a semiconductor device, it is further possible to perform the step of forming a fourth concentration p-type impurity region in a selected region of the island semiconductor layer which forms a source region or a drain region of the p-channel TFT, after the step of forming the protective insulating film made of an inorganic insulating material over the gate electrode of a p-channel TFT of the driver circuit, to thereby form an off-set region between the channel forming region of the p-channel TFT and the fourth concentration p-type impurity region which forms a source region or a drain region.

In the above method of manufacturing a semiconductor device, it is characterized by further comprising the steps of: forming a gate electrode of the pixel TFT and the p-channel TFT and the n-channel TFT in the periphery of the pixel portion from a heat-resistant conductive material; and forming a gate wiring from a low-resistant conductive material, extending from the driver circuit to be connected to the gate electrode. Preferably the heat-resistant conductive material is formed from an element selected from the group consisting of tantalum (Ta), titanium (Ti), molybdenum (Mo), and tungsten (W); or a compound containing the above elements; or a compound of a combination of the above elements; or a nitride compound containing the above elements; or a silicide containing the above elements.

Still further, in the above method of manufacturing a semiconductor device, it is characterized in that the columnar spacer is also formed on the p-channel TFT and the n-channel TFT of the driver circuit, and that the column-shape spacer is formed at least covering the source wiring or the drain wiring of the p-channel TFT and the n-channel TFT of the driver circuit

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A to 1E are cross-sectional views showing manufacturing steps of a pixel TFT and TFTs of a driving circuit;

Fig. 2A to 2D are cross-sectional views showing manufacturing steps of a pixel TFT and TFTs of a driving circuit;

Fig. 3A to 3C are cross-sectional views showing manufacturing steps of a pixel TFT and TFTs of a driving circuit;

Fig. 4A to 4 C are are cross-sectional views showing manufacturing steps of a pixel TFT and TFTs of a driving circuit;

Fig. 5A to 5C are cross-sectional views showing manufacturing steps of a pixel TFT and TFTs of a driving circuit;

Fig. 6A and 6B are a top views showing the construction of the TFT of the driving circuit and the pixel TFT;

Fig. 7A and 7B are cross-sectional views showing manufacturing steps of a pixel TFT and TFTs of a driving circuit;

Fig. 8A to 8C are cross-sectional views showing manufacturing steps of a pixel TFT and TFTs of a driving circuit;

Fig. 9 is a cross-sectional view showing a manufacturing step of a pixel TFT and TFTs of a driving circuit;

Fig. 10A and 10B are cross-sectional views showing manufacturing steps of a pixel TFT and TFTs of a driving circuit;

Fig. 11A and 11B are cross-sectional views showing manufacturing steps of an active matrix liquid crystal display device;

Fig 12 is a cross-sectional view showing manufacturing step of an active matrix liquid crystal display device;

Fig. 13 is an explanatory view used for explaining the shape of a columnar spacer;

Fig. 14 is a top view useful for explaining the arrangement of input/output terminals, wires, circuit arrangement, spacers and sealants of a liquid crystal display device;

Fig. 15 is a perspective view showing the construction of the liquid crystal display device;

Fig. 16 is a top view showing the pixel of the pixel section;

Fig. 17 is a block diagram useful for explaining the circuit construction of the liquid crystal display device;

Fig. 18 is an explanatory view of the connection structure between a flexible printed circuit board and external input/output terminals;

Fig. 19 is a cross-sectional view showing a manufacturing step of an active matrix type liquid crystal display device;

Fig. 20 is an explanatory view of the connection structure between the flexible printed board and the external input/output terminals;

Fig. 21A and 21B is a schematic view showing an example of semiconductor devices;

Fig. 22A to 22F are diagrams showing an example of the semiconductor devices; and

Fig. 23A to 23D are diagrams showing an example of the projection type liquid crystal display devices.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, preferred embodiments of the present invention will be explained in detail.

[Embodiment 1]

An embodiment of the present invention will be explained with reference to Figs. 1A to 3C. In this embodiment, a method of forming simultaneously pixel TFTs and storage capacitors of a pixel section and TFTs of a driving circuit disposed in the periphery of the display region will be explained step-wise in detail.

In Fig. 1A, as well as barium borosilicate glass or aluminoborosilicate glass as typified by Corning #7059 glass and #1737 glass, plastic substrates which do not have optical anisotropy such as polyethylene terephthalate (PET), polyethylene naphthalate (PEN), polyethersulfone (PES), etc, can be used as the substrate 101. When the glass substrate is used, the substrate may be heat-treated in advance at a temperature lower by about 10 to 20°C than a glass strain point. A base film 102 of a silicon oxide film, a silicon nitride film or a silicon oxynitride film, etc. is formed on the surface of the substrate 101, on which TFT is to be formed, in order to prevent the diffusion of impurities from the substrate 101. For example, the silicon oxynitride film 102a is formed from SiH_4, NH_3 and N_2O to a thickness of 10 to 200 nm (preferably, 50 to 100 nm) by plasma CVD, and a hydrogenated silicon oxynitride film 102b is similarly formed from SiH_4 and N_2O to a thickness of 50 to 200 nm (preferably, 100 to 150 nm) in lamination.

The silicon oxynitride film is formed by using the conventional parallel plate type plasma-enhanced CVD. The silicon oxynitride film 102a is formed by introducing SiH_4 at 10 sccm, NH_3 at 100 sccm and N_2O at 20 sccm into a reaction chamber under the condition of a substrate temperature of 325°C, a reaction pressure of 40 Pa, a discharge power density of 0.41 W/cm^2 and a discharge frequency of 60 MHz. On the other hand, the silicon oxynitride film 102b is formed by introducing SiH_4 at 5 sccm, N_2O at 120 sccm and H_2 at 125 sccm into a reaction chamber under the condition of a substrate temperature of 400°C, a reaction pressure of 20 Pa, a discharge power density of 0.41 W/cm^2 and a discharge frequency of 60 MHz. These films can be formed by only changing the substrate temperature and by switching the reactive gases.

The silicon oxynitride film 102a thus formed has a density of $9.28 \times 10^{22}/cm^3$, has an etching rate of about 63 nm/min in a mixed solution ("LAL500", a product of Stella Chemifa Co.) containing 7.13% of ammonium hydrogenfluoride (NH_4HF_2) and

15.4% of ammonium fluoride at 20°C, and is a compact and hard film. When such a film is used for the base film, the diffusion of alkali metal elements from the glass substrate into the semiconductor layers formed thereon can be effectively prevented.

Next, a semiconductor layer 103a having an amorphous structure is formed to a thickness of 25 to 80 nm (preferably, 30 to 60 nm) by a known method such as plasma CVD or sputtering. For example, the amorphous silicon film is formed to a thickness of 55 nm by plasma CVD. Semiconductor films having such an amorphous structure include an amorphous semiconductor film and a micro-crystalline semiconductor film, and a compound semiconductor film having an amorphous structure such as an amorphous silicon-germanium film may also be used. It is possible to continuously form the base film 102 and amorphous semiconductor layer 103a. For example, after the silicon oxynitride film 102a and the hydrogenated silicon oxynitride film 102b are formed continuously by plasma CVD as described above, the film formation can be carried out continuously by switching the reactive gases from SiH_4, N_2O and H_2 to SiH_4 and H_2 , or SiH_4 alone, without exposing them once to the atmosphere of the open air. As a result, the contamination of the surface of the hydrogenated silicon oxynitride film 102b can be prevented, and variance of the characteristics of the TFT to be fabricated and fluctuation of the threshold voltage can be reduced.

The crystallization step is then carried out to form a crystalline semiconductor layer 103b from the amorphous semiconductor layer 103a. A laser annealing method, a thermal annealing method (solid phase growth method) or a rapid thermal annealing (RTA) method can be used for this method. It is preferable to employ the laser annealing method when the glass substrate or the plastic substrate having a low heat resistance as described above is used. The RTA method uses an IR lamp, a halogen lamp, a metal halide lamp or a xenon lamp as the light source. Alternatively, the crystalline semiconductor layer 103b can be formed by the crystallization method using a catalytic element in accordance with the technology disclosed in Japanese Patent Application Laid-Open No. 7-130652. In the crystallization step, hydrogen contained in the amorphous semiconductor layer is first discharged preferably. It is good to perform the crystallization step after heat-treatment is conducted at 400 to 500°C for about 1 hour to lower the hydrogen content to 5 atom% or below, because roughness of the film surface can be prevented advantageously.

When the crystallization step is conducted by the laser annealing method, a pulse oscillation type or continuous light emission type excimer laser, or an argon laser is used as the light source. When the pulse oscillation type excimer laser is used, the laser beam is processed to a linear shape and laser annealing is then conducted. The laser annealing condition can be selected appropriately by the operator. For example, the laser pulse oscillation is 30 Hz and the laser energy density is 100 to 500 mJ/cm^2 (typically, 300 to 400 mJ/cm^2). The linear beams are irradiated to the entire surface of the substrate, and the overlap ratio of the linear beams at this time is 80 to 98%. In this way, the crystalline semiconductor layer 103b can be obtained as shown in Fig. 1B.

A resist pattern is formed on the crystalline semiconductor layer 103b by photolithography that uses a photo-mask 1 (PM1). The crystalline semiconductor layer is divided into an island shape by dry etching, forming thereby island semiconductor layers 104 to 108. A mixed gas of CF_4 and O_2 is used for dry etching. A mask layer 194 is then formed from a silicon oxide film having 50 to 100 nm thickness by plasma-enhanced CVD or sputtering.

An impurity for imparting the p-type may be applied in a concentration of about 1 x 10^{16} to 5 x 10^{17} atoms/cm^3 to the entire surface of the island semiconductor layers of this state to control the threshold voltage (Vth) of the TFTs. The elements of the Group XIII of the periodic table such as boron (B), aluminum (Al) or gallium (Ga) are known as the impurity elements for imparting p-type to the semiconductor. Ion implantation or ion doping is known as the method of doping these elements, but ion doping is suitable for processing a substrate having a large area. This ion doping method uses diborane (B_2H_6) as a source gas and adds boron (B). Addition of such an impurity element is not always necessary and may be omitted however, this is the method that can be used appropriately for keeping the threshold voltage of specifically the n-channel TFT, within a predetermined range.

In order to form a LDD region of the n-channel TFT of the driver circuit, an impurity element that imparts n-type is selectively doped into island semiconductor layers 105 and 107. For this purpose, resist masks 195a to 195e are formed by utilizing a photo mask 2 (PM2). It is appropriate to use phosphorous (P) or arsenic (As) as the impurity element that imparts n type. Ion doping using phosphine (PH_3) is applied here for doping phosphorous (P). The phosphorous (P) concentration in the formed first concentration n-type impurity regions 196 and 197 is in the range of 2×10^{16} to 5×10^{19} atoms/cm^3. Note that throughout the present specification, the concentration of the impurity element that imparts n-type contained in the impurity regions 196 and 197 formed here is indicated by (n^-). In addition, an impurity region 198, a semiconductor layer for forming a storage capacitor of the pixel portion, is also doped with phosphorous (P) at the same concentration. (See Fig. 1D)

The step of activating the doped impurity element is performed next. Activation can be performed by methods such as laser activation or heat treatment performed in a nitrogen atmosphere at 500°C to 600°C for 1 to 4 hours, or both methods may be used together. For the case of employing the laser activation method, the KrF excimer laser light (wavelength of 248 nm) is used to form a linear shape beam with the oscillating frequency set between 5 and 50 Hz, the energy density set between 100 and 500 mJ/cm^2 to scan at an overlapping ratio of between 80% and 98% to thereby treat the entire surface of the substrate on which the island-like semiconductor layer is formed. Note that there are no limitations placed on the irradiation conditions of the laser light, appropriate irradiation conditions may be determined by an operator. The mask layer 194 is removed by etching with a solution such as fluorine.

A gate insulating film 109 is formed from an insulating film containing silicon at a film thickness of between 40 and 150 nm by plasma CVD or sputtering. For example, it is appropriate to form the gate insulating film at a thickness of 120 nm from a silicon oxide nitride film. In addition, a silicon oxide nitride film made from SiH_4 and N_2O, both doped with O_2, is a favorable material for the application here because the fixed electric charge density has been reduced. The gate insulating film, of course, is not limited to such silicon oxide nitride film. A single layer or a laminated layer of other insulating films containing silicon may be used. (See Fig. 1E)

As shown in Fig. 1E, a heat-resistant conductive layer, for forming a gate electrode on the gate insulating film 109, is formed. The heat-resistant conductive layer may be formed as a single layer, or if necessary, it may have a laminated structure formed of a plurality of layers, such as 2 or 3 layers. Using such heat-resistant conductive materials, a lamination structure of, for example, a conductive layer (A) 110 formed from a conductive nitride metallic film and a conductive layer (B) 111 formed from a metallic film, is appropriate. The conductive layer (B) 111 may be formed from an element selected from the group consisting of tantalum (Ta), titanium (Ti), molybdenum (Mo), and tungsten (W); or an alloy having the above elements as its principal constituent; or an alloy film formed from a combination of the above elements (typically, an Mo-W alloy film and an Mo-Ta alloy film). The conductive layer (A) 110 is formed of elements such as tantalum nitride (TaN), tungsten nitride (WN), titanium nitride (TiN) film, and molybdenum nitride (MoN). Additionally, tungsten silicide, titanium silicide, and molybdenum silicide are also applicable for forming the conductive layer (A) 110. For the purpose of lowering the resistance of the conductive layer (B) 111, it is favorable to reduce the concentration of the impurity element contained therein, particularly, in regards to the oxygen concentration, better at 30 ppm or less. For example, a resistivity of 20 μΩcm or less can be realized provided that the oxygen concentration of tungsten (W) is 30 ppm or less.

It is appropriate to form the conductive layer (A) 110 at a thickness of between 10 and 50 nm (preferably between 20 and 30 nm), and the conductive layer (B) 111 at a thickness of between 200 and 400 nm (preferably between 250 and 350 nm). For the case of using W as the gate electrode, a 50 nm thick conductive layer (A) 111 formed of tungsten nitride (WN) and a 250 nm thick conductive layer (B) 110 formed of W are formed by sputtering with W as the target and introducing argon (Ar) gas and nitrogen (N_2) gas. As another method, the W film may also be formed by thermal CVD using tungsten fluoride 6 (WF_6). In any case, it is necessary to lower the resistance of the W film for use as the gate electrode, the desired resistivity of the W film is 20 μΩcm or less. Growing larger crystal grains in the W film can lower the resistivity. However, crystallization is impeded when many impurity elements exist in the W, such as oxygen, then the W film become high resistance. Because of this, a W target having 99.9999% degree of purity is utilized for the case of sputtering, and furthermore, sufficient consideration must be made to prevent an impurity from the vapor from mixing into the films during film deposition. Accordingly, a resistivity of between 9 and 20 μΩcm can be realized.

On the contrary, for the case of using a TaN film as the conductive layer (A)

110 and a Ta film as the conductive layer (B) 111, similarly, both can be formed by sputtering. The TaN film, with Ta as the target, is formed by utilizing a gaseous mixture of Ar and nitrogen as the sputtering gas while only Ar is utilized as the sputtering gas for the Ta film. Further, the internal stress of the films to be formed may be relaxed by adding a moderate amount of Xe or Kr into the sputtering gas of these films to prevent the films from peeling. The resistivity of an α phase Ta film is about 20 μΩcm, and therefore it can be used as the gate electrode. Contrary to this, the resistivity of a β phase Ta film is about 180 μΩcm, and therefore it is unsuitable to be used as the gate electrode. Since the TaN film has a crystal structure close to the α phase, the α phase Ta film can be readily obtained by forming the Ta film on the TaN film. Although not shown in the figure, note that it is effective to form a phosphorous (P) doped silicon film at a thickness of between 2 and 20 nm under the conductive layer (A) 110. Due to this, the adhesion of the conductive film formed on the silicon film can be improved and averted from being oxidized, as well as preventing the very small amount of alkali metallic element contained in the conductive layer (A) 110 or the conductive layer (B) 111 from diffusing into the gate insulating film 109. Nevertheless, it is preferred that the conductive layer (B) 111 be formed within the resistivity range of between 10 and 50 μΩcm.

With employment of the photomask 3 (PM3), resist masks 112 through 117 are formed next by utilizing the photolithography technique. Then the conductive layer (A) 110 and the conductive layer (B) 111 are etched together to form gate electrodes 118 through 122 and a condenser wiring 123. The gate electrodes 118 through 122 and the condenser wiring 123 are integrally formed with layers 118a to 122a, formed of the conductive layer (A) 110, and with layers 118b to 122b, formed of the conductive layer (B) 111. (See Fig. 2A)

A method of etching the conductive layer (A) and the conductive layer (B) may be appropriately selected by the operator. As stated above, if the conductive layers are formed of a material having W as its principal constituent, it is desired that the dry etching method using high-density plasma be applied for implementing a speedy and precise etching. As one means of attaining high-density plasma, it is appropriate to employ the ICP (Inductively Coupled Plasma) etching device. In the etching method of W employing the ICP etching device, two types of gas, CF_4 and Cl_2 are introduced into the reaction chamber as etching gas, pressure is set between 0.5 and 1.5 Pa (preferably 1 Pa), and a high frequency electric power (13.56 MHz) of between 200 and 1000 W is applied to the inductively coupled portion. At this point, a 20W high frequency electric power is applied to the stage with a substrate disposed therein. Due to charging a negative electric potential by self-bias, a positive ion is accelerated to thereby perform anisotropy etching. With employment of the ICP etching device, an etching speed of between 2 and 5 nm/sec can be achieved even in a hard metallic film such as W. In order to perform etching without leaving any residues, the etching time may be increased by about 10% to 20% to perform over-etching. However, attention must be paid to the selective ratio of etching with the base layer at this point. For example, the selective ratios of the oxidized silicon nitride film (the gate insulating film 109) to the W film is between 2.5 and 3. Due to such over-etching treatment, the exposed surface of the oxidized silicon nitride film is etched about 20 to 50 nm, substantially making the film become thinner.

The step of doping an impurity element that imparts n type (n^- doping step) is performed next to form an LDD region in the n-channel TFT of the pixel TFT. Using the gate electrodes 118 through 122 as a mask, the impurity element that imparts n type is doped by ion doping in a self-aligning manner. The concentration of phosphorous (P), as the impurity element imparting n type, is doped at a concentration range from 1 x 10^{16} to 5 x 10^{19} atoms/cm^3. Second concentration n-type impurity regions 124 to 129 are thus formed in the island-like semiconductor layer as shown in Fig. 2B.

The step of forming a third concentration n-type impurity region (n^+ doping step) to function as a source region or a drain region in the n-channel TFT is performed next. First, resist masks 130 through 134 are formed by using the photomask 4 (PM4), then an impurity element that imparts n type is doped to thereby form the third concentration n-type impurity regions 135 through 140. Phosphorous (P) is used as the impurity element imparting n type. Ion doping using phosphine (PH_3) is performed so that the concentration of phosphorous will be in the concentration range from 1 x 10^{20} to 1 x 10^{21} atoms/cm^3. (See Fig. 2C)

Next, fourth concentration p-type impurity regions 144 and 145 are formed as a source region or a drain region in the island-like semiconductor layers 104 and 106 that form the p-channel TFT. Using the gate electrodes 118 and 120 as masks, an impurity element that imparts p type is doped to thereby form the fourth concentration p-type impurity region in a self-aligning manner. At this point, the island-like semiconductor films 105,107,and 108,which form the n-channel TFT, covers the entire surface of resist masks 141 through 143 formed by using the photomask5 (PM5). Fourth concentration p-type impurity regions 144 and 145 are formed by ion doping using diborane (B_2H_6). The boron (B) concentration in this region is set to be between 3 x 10^{20} and 3 x 10^{21} atoms/cm^3. (See Fig. 2D) In a previous step, phosphorous has been doped into the fourth concentration p-type impurity regions 144 and 145. Accordingly, the fourth concentration p-type impurity regions 144a and 145a has a concentration of between 1 x 10^{20} and 1 x 10^{21} atoms/cm^3 and the fourth concentration p-type impurity regions 144b and 145b has a concentration of between 1 x 10^{16} and 5 x 10^{19} atoms/cm^3. By doping boron (B) at a concentration of 1.5 to 3 times that of phosphorous in this step, there are no problems whatsoever as to the fourth concentration p-type impurity regions 144b and 145b functioning as a source region and a drain region of the p-channel TFT.

Thereafter, as shown in Fig. 3A, a protective insulating film 146 is formed from above the gate electrode and the gate insulating film. The protective insulating film may comprise a silicon oxide film, a silicon oxynitride film, a silicon nitride film or a laminate film of the combination of these films. In any case, the protective insulating film 146 is formed of an inorganic insulating material. The protective insulating film 146 has a film thickness of 100 to 200 nm. When the silicon oxide film is used, the film may be formed by plasma CVD, mixing tetraethyl orthosilicate (TEOS) and O_2, and setting the reaction pressure at 40 Pa, the substrate temperature of 300 to 400°C and discharging at a high frequency (13.56 MHz) power density of 0.5 to 0.8 W/cm^2. When the silicon oxynitride film is used, a silicon oxynitride film formed from SiH_4, NH_3 and N_2O by plasma CVD or a silicon oxynitride film formed from SiH_4 and N_2O by plasma CVD may be formed. The deposition condition in this case is the reaction pressure of 20 to 200 Pa, the substrate temperature of 300 to 400°C, and the high frequency (60 MHz) power density of 0.1 to 1.0 W/cm^2. The hydrogenated silicon oxynitride film formed from SiH_4, N_2O and H_2 may be used, as well. The silicon nitride film can be formed similarly from SiH_4 and NH_3 by plasma CVD.

Thereafter, the step for activating the impurity elements imparting n-type or p-type added in the respective concentrations is conducted. This step is conducted by a thermal annealing method using a furnace annealing oven. Besides the thermal annealing method, it is possible to employ a laser annealing method and a rapid thermal annealing method (RTA method). The thermal annealing method is conducted in a nitrogen atmosphere containing oxygen in a concentration of 1 ppm or below, preferably 0.1 ppm or below, at 400 to 700°C, typically 500 to 600°C. In this embodiment, the heat-treatment is conducted at 550°C for 4 hours. When a plastic substrate having a low heat-resistant temperature is used for the substrate 101, the laser annealing method is preferably employed (Fig. 3B).

After the activation step, heat-treatment was further conducted in an atmosphere containing 3 to 100% at 300 to 450°C for 1 to 12 hours to hydrogenate the island semiconductor films. This is the process step that terminates the dangling bonds of 10^{16} to 10^{18} /cm^3 in the island semiconductor film by hydrogen that is thermally excited. Plasma hydrogenation (using hydrogen that is excited by plasma) may be used as another means for hydrogenation.

After the activation and hydrogenation steps are completed, an interlayer insulating film 147 made of an organic insulating material is formed to a mean thickness of 1.0 to 2.0 μm. Examples of the organic resin materials are polyimide, acrylic, polyamide, polyimidamide, BCB (benzocyclobutene), and so forth. When polyimide of the type, that is thermally polymerized after being applied to the substrate, is used, the material is baked at 300°C in a clean oven. When acrylic is used, a two-component type is used. After the main agent and the curing agent are mixed, the mixture is applied to the entire surface of the substrate by using a spinner. Preparatory heating is then conducted by using a hot plate at 80°C for 60 seconds, and baking is then made in the clean oven at 250°C for 60 minutes.

By forming the interlayer insulating film from the organic insulating material, its surface can be planarized satisfactorily. The organic resin materials have generally a low dielectric constant, and the parasitic capacitance can be reduced. However, since they are hygroscopic, they are not suitable for the protective film. Therefore, the organic insulating material must be used in combination with the silicon oxide film, the silicon oxide nitride film or the silicon nitride film formed as the protective insulating film 146 as in this embodiment.

Thereafter, a resist mask having a prescribed pattern is formed by using a photo-mask 6 (PM6), and contact holes reaching the source or drain regions of the respective island semiconductor films are formed. The contact holes are formed by dry etching. In this case, a mixed gas of CF_4, O_2 and He is used as the etching gas to first etch the interlayer insulating film formed of the organic resin material. The protective insulation film 146 is then etched with etching gases of CF_4 and O_2. By switching the etching gas further to CHF_3 to improve the selection ratio with the island semiconductor layers, the gate insulating film is etched and the contact holes can be formed satisfactorily.

A conductive metal film is formed by sputtering or vacuum deposition. A resist mask pattern is then formed by using a photo-mask 7(PM7). Source wirings 148 to 152 and drain wirings 153 to 158 are formed by etching. Here, the drain wiring 157 functions as the pixel electrode. Though not shown in the drawing, in this embodiment, Ti film is formed into 50 to 150 nm thickness, a contact is formed with the semiconductor film that forms source or drain region in the island semiconductor layer, and aluminum (Al) is formed to a thickness of 300 to 400 nm in superposition with the Ti film to give this wiring.

When the hydrogenation treatment is conducted under this state, favorable results can be obtained for the improvement of TFT performance. For example, the heat-treatment is conducted preferably at 300 to 450°C for 1 to 12 hours in an atmosphere containing 3 to 100% of hydrogen. A similar effect can be obtained by using the plasma hydrogenation method. Such a heat-treatment can diffuse hydrogen existing in the protective insulating film 146 and the base film 102 into the island semiconductor films 104 to 108 and can hydrogenate these films. In any case, the defect density in the island semiconductor films 104 to 108 is lowered preferably to $10^{16}/cm^3$ or below, and for this purpose, hydrogen may be added in an amount of about 0.01 to about 0.1 atomic% (Fig. 3C).

Thus a substrate having the TFTs of the driving circuit and the pixel TFTs of the pixel section over the same substrate can be completed with 7 photo-masks. The first p-channel TFT 200, the first n-channel TFT 201, the second p-channel TFT 202 and the second n-channel TFT 203 are formed in the driving circuit. The pixel TFT 204 and the storage capacitance 205 are formed in the pixel section. In this specification, such a substrate will be referred to as an "active matrix substrate" for convenience sake.

The first p-channel TFT 200 in the driving circuit has a single drain structure, which has in the island semiconductor film 104: the channel formation region 206; and the source regions 207a and 207b and the drain regions 208a and 208b each comprising the p-type impurity region having the fourth concentration. The first n-channel TFT 201 has in the island semiconductor film 105: the channel forming region 209; the LDD region 210 that partly overlaps with the gate electrode 119 and comprises the impurity region having the first concentration; and the source region 212 and the drain region 211 comprising the impurity region having the third concentration. The LDD region that overlaps the gate electrode 119 is referred to as Lov here, and the length of this region in the direction of the channel length is 0.5 to 3.0 μm, preferably 1.0 to 2.0 μm. As the length of the LDD region in the n-channel TFT is determined in this way, a high electric field generated in the proximity of the drain region can be mitigated, and the occurrence of hot carriers and degradation of the TFT can be prevented. The second p-channel TFT 202 in the driving circuit has similarly the single drain structure including the channel forming region 213, the source regions 214a and 214b and the drain regions 215a and 215b comprising the p-type impurity region having the fourth concentration, in the island semiconductor film 106. A channel forming region 216; LDD regions 217 and 218 that partly overlap the gate electrode 121 and comprises the impurity region of the first concentration; and a source region 220 and a drain region 219 comprising the impurity region of the third concentration; are formed in the second n-channel TFT 203. The length of the Lov that partly overlaps the gate electrode of this TFT, too, is also set to 0.5 to 3.0 μm, preferably from 1.0 to 2.0 μm. Further, a LDD region that does not overlap the gate electrode is referred to as an Loff region, and its length in the channel length direction is 0.5 to 4.0 μm, preferably 1.0 to 2.0 μm. The pixel TFT 204 has in the island semiconductor film 108: channel forming regions 221 to 222; and LDD regions 223 to 225 comprising an impurity region of the second concentration; and source or drain regions 226 to 228 comprising an impurity region of the third concentration. The length of the LDD region (Loff) in the direction of the channel length is 0.5 to 4.0 μm, preferably 1.5 to 2.5 μm. Furthermore, a storage capacitance 205 comprises a capacitance wiring 123, an insulating film made of the same material as the gate insulating film and a semiconductor layer 229 that is connected to the drain region 228 of the pixel TFT 204. In Fig. 3C, the pixel TFT 204 is shown as having a double gate structure. However, it may have a single gate structure or a multi-gate structure having a plurality of gate electrodes.

Fig. 16 is a top view showing substantially one pixel of the pixel section. The cross section A – A' in the drawing corresponds to the sectional view of the pixel section shown in Fig. 3C. The gate electrode 122 of the pixel TFT 204, that functions also the gate wiring, intersects the island semiconductor layer 108 below it through a gate insulating film, which is not shown in the drawing. The source region, the drain region and the LDD region are formed in the island semiconductor layer, though they are not shown in the drawing. Reference numeral 256 denotes a contact portion between the source wiring 152 and the source region 226. Reference numeral 257 denotes a contact portion between the drain wiring 157 and the drain region 228. A storage capacitance 205 is formed by the overlapping region of the semiconductor layer 229 that extends from the drain region 228 of the pixel TFT 204 and a capacitance wiring 123 through the gate insulating film. In this construction, an impurity element for valency control is not added to the semiconductor layer 229.

The construction described above makes it possible to optimize the structure of the TFT constituting each circuit in accordance with the specification required by the pixel TFT and the driving circuit, and to improve operation performance and reliability of the semiconductor device. Furthermore, this construction makes it easy to activate the LDD region, the source region and the drain region by forming the gate electrode by a conductive material having heat resistance.

[Embodiment 2]

To accomplish a high-precision and high-quality liquid crystal display device, the characteristics of the TFT constituting the each circuit of the pixel TFT and the driving circuit must be improved. One of the required TFT characteristics is the decrease of the current flowing under the OFF state (OFF current) besides the threshold voltage, the field effect mobility, the sub-threshold coefficient (S value), and so forth. When the OFF current value is high, not only the power consumption increases, but also the operation characteristics of the driving circuit get deteriorated and may invite the drop of image quality. In the n-channel TFT fabricated in Embodiment 1, the LDD region is formed, and this LDD region can lower the OFF current value to the extent that renders no problem. On the other hand, since the p-channel TFT has the single drain structure, the increase of the OFF current value often becomes the problem. This embodiment provides a method of fabricating a p-channel TFT having an offset region suitable to cope with such a problem, by referring to Fig. 4A to 4C.

The process steps shown in Figs. 1A to 2A are conducted first in the same way as in Embodiment 1, and the gate electrodes 118 to 122 and the capacitance wiring 123 are formed. Next, the step of adding the impurity element imparting n-type (n^- doping step) is conducted to form the LDD region in the n-channel TFT. Here, the impurity element imparting n-type is added by self-alignment using a gate electrodes. In this case, by using a photo-mask, the entire surface of island semiconductor layers 104 and 106, on which the p-channel TFT is to be formed, is covered with resist masks 158 and 159 so that the impurity element is not added to these areas. In this way, the n-type impurity regions 125 to 129 having the second concentration are formed in the island semiconductor layers as shown in Fig. 4A.

Next, in the n-channel TFT, an n-type impurity region having the third concentration that functions as the source or drain region is formed. Resist masks 130 to 134 are formed by using a photo-mask, and an impurity element imparting n-type is added to form n-type impurity regions 135 to 140 having the third concentration (Fig. 4B).

Thereafter, a protective insulating layer 146 is formed in the same way as in Embodiment 1. P-type impurity regions 144 and 145 having the fourth concentration to serve as the source and drain regions are formed in the island semiconductor layers 104 and 106 that constitute the p-channel TFT. Resist masks 160 to 162 are formed by using the photo-mask to cover the entire surface of the island semiconductor films 105, 107 and 108 that constitute the n-channel TFTs. This step is conducted by ion doping.

The impurity element doped has slight fluctuation but is incident substantially vertically to the surface of the island semiconductor layers. The protective insulating layer 146 is formed with good coverage even at the end portion of the gate electrode. Therefore, the protective insulating layer formed at the end portion serves as a mask, and p-type impurity regions 144 and 145 having the fourth concentration are formed in the spaced-apart relation from the gate electrode by the distance corresponding to the film thickness of the protective insulating layer. In other words, offset regions 230 and 231 are formed to a length L_0 between the channel forming region and the p-type impurity region having the fourth concentration. More concretely, since the length L_0 corresponds to the thickness of the protective insulating layer 146, it is formed to a length of 100 to 200 nm.

Such an offset region contributes as a series resistance component to the electric characteristics of the TFT, and can reduce the OFF current value by about 1/10 to 1/100. Subsequently, the process steps from Fig. 3A are carried out in the same way as in Embodiment 1. An active matrix substrate can be completed by using seven photo-masks.

[Embodiment 3]

Embodiment 1 showed the example that uses the heat-resistant conductive material such as W and Ta for the gate electrode. The reason why such materials are used is because the impurity elements that are added mainly for valency control are activated by thermal annealing at 400 to 700°C after the gate electrode is formed. However, such heat-resistant conductive material has the sheet resistivity of about 10 Ω and are not suitable for a liquid crystal display device having a screen size of 4 inches or more. When the gate wiring connected to the gate electrode is made of the same material, the length of the lead wire on the substrate becomes essentially great, and the wiring delay resulting from the influence of the wiring resistance cannot be neglected.

When the pixel density is VGA, for example, 480 gate wirings and 640 source wirings are formed. When the pixel density is XGA, 768 gate wirings and 1,024 source wirings are formed. As for the screen size of the display region, the length of the diagonal is 340 mm in the case of the 13-inch class and 460 mm in the case of the 18-inch class. This embodiment explains the method of accomplishing such a liquid crystal display device by using low resistance conductive materials such as Al or Cu (copper) for the gate wirings with reference to Figs. 5A to 5C.

First, the process steps shown in Figs. 1A to 2D are conducted in the same way as in Embodiment 1. Next, the step for activating the impurity elements added to the respective island semiconductor layer for valency control is performed. This step is carried out by the thermal annealing method using the furnace annealing oven. The laser annealing method or the rapid thermal annealing method (RTA method) can be employed besides the thermal annealing method. This thermal annealing method is conducted in a nitrogen atmosphere having an oxygen concentration of 1 ppm or below, preferably 0.1 ppm or below, at 400 to 700°C, typically at 500 to 600°C. In this embodiment, the heat-treatment is conducted at 525°C for 4 hours.

In this heat-treatment, conductive layers (C) 118c to 123c are formed to a thickness of 5 to 80 nm from the surface on the conductive layers (B) 118b to 123b forming the gate electrodes 118 to 122 and the capacitance wiring 123. When the conductive layers (B) 118b to 123b are made of tungsten (W), for example, tungsten nitride (WN) is formed and when they are made of tantalum (Ta), tantalum nitride (TaN) is formed. The conductor layers (C) 118c to 123c can be formed similarly by exposing the gate electrodes 118 to 123 to a plasma atmosphere containing nitrogen, such as nitrogen or ammonia. The heat-treatment is carried out further in an atmosphere containing 3 to 100% hydrogen at 300 to 450°C for 1 to 12 hours to hydrogenate the island semiconductor layers. This process step is the one that terminates the dangling bonds of the semiconductor layers by thermally excited hydrogen. Plasma hydrogenation (using hydrogen excited by plasma) may be used as another hydrogenation means (Fig. 5A).

After the activation and hydrogenation steps are completed, the gate wirings are made of the low resistance conductive material. The low resistance conductive layer is formed of a conductive layer (D) containing Al or Cu as the principal component. For example, an Al film containing 0.1 to 2 wt% of Ti is formed as the conductor layer (D) on the entire surface (not shown in the drawing). The thickness of the conductive layer (D) 145 is 200 to 400 nm (preferably, 250 to 350 nm). Predetermined resist patterns are formed using a photo-mask and etching is conducted to form the gate wirings 163 and 164 and the capacitance wiring 165. This etching is made by wet etching using a phosphoric acid type etching solution and removes the conductor layer (D). In this way, the gate lead wires can be formed while keeping selective workability with the base films. A protective insulating film 146 is then formed (Fig. 5B).

An interlayer insulating film 147 made of an organic insulating material, source wirings 148 to 151 and 167 and drain wirings 153 to 156 and 168 are formed in the same way as in Embodiment 1. An active matrix substrate can be thus completed. Figs. 6A and 6B are top views of this state. The B – B' section of Fig. 6A and the C – C' section of Fig. 6B correspond to A – A' and C – C' of Fig. 5C, respectively. The gate insulating film, the protective insulating film and the interlayer insulating film are omitted in Figs. 6A and 6B. However, the source wirings 148, 149 and 167 and the drain wirings 153, 154 and 168 are connected to the source and drain regions, not shown, of the island semiconductor layers 104, 105 and 108 through contact holes. The D – D' section of Fig. 6A and the E – E' section of Fig. 6B are shown in Figs. 7A and 7B, respectively. The gate wiring 163 and 164 are formed in such a fashion that the former 163 overlaps with the gate electrodes 118 and 119 and the latter 164, with the gate electrode 122, outside the island semiconductor layers 104, 105 and 108, respectively. The conductor layer (C) and the conductor layer (D) are in contact, and connected electrically. In this way, the wiring resistance can be lowered sufficiently by forming the gate wiring from the low resistance conductive material. Therefore, this embodiment can be applied to the display device having the pixel section (screen size) of the 4-inch class or larger.

[Embodiment 4]

The active matrix substrate fabricated in Embodiment 1 can be applied to a reflection type liquid crystal display device. When it is applied to a transmission type liquid crystal display device on the other hand, the pixel electrode provided to each pixel of the pixel section may be formed of the transparent electrode. In this embodiment, a method of fabricating the active matrix substrate adapted to the transmission type liquid crystal display device will be explained with reference to Figs. 10A and 10B.

The active matrix substrate is manufactured in the same way as in Embodiment 1. In Fig. 10A, the source wiring and the drain wiring are formed from a conductive metal film by sputtering or vacuum evaporation. A Ti film is formed to a thickness of 50 to 150 nm and a contact is formed with the semiconductor films that form the source or drain region in the island semiconductor layer. Aluminum (Al) is formed to a thickness of 300 to 400 nm in superposition with the Ti film. Furthermore, a Ti film or a titanium nitride (TiN) film is formed to a thickness of 100 to 200 nm. In this way, a three-layered structure is completed. Thereafter, a transparent conductive film is formed on the entire surface, and pixel electrode 171 is formed by patterning treatment and etching treatment with a photo-mask. The pixel electrode 171 is formed on the interlayer insulating film 147, and a portion overlapping with the drain wiring 169 of each pixel TFT 204 is disposed to form a connection structure.

Fig. 10B is an example of first forming a transparent conductor film on the interlayer insulating film 147, forming the pixel electrode 171 through patterning treatment and etching treatment, and then forming drain wiring 169 to dispose portions that overlap the pixel electrode 171. The drain wiring 169 is disposed by: forming a Ti film to a thickness of 50 to 150 nm; forming contact with a semiconductor film which form the source or drain region in the island semiconductor layer; and forming aluminum (Al) to a thickness of 300 to 400 nm in superposition with the Ti film. According to this construction, the pixel electrode 171 comes into contact with only the Ti film that forms the drain wiring 169. As a result, the reaction between the transparent conductor film and Al can be prevented.

Indium oxide (In_2O_3) or an indium oxide – tin oxide alloy (In_2O_3-SnO_2; ITO) may be formed by sputtering or vacuum evaporation as the material of the transparent conductor film. Etching treatment of such a material is made by using a hydrochloric acid type solution. However, because the residue is likely to remain particularly in etching of ITO, indium oxide – zinc oxide alloy (In_2O_3 – ZnO) may be used to improve the etching factor. The indium oxide – zinc oxide alloy is excellent in surface flatness and heat stability with respect to ITO. Therefore, this material can prevent the corrosive reaction with Al which comes into contact on the end face of the drain wiring

169. Similarly, zinc oxide (ZnO) is a suitable material, and further, zinc oxide added with gallium (Ga) (ZnO:Ga), for improving transmissivity of the visible rays and the electric conductivity can be used, too.

In this way, an active matrix substrate adaptable to the transmission type liquid crystal display device can be completed. Though this embodiment has been explained by using the same process steps as those of Embodiment 1, this construction can be applied to the active matrix substrate shown in Embodiment 2 and Embodiment 3.

[Embodiment 5]

This embodiment shows another method of fabricating the crystalline semiconductor layer for forming the active layer of the TFTs of the active matrix substrate described in Embodiments 1 through 4. The crystalline semiconductor layer is formed by crystallizing the amorphous semiconductor layer by thermal annealing, laser annealing or RTA, etc. In addition, the crystallization method using a catalytic element, that is disclosed in Japanese Patent Application Laid-Open No. 7-130652, can be applied. An example of this case will be explained with reference to Figs. 8A to 8C.

Base films 102a and 102b and an amorphous semiconductor layer 103a to a thickness of 25 to 80 nm are formed over a glass substrate 101 in the same way as in Embodiment 1, as shown in Fig 8A. An amorphous silicon film, for example, is formed to a thickness of 55 nm. An aqueous solution containing 10 ppm, calculated by weight, of a catalytic element is applied by a spin coating method to form a layer 170 containing the catalytic element. Examples of the catalytic element include nickel (Ni), germanium (Ge), iron (Fe), palladium (Pd), tin (Sn), lead (Pb), cobalt (Co), platium (Pt), copper (Cu) and gold (Au). Besides spin coating, the layer 170 containing the catalytic element may be formed by sputtering or vacuum evaporation so that the thickness of the layer of the catalytic element is 1 to 5 nm.

In the crystallization step shown in Fig. 8B, heat treatment is conducted first at 400 to 500°C for about 1 hour and the hydrogen content of the amorphous silicon film is lowered to not greater than 5 atom%. Thermal annealing is then conducted in a nitrogen atmosphere at 550 to 600°C for 1 to 8 hours by using a furnace annealing oven. This process step can acquire a crystalline silicon layer 103c comprising the crystalline silicon film (Fig. 8C). When the crystalline semiconductor layer 103c formed by heat annealing is observed macroscopically through an optical microscope in this case, however, amorphous regions are found sometimes remaining locally in the crystalline semiconductor layer 103c formed by this heat annealing, and amorphous components having a broad peak at 480 cm^{-1} is observed by a Raman spectroscopy. Therefore, it is effective to process the crystalline semiconductor layer 103c by the laser annealing method after heat annealing in the same way as in Embodiment 1 to improve its crystallinity.

An active matrix substrate can be completed similarly to Embodiment 1 when island semiconductor layers 104 to 108 are manufactured from thus formed crystalline semiconductor film 103c. However, in case of using a catalyst element that promotes crystallization of silicon in the crystallization step, a trace amount (approximately 1×10^{17} to 1×10^{19} atoms/cm^3) of catalyst element remained in the island semiconductor layers. Though it is possible to complete TFTs in such a state, it was more preferable to remove the remained catalytic elements at least from the channel forming regions. There is a means using gettering effect by phosphorus (P) to remove the catalytic element.

A gettering treatment with phosphorus (P) for this purpose can be conducted simultaneously with the activation step explained in Fig. 3B. This process step is shown in Fig. 9. The concentration of phosphorus (P) necessary for gettering may be approximately the same as the impurity concentration of the n-type impurity region having the third concentration. Thermal annealing of the activation step can make the catalytic element to segregate from the channel formation region of the n-channel TFT and the p-channel TFT to the impurity region containing phosphorus (P) in that concentration (in the direction indicated by an arrow in Fig. 9). As a result, the catalytic element segregates in a concentration of 1×10^{17} to 1×10^{19} atoms/cm^3 in the impurity region. The TFT thus fabricated has a lowered OFF current value and has high crystallinity. Therefore, high field effect mobility can be obtained, and excellent characteristics can be accomplished.

[Embodiment 6]

This embodiment explains the manufacturing steps of an active matrix liquid crystal display device from the active matrix substrate manufactured in Embodiment 1. First, as shown in Fig. 11A, a spacer comprising a columnar spacer is formed on the active matrix substrate under the state shown in Fig. 3C. The spacer may be formed by spraying of particles having a size of several microns. In this embodiment, however, a method of forming the spacers by forming a resin film over the entire surface of the substrate and then patterning, was adopted. The material of the spacer is not limited, in particular. For example they may be formed by using “NN700” of JSR Co., and after the material is coated by a spinner, a prescribed pattern is formed by exposure and development. The pattern is then heated and cured at 150 to 200°C in a clean oven, or the like. The shape and size of the spacer can be changed depending on the conditions of exposure and development. Preferably, however, the columnar spacer 173 has a columnar shape with a flat top as shown in Fig. 13. When the substrate on the opposite side is put, the mechanical strength as the liquid crystal display panel can be secured. The shape is not particularly limited and may be conical or pyramidal. When it is conical, for example, the height H is 1.2 to 5 μm, the mean radius L1 is 5 to 7 μm and the ratio of the mean radius L1 to the radius L2 of the bottom is 1:1.5. The taper angle of the side surface is not greater than ±15° at this time.

The arrangement of the columnar spacer may be decided arbitrarily. Preferably, however, the columnar spacer 173 is disposed in such a manner as to be superposed with, and cover, the contact section of the drain wiring 168 (pixel electrode) in the pixel section as shown in Fig. 11A. Since planarity at the contact section is lost and the liquid crystal is not oriented well at this section, disclination, etc. can be prevented by forming the columnar spacer 173 in the form in which the spacer resin is filled to the contact section.

Thereafter, the alignment film 174 is formed. A polyimide resin is used generally for the alignment film of the liquid crystal display element. After the alignment film is formed, rubbing treatment is conducted so that the liquid crystal molecules are oriented with a certain pre-tilt angle. The region from the end portion of the columnar spacer 173 disposed in the pixel section to the region that is not rubbed, in the rubbing direction is not greater than 2 μm. The occurrence of static electricity often becomes the problem during the rubbing treatment. When the spacer 172 is formed over the TFT of the driving circuit, too, both original role as the spacer and the protection effect of the TFT from static electricity can be acquired.

A shielding film 176, a transparent conductive film 177 and an alignment film 178 are formed on an opposing substrate 175 on the opposite side. Ti, Cr, Al or the like is formed to a thickness of 150 to 300 nm as the shielding film 176. The active matrix substrate on which the pixel section and the driving circuit are formed and the opposing substrate are bonded to each other through a sealant 179. A filler 180 is mixed in the sealant 179. These two substrates are bonded together while keeping a uniform gap by the filler 180 and the spacers 172 and 173. Thereafter, a liquid crystal material 606 is injected between both substrates, and the substrates are completely sealed by the sealant (not shown). A known liquid crystal material may be used for the liquid crystal material. In this way, the active matrix liquid crystal display device shown in Fig. 11B can be completed.

It is also possible to first form the alignment film 174 and then form the spacer, as shown in Fig. 19.

Fig. 11 shows the example where the spacer 172 is formed on the entire surface of the TFT of the driving circuit. However, the spacer may be divided into a plurality of spacers 172a to 172e as shown in Fig. 12. The spacer disposed at the area where the driving circuit are formed may formed in such a manner as to cover at least the source and drain wirings of the driving circuit. According to this construction, each TFT of the driving circuit is completely covered and protected by the protective insulating film 146, the interlayer insulating film 147 and the spacer 172 or the spacers 172a to 172e.

Fig. 14 is a top view of an active matrix substrate. It is the top view showing the positional relationship among the pixel section, the driving circuit section, the spacers and the sealant. A scanning signal driving circuit 185 and an image signal driving circuit 186 are disposed as the driving circuit in the peripheral of the pixel section 188. A signal processing circuit 187 such as a CPU, a memory, etc, may be further added. These driving circuits are connected to external input/output terminals 182 by connection wiring 183. In the pixel unit 188, a group of gate wirings 189 extending from the scanning signal driving circuit 185 and a group of source wirings

190 extending from the image signal driving circuit 186 cross one another in the matrix form. A pixel TFT 204 and a storage capacitance 205 are provided to each pixel.

The columnar spacer 173 disposed in the pixel section may be provided to all the pixels, or, they may be provided to every several or dozens of pixels disposed in matrix. In other words, the proportion of the number of spacers to the total number of pixels constituting the pixel unit may be preferably 20 to 100%. The spacers 172, 172' and 172" provided to the driving circuit section may be disposed in such a fashion as to cover the entire surface of the driving circuit section, or may be divided into several segments in match with the positions of the source and drain wirings of the TFT as shown in Fig. 12.

The sealant 179 is applied outside the pixel section 188, the scanning signal control circuit 185, the image signal control circuit 186 and other signal processing circuits 187 over the substrate 101, but inside the external input/output terminals 182.

The construction of such an active matrix liquid crystal display device will be explained with reference to the perspective view of Fig. 15. In Fig. 15, the active matrix substrate comprises the pixel section 188, the scanning signal driving circuit 185, the image signal driving circuit 186 and other signal processing circuit 187 formed over the glass substrate 101. The pixel TFT 204 and the storage capacitance 205 are provided to the pixel section 188. The driving circuit disposed in the periphery of the pixel section comprises the CMOS circuit as the basic circuit. The scanning signal driving circuit 185 and the image signal driving circuit 186 are connected to the pixel TFT 204 by the gate wiring 122 and the source lead wiring 152. A flexible printed circuit (FPC) 191 is connected to the external input terminal 182 and is used for inputting the image signal, and the like. It is connected to the respective driving circuit by connection wiring 183. Though not shown in the figure, the shielding film and the transparent electrodes are disposed on the opposing substrate 175.

Fig. 18 is an explanatory view used for explaining the connection structure between the external input/output terminal 182 and the FPC 191. The external input/output terminal 182 is formed from the conductive metal film in the same structure as the source wiring or the drain wiring, and is formed on the substrate 101 from which the interlayer insulating film 147 is removed. The FPC 191 has copper wirings 302 formed on the organic resin film 301 such as polyimide and is connected to the external input/output terminal 182 by an anisotropic conductive adhesive. The anisotropic conductive adhesive comprises an adhesive 303 and particles 304 that have a diameter of dozens to hundreds of microns, have a conductive surface plated with gold, or the like, and are mixed in the adhesive 303. When the particles 304 come into electric contact with the external input/output terminal 182 and with the copper wirings 302, the electric contact is established at such portions. The FPC 191 swells out from the external input/output terminals 182 and is bonded so as to improve the bonding strength with the substrate 101. It has a resin layer 192 at its end portion to improve the mechanical strength at this portion.

Further, as shown in Fig. 20, when the connection structure of the external input/output terminals 182 and the FPC 191 are made the same, and the spacer 199 is further provided to the outside of the sealant 179 and clamped between the active matrix substrate and the opposing substrate, the mechanical strength at this portion can be increased. This construction functions particularly effectively when a part of the opposing substrate is cut off so as to expose the external input/output terminals 182.

The liquid crystal display device having such a construction can be fabricated by using the active matrix substrate explained in Embodiments 1 through 4. When the active matrix substrate of any of Embodiments 1 through 3 is used, a reflection type liquid crystal display device can be obtained. When the active matrix substrate shown in Embodiment 4 is used, a transmission type liquid crystal display device can be obtained.

[Embodiment 7]

Fig. 17 shows an example of the circuit construction of the active matrix substrate shown in Embodiments 1 through 4. The drawing shows a circuit construction of a direct-view type display device. The active matrix substrate comprises an image signal driving circuit 186, scanning signal driving circuits (A) and (B) 185 and a pixel section 188. Incidentally, the term "driving circuit" used in this specification is a generic term that includes the image signal driving circuit 186 and the scanning signal driving circuit 185.

The image signal driving circuit 186 comprises a shift register circuit 501a, a level shifter circuit 502a, a buffer circuit 503a and a sampling circuit 504. The scanning signal driving circuits (A) and (B) 185 comprise a shift register circuit 501b, a level shifter circuit 502b and a buffer circuit 503b.

Shift register circuits 501a and 501b use a driving voltage of 5 to 16 V (typically, 10 V). The TFT constituting the CMOS circuit for forming this circuit comprises the first p-channel TFT 200 and the first n-channel TFT 201 shown in Fig. 3C. The driving voltages of the level shifter circuits 502a and 502b and the buffer circuits 503a and 503b are as high as 14 to 16 V, but the TFTs similar to that of the shift register circuit may be used. The withstand voltage can be improved when these circuits are constituted into the multi-gate structure, and reliability of the circuit can be improved effectively.

A sampling circuit 504 comprises an analog switch and its driving voltage is 14 to 16 V. Since this circuit is driven while its polarity is alternately reversed and moreover, since the OFF current value must be lowered, the sampling circuit 504 preferably comprises the second p-channel TFT 202 and the second n-channel TFT 203 shown in Fig. 3C. When the OFF current value of the p-channel TFT 202 becomes the problem in this circuit, the TFT having the single drain structure having the offset region and fabricated in Embodiment 2 is preferably used.

The driving voltage of the pixel section is 14 to 16 V. The OFF current value must be further lowered than in the sampling circuit from the aspect of low power consumption. Therefore, the TFT having the multi-gate structure and further having the LDD region, such as the pixel TFT 204 shown in Fig. 3C, is preferably used.

The constitutions of this embodiment can be achieved easily by manufacturing the TFTs in accordance with the process steps shown in Embodiments 1 through 4. Though this embodiment shows only the constructions of the pixel section and the driving circuit, it is possible to form other circuits such as a signal divider circuit, a frequency divider circuit, a D/A converter, a γ correction circuit, an operational amplifier circuit, a signal processing circuit such as a memory circuit and an arithmetic processing circuit, or a logic circuit, over the same substrate in accordance with the process steps of Embodiments 1 through 4. As described above, the present invention can accomplish a semiconductor device comprising a pixel section and the driving circuit over a substrate, for example, a liquid crystal display device comprising the pixel section and the signal controlling circuit over a substrate.

[Embodiment 8]

The active matrix substrate, the liquid crystal display device and the EL display device fabricated in accordance with the present invention can be used for various electro-optical devices. The present invention can be applied to all those electronic appliances that include such an electro-optical device as the display medium. Examples of the electronic appliances include a personal computer, a digital camera, a video camera, a portable information terminal (a mobile computer, a cellular telephone, an electronic book), and a navigation system. Fig. 22A to 22F show examples of these.

Fig. 22A shows a personal computer, which comprises: a main body 2001 comprising a microprocessor and a memory; an image input section 2002; a display device 2003; and a keyboard 2004. The present invention can form the display device 2003 or other signal processing circuits.

Fig. 22B shows a video camera, which comprises: a main body 2101; a display device 2102; a sound input section 2103; an operation switch 2104; a battery 2105; and an image receiving section 2106. The present invention can be applied to the display device 2102 or other signal control circuits.

Fig. 22C shows the portable information terminal, that comprises: a main body 2201; an image input section 2202; an image receiving section 2203; an operation switch 2204; and a display device 2205. The present invention can be applied to the display device 2205 or other signal controlling circuits.

Such a portable information terminal is often used indoors as well as outdoors. To operate the terminal for a long time, a reflection type liquid crystal display device utilizing external light is more suitable for the low power consumption type than the type using back-light. However, when the environment is dark, a transmission type liquid crystal display device quipped with back-light is more suitable. Under such circumstances, a hybrid type liquid crystal display device having the features of both reflection type and transmission type has been developed. The present invention can be also applied to such a hybrid type liquid crystal display device. Fig. 21 shows an example of such an application to the portable information terminal. The display device 2205 comprises a touch panel 3002, a liquid crystal display device 3003 and LED back-light 3004. The touch panel 3002 is provided so as to easily operate the portable information terminal. A light emitting element 3100 such as LED is disposed at one of the ends of the touch panel 3002 and a light receiving device 3200 such as a photo-diode is disposed at the other end. An optical path is defined between them. When the touch panel 3002 is pushed and the optical path is cut off, the output of the light receiving element 3200 changes. When these light emitting elements and light receiving elements are disposed in matrix on the liquid crystal display device by utilizing this principle, the touch panel can be allowed to function as the input medium.

Fig. 21B shows the construction of the pixel section of the hybrid type liquid crystal display device. A drain electrode 169 and a pixel electrode 171 are disposed on an interlayer insulating film 147. Such a construction can be achieved by applying Embodiment 4. The drain electrode has a laminate structure of a Ti film and an Al film and operates also as the pixel electrode. The pixel electrode 171 is made of the transparent conductive film material explained in Embodiment 4. As the liquid crystal display device 3003 is fabricated from the active matrix substrate, it can be used suitably for the portable information terminal.

Fig. 22D shows an electronic game machine such as a television game or a video game. It comprises a main body 2301 having mounted thereto an electronic circuit 2308 such as a CPU, a recording medium 2304, etc.; a controller 2305; a display device 2303; and a display device 2302 that is assembled in the main body 2301. The display device 2303 and the display device 2302 assembled in the main body 2301 may display the same information. Alternatively, the latter may be used mainly as a main display device and the latter, as a sub-display device to display the information of the recording medium 2304, the operation condition of the apparatus or as an operation board by adding the function of a touch sensor. The main body 2301, the controller 2305 and the display device 2303 may have wire communication functions to transmit signals between them, or may be equipped with sensor units 2306 and 2307 for achieving wireless communication or optical communication function. The present invention can be applied to the display devices 2302 and 2303. A conventional CRT may be used for the display device 2303.

Fig. 22E shows a player that uses a recording medium storing a program (hereinafter called the "recording medium"). It comprises a main body 2401, a display device 2402, a speaker unit 2403, a recording medium 2404 and an operation switch 2405. Incidentally, a DVD (Digital Versatile Disc) or a compact disk (CD) can be used for the recording medium to reproduce a music program or to display images or information display such as a video game (or a television game) and information display through the Internet. The present invention can be utilized suitably for the display device 2402 and other signal control circuits.

Fig. 22F shows a digital camera, which comprises: a main body 2501; a display device 2502; a view finder section 2503; an operation switch 2504; and an image reception unit (not shown). The present invention can be applied to the display unit 2502 or other signal control circuits.

Fig. 23A shows a front type projector, which comprises: a light source optical system and a display device 2601; and a screen 2602. The present invention can be applied to the display device and other signal control circuits. Fig. 23B shows a rear type projector, which comprises: a main body 2701; a light source optical system and a display device 2702; a mirror 2703; and a screen 2704. The present invention can be applied to the display device or other signal control circuit.

Incidentally, Fig. 23C shows an example of the construction of the light source optical system and the display devices 2601 and 2702 in Figs. 23A and 23B. The light source optical system and the display device 2601 and 2702 comprise a light source optical system 2801, mirrors 2802, 2804 to 2806, a dichroic mirror 2803, a beam splitter 2807, a liquid crystal display device 2808, a phase difference plate 2809 and a projection optical system 2810. The projection optical system 2810 comprises a plurality of optical lenses. Fig. 23C shows an example of the three-plate system that uses three liquid crystal display devices 2808. However, the present invention is not limited to such a system, but may be applied to a single-plate optical system. Optical lenses, a film having a polarization function, a film for adjusting the phase, an IR film, etc, may be inserted appropriately in the optical path indicated by an arrow in Fig. 23C. Fig. 23D shows a structural example of the light source optical system 2801 in Fig. 23C. In this embodiment, the light source optical system 2801 comprises: a reflector 2811; a light source 2812; lens arrays 2813 and 2814; a polarization conversion element 2815; and a convergent lens 2816. Incidentally, the light source optical system shown in Fig. 23D is an example but is in no way restrictive.

The present invention can be applied to a read circuit of a navigation system or an image sensor, though they are not shown in the drawings. The application range of the present invention is thus extremely broad, and the present invention can be applied to electronic appliances of all fields. The electronic appliances of this embodiment can be accomplished by the crystallization techniques of Embodiments 1 through 4.

When the present invention is employed, the TFTs having suitable performance can be arranged in accordance with the specification required by each functional circuit in the semiconductor devices (concretely, the electro-optical devices here) having a plurality of functional circuits formed on the same substrate. Moreover, the operation characteristics of such TFTs can be drastically improved.

According to the manufacturing method of the semiconductor device of the present invention, the active matrix substrate, in which the p-channel TFT of the driving circuit has the single drain structure, the n-channel TFT has the GOLD structure or the LDD structure, and the pixel TFT of the pixel section has the LDD structure, can be fabricated by using six photo-masks. A reflection type liquid crystal display device can be fabricated from such an active matrix substrate. A transmission type liquid crystal display device can be fabricated in accordance with the same process steps by using seven photo-masks.

According to the manufacturing method of the semiconductor device of the present invention, an active matrix substrate, in which the p-channel TFT of the driving circuit has the single drain structure having the offset region, the n-channel TFT has the GOLD structure or the LDD structure, and pixel TFT of the pixel section has the LDD structure, can be fabricated by using seven photo-masks. The reflection type liquid crystal device can be fabricated from such an active matrix substrate. A transmission type liquid crystal display device can be fabricated in accordance with the same process steps by using eight photo-masks.

According to the present invention, with respect to the TFTs having the gate electrode formed from the heat-resistant conductive material and the gate wiring of formed from the low resistance conductive material, the fabrication method of the active material substrate in which the p-channel TFT of the driving circuit has the single drain structure, the n-channel TFT has the GOLD structure and the LDD structure, and the pixel TFT of the pixel section has the LDD structure, by using seven photo-masks.

The reflection type liquid crystal display device can be fabricated from such an active matrix substrate. The transmission type liquid crystal display device can be fabricated in accordance with the same process steps by using eight photo-masks.

As described above, the number of photo-masks necessary for fabricating the active matrix substrate is limited to 6 to 8. In consequence, the fabrication process can be simplified, and the production cost can be drastically reduced.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a pixel TFT disposed in a pixel section; and

a driver circuit comprising a p-channel TFT and an n-channel TFT,

over a substrate,

wherein:

the p-channel TFT of the driver circuit comprises a channel forming region and a p-type impurity region of a fourth concentration that forms a source region or a drain region;

the n-channel TFT of the driver circuit comprises a channel forming region, an n-type impurity region of a first concentration which forms a LDD region that is disposed in contact with the channel forming region and partly overlaps a gate electrode, and an n-type impurity region of a third concentration which is disposed in the outside of the n-type impurity region of the first concentration and forms a source region or a drain region;

the pixel TFT comprises a channel forming region, an n-type impurity region of a second concentration which is disposed in contact with the channel forming region and forms a LDD region, and an n-type impurity region of the third concentration which is disposed in the outside of the n-type impurity region of the second concentration and forms a source region or a drain region and

a pixel electrode disposed in the pixel section has a light reflective surface, the pixel electrode is formed over an interlayer insulating film comprising an organic insulating material, and is connected to the pixel TFT through an opening formed in a protective insulating film comprising an inorganic insulating material disposed over a gate electrode of the pixel TFT and in the interlayer insulating film formed in contact with the protective insulating film.

2. A semiconductor device comprising:

a pixel TFT disposed in a pixel section; and

a driver circuit comprising a p-channel TFT and an n-channel TFT,

over a substrate,

wherein:

the p-channel TFT of the driver circuit comprises a channel forming region and a p-type impurity region of a fourth concentration that forms a source region or a drain region;

the n-channel TFT of the driver circuit comprises a channel forming region, an n-type impurity region of a first concentration which forms a LDD region that is disposed in contact with the channel forming region and partly overlaps a gate electrode, and an n-type impurity region of a third concentration which is disposed in the outside of the n-type impurity region of the first concentration and forms a source region or a drain region;

the pixel TFT comprises a channel forming region, an n-type impurity region of a second concentration which is disposed in contact with the channel forming region and forms a LDD region, and an n-type impurity region of the third concentration which is disposed in the outside of the n-type impurity region of the second concentration and forms a source region or a drain region; and

a pixel electrode disposed in the pixel section has a light transmitting property, the pixel electrode is formed over an interlayer insulating film comprising an organic insulating material, and is connected to a conductive metal wiring connected to the pixel TFT through an opening formed in a protective insulating film comprising an inorganic insulating material disposed over a gate electrode of the pixel TFT and in the interlayer insulating film formed in contact with the protective insulating film.

3. A semiconductor device having a liquid crystal sandwiched between a pair of substrates, wherein:

one of the substrates comprises a pixel TFT disposed in a pixel section and a p-channel TFT and an n-channel TFT of a driver circuit, wherein:

the p-channel TFT of the driver circuit comprises a channel forming region, a p-type impurity region of a fourth concentration which forms a source region or a drain region;

the n-channel TFT of the driver circuit comprises a channel forming region, an n-type impurity region of a first concentration which is disposed in contact with the channel forming region and forms a LDD region that partly overlaps a gate electrode and an n-type impurity region of a third concentration which is disposed on the outside of the n-type impurity region of the first concentration and forms a source region or a drain region;

the pixel TFT comprises a channel forming region, an n-type impurity region of a second concentration which is disposed in contact with the channel forming region and forms a LDD region and an n-type impurity of the third concentration which is disposed on the outside of the n-type impurity region of the second concentration and forms a source region or a drain region;

a pixel electrode disposed in the pixel section has a light reflective surface, the pixel electrode is formed over an interlayer insulating film comprising an organic insulating material and is connected to the pixel TFT through an opening formed in a protective insulating film comprising an inorganic insulating material disposed over a gate electrode of the pixel TFT and in the interlayer insulating film formed in contact with the protective insulating film; and said one of the substrate is stuck to the other substrate on which a transparent conductive film is formed, through at least a columnar spacer formed on superposition of the opening.

4. A semiconductor device having a liquid crystal sandwiched between a pair of substrates, wherein:

one of the substrates comprises a pixel TFT disposed in a pixel section and a p-channel TFT and an n-channel TFT of a driver circuit, wherein:

the p-channel TFT of the driver circuit comprises a channel forming region, a p-type impurity region of a fourth concentration which forms a source region or a drain region;

the n-channel TFT of the driver circuit comprises a channel forming region, an n-type impurity region of a first concentration which is disposed in contact with the channel forming region and forms a LDD region that partly overlaps a gate electrode and an n-type impurity region of a third concentration which is disposed on the outside of the n-type impurity region of the first concentration and forms a source region or a drain region;

the pixel TFT comprises a channel forming region, an n-type impurity region of a second concentration which is disposed in contact with the channel forming region and forms a LDD region and an n-type impurity of the third concentration which is disposed on the outside of the n-type impurity region of the second concentration and forms a source region or a drain region;

a pixel electrode disposed in the pixel section has a light transmitting property, the pixel electrode is formed over an interlayer insulating film comprising an organic insulating material, and is connected to a conductive metal wiring connected to the pixel TFT through an opening formed in a protective insulating film comprising an inorganic insulating material disposed over a gate electrode of the pixel TFT and in the interlayer insulating film formed in contact with the protective insulating film; and

said one of the substrate is stuck to the other substrate on which a transparent conductive film is formed, through at least a columnar spacer formed on superposition of the opening.

5. A semiconductor device according to claim 1 wherein the p-channel TFT of the driver circuit comprises a offset region between the channel forming region and the p-type impurity region of the fourth concentration which forms a source region or a drain region.

6. A semiconductor device according to claim 2 wherein the p-channel TFT of the driver circuit comprises a offset region between the channel forming region and the p-type impurity region of the fourth concentration which forms a source region or a drain region.

7. A semiconductor device according to claim 3 wherein the p-channel TFT of the driver circuit comprises a offset region between the channel forming region and the p-type impurity region of the fourth concentration which forms a source region or a drain region.

8. A semiconductor device according to claim 4 wherein the p-channel TFT of the driver circuit comprises a offset region between the channel forming region and the p-type impurity region of the fourth concentration which forms a source region or a drain region.

9. A semiconductor device according to claim 5 wherein the p-channel TFT of the driver circuit is used as an analog switch.

10. A semiconductor device according to claim 6 wherein the p-channel TFT of the driver circuit is used as an analog switch.

11. A semiconductor device according to claim 7 wherein the p-channel TFT of the driver circuit is used as an analog switch.

12. A semiconductor device according to claim 8 wherein the p-channel TFT of the driver circuit is used as an analog switch.

13. A semiconductor device according to claim 1 wherein gate electrodes of the pixel TFT and the p-cannel TFT and the n-channel TFT of the driver circuit comprise a heat resistant conductive material and a gate wiring extended from the driver circuit and connected to the gate electrodes comprises a low resistive conductive material.

14. A semiconductor device according to claim 2 wherein gate electrodes of the pixel TFT and the p-cannel TFT and the n-channel TFT of the driver circuit comprise a heat resistant conductive material and a gate wiring extended from the driver circuit and connected to the gate electrodes comprises a low resistive conductive material.

15. A semiconductor device according to claim 3 wherein gate electrodes of the pixel TFT and the p-cannel TFT and the n-channel TFT of the driver circuit comprise a heat resistant conductive material and a gate wiring extended from the driver circuit and connected to the gate electrodes comprises a low resistive conductive material.

16. A semiconductor device according to claim 4 wherein gate electrodes of the pixel TFT and the p-cannel TFT and the n-channel TFT of the driver circuit comprise a heat resistant conductive material and a gate wiring extended from the driver circuit and connected to the gate electrodes comprises a low resistive conductive material.

17. A semiconductor device according to claim 13 wherein the heat resistant material is an element selected from a group consisting of tantalum (Ta), titanium (Ti), molybdenum (Mo) and tungsten (W), a compound comprising the element, a compound combining the elements, a nitride comprising the element or a silicide

comprising the element.

18. A semiconductor device according to claim 14 wherein the heat resistant material is an element selected from a group consisting of tantalum (Ta), titanium (Ti), molybdenum (Mo) and tungsten (W), a compound comprising the element, a compound combining the elements, a nitride comprising the element or a silicide comprising the element.

19. A semiconductor device according to claim 15 wherein the heat resistant material is an element selected from a group consisting of tantalum (Ta), titanium (Ti), molybdenum (Mo) and tungsten (W), a compound comprising the element, a compound combining the elements, a nitride comprising the element or a silicide comprising the element.

20. A semiconductor device according to claim 16 wherein the heat resistant material is an element selected from a group consisting of tantalum (Ta), titanium (Ti), molybdenum (Mo) and tungsten (W), a compound comprising the element, a compound combining the elements, a nitride comprising the element or a silicide comprising the element.

21. A semiconductor device according to claim 3 wherein the columnar spacer is formed over the p-channel TFT and the n-channel TFT of the driver circuit.

22. A semiconductor device according to claim 4 wherein the columnar spacer is formed over the p-channel TFT and the n-channel TFT of the driver circuit.

23. A semiconductor device according to claim 3 wherein the columnar spacer is formed to cover at least a source wiring or a drain wiring of the p-channel TFT and the n-channel TFT of the driver circuit.

24. A semiconductor device according to claim 4 wherein the columnar spacer is formed to cover at least a source wiring or a drain wiring of the p-channel TFT and the

n-channel TFT of the driver circuit.

25. A semiconductor device according to claim 1 wherein the semiconductor device is selected from a group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic game machine and a projector.

26. A semiconductor device according to claim 2 wherein the semiconductor device is selected from a group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic game machine and a projector.

27. A semiconductor device according to claim 3 wherein the semiconductor device is selected from a group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic game machine and a projector.

28. A semiconductor device according to claim 4 wherein the semiconductor device is selected from a group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic game machine and a projector.

29. A method for forming a semiconductor device comprising a pixel TFT of a pixel section and a driver circuit comprising a p-channel TFT and an n-channel TFT disposed in the periphery of the pixel section over a substrate, comprising the steps of:

forming a base film in contact with the substrate;

forming a plurality of island semiconductor layers over the base film;

forming an n-type impurity region of a first concentration in selected regions of the island semiconductor layers, which form at least a LDD region that partly overlaps a gate electrode of the n-channel TFT of the driver circuit;

forming an n-type impurity region of a second concentration in selected regions of the island semiconductor layers, which form at least a LDD region of the pixel TFT;

forming an n-type impurity region of a third concentration in selected regions of the island semiconductor layers, which form at least a source region or a drain region in the n-channel TFT of the driver circuit and the pixel TFT;

forming a p-type impurity region of a fourth concentration in selected regions of the island semiconductor layers, which form at least a source region or a drain region of the p-channel TFT of the driver circuit;

forming a protective insulating film comprising an inorganic insulating material over gate electrodes of: the pixel TFT; and the n-channel TFT and the p-channel TFT of the driver circuit;

forming an interlayer insulating film comprising an organic insulating material in contact with the protective insulating film; and

forming a pixel electrode having a light reflecting surface over the interlayer insulating film, which pixel electrode is connected to the pixel TFT.

30. A method for forming a semiconductor device comprising a pixel TFT of a pixel section and a driver circuit comprising a p-channel TFT and an n-channel TFT disposed in the periphery of the pixel section over a substrate, comprising the steps of:

forming a base film over the substrate;

forming a plurality of island semiconductor layers over the base film;

forming an n-type impurity region of a first concentration in selected regions of the island semiconductor layers, which form at least a LDD region that partly overlaps a gate electrode of the n-channel TFT of the driver circuit;

forming an n-type impurity region of a second concentration in selected regions of the island semiconductor layers, which form at least a LDD region of the pixel TFT;

forming an n-type impurity region of a third concentration in selected regions of the island semiconductor layers, which form at least a source region or a drain region in the n-channel TFT of the driver circuit and the pixel TFT;

forming a p-type impurity region of a fourth concentration in selected regions of the island semiconductor layers, which form at least a source region or a drain region of the p-channel TFT of the driver circuit;

forming a protective insulating film comprising an inorganic insulating material over gate electrodes of: the pixel TFT; and the n-channel TFT and the p-channel TFT of the driver circuit;

forming an interlayer insulating film comprising an organic insulating material in contact with the protective insulating film;

forming a conductive metal wiring that is connected to the pixel TFT; and

forming a pixel electrode comprising a transparent conductive film that is connected to the conductive metal wiring, over the interlayer insulating film.

31. A method for forming a semiconductor device which holds liquid between a pair of substrates,

wherein the manufacturing method for one of the substrates which comprises a pixel TFT disposed in a pixel section and a p-channel TFT and an n-channel TFT of a driver circuit comprises the steps of:

forming a base film over the substrate;

forming a plurality of island semiconductor layers over the base film;

forming an n-type impurity region of a first concentration in selected regions of the island semiconductor layers, which form at least a LDD region that partly overlaps a gate electrode of the n-channel TFT of the driver circuit;

forming an n-type impurity region of a second concentration in selected regions of the island semiconductor layers, which form at least a LDD region of the pixel TFT;

forming an n-type impurity region of a third concentration in selected regions of the island semiconductor layers, which form at least a source region or a drain region in the n-channel TFT of the driver circuit and the pixel TFT;

forming a p-type impurity region of a fourth concentration in selected regions of the island semiconductor layers, which form at least a source region or a drain region of the p-channel TFT of the driver circuit;

forming a protective insulating film comprising an inorganic insulating material over gate electrodes of: the pixel TFT; and the n-channel TFT and the p-channel TFT of the driver circuit;

forming an interlayer insulating film comprising an organic insulating material in contact with the protective insulating film; and

forming a pixel electrode having a light reflecting surface over the interlayer insulating film, which is connected to the pixel TFT through an opening disposed in the interlayer insulating film and the protective insulating film,

wherein a manufacturing method for the other substrate comprises at least a step of forming a transparent conductive film, and

said one of the substrates and the other substrate are stuck together through at least a columnar spacer formed in superposition of the opening.

32. A method for forming a semiconductor device which holds liquid between a pair of substrates,

wherein the manufacturing method for one of the substrates which comprises a pixel TFT disposed in a pixel section and a p-channel TFT and an n-channel TFT of a driver circuit comprises the steps of:

forming a base film over the substrate;

forming a plurality of island semiconductor layers over the base film;

forming an n-type impurity region of a first concentration in selected regions of the island semiconductor layers, which form at least a LDD region that partly overlaps a gate electrode of the n-channel TFT of the driver circuit;

forming an n-type impurity region of a second concentration in selected regions of the island semiconductor layers, which form at least a LDD region of the pixel TFT;

forming an n-type impurity region of a third concentration in selected regions of the island semiconductor layers, which form at least a source region or a drain region in the n-channel TFT of the driver circuit and the pixel TFT;

forming a p-type impurity region of a fourth concentration in selected regions of the island semiconductor layers, which form at least a source region or a drain region of the p-channel TFT of the driver circuit;

forming a protective insulating film comprising an inorganic insulating material over gate electrodes of: the pixel TFT; and the n-channel TFT and the p-channel TFT of the driver circuit;

forming an interlayer insulating film comprising an organic insulating material in contact with the protective insulating film;

forming a conductive metal wiring which is connected to the pixel TFT through an opening disposed in the interlayer insulating film and the protective insulating film; and

forming a pixel electrode comprising a transparent conductive film over the interlayer insulating film, which is connected to the metal wiring,

wherein a manufacturing method for the other substrate comprises at least a step of forming a transparent conductive film, and

said one of the substrates and the other substrate are stuck together through at least a columnar spacer formed in superposition of the opening.

33. A method for forming a semiconductor device according to claim 29 wherein the step of forming the p-type impurity region of the fourth concentration in selected regions of the island semiconductor layers which form at least a source region or a drain region of the p-channel TFT, is performed after the step of forming a protective insulating film comprising an inorganic insulating material over a gate electrode of the pixel TFT, thereby forming an offset region between the channel forming region and the p-type impurity region of the fourth concentration which forms a source region or a drain region.

34. A method for forming a semiconductor device according to claim 30 wherein the step of forming the p-type impurity region of the fourth concentration in selected regions of the island semiconductor layers which form at least a source region or a drain region of the p-channel TFT, is performed after the step of forming a protective insulating film comprising an inorganic insulating material over a gate electrode of the pixel TFT, thereby forming an offset region between the channel forming region and the p-type impurity region of the fourth concentration which forms a source region or a drain region.

35. A method for forming a semiconductor device according to claim 31 wherein the step of forming the p-type impurity region of the fourth concentration in selected regions of the island semiconductor layers which form at least a source region or a drain region of the p-channel TFT, is performed after the step of forming a protective insulating film comprising an inorganic insulating material over a gate electrode of the pixel TFT, thereby forming an offset region between the channel forming region and the p-type impurity region of the fourth concentration which forms a source region or a drain region.

36. A method for forming a semiconductor device according to claim 32 wherein the step of forming the p-type impurity region of the fourth concentration in selected regions of the island semiconductor layers which form at least a source region or a drain region of the p-channel TFT, is performed after the step of forming a protective insulating film comprising an inorganic insulating material over a gate electrode of the pixel TFT, thereby forming an offset region between the channel forming region and the p-type impurity region of the fourth concentration which forms a source region or a drain region.

37. A method for manufacturing a semiconductor device according to claim 29 further comprising the steps of:

forming gate electrodes of the pixel TFT of the pixel section, and of the p-channel TFT and the n-channel TFT disposed in the periphery of the pixel section, from a heat resistant conductive material; and

forming a gate wiring that is extended from the driver circuit and is connected to the gate electrodes from a low resistive conductive material.

38. A method for manufacturing a semiconductor device according to claim 30 further comprising the steps of:

forming gate electrodes of the pixel TFT of the pixel section, and of the p-channel TFT and the n-channel TFT disposed in the periphery of the pixel section, from a heat resistant conductive material; and

forming a gate wiring that is extended from the driver circuit and is connected to the gate electrodes from a low resistive conductive material.

39. A method for manufacturing a semiconductor device according to claim 31 further comprising the steps of:

forming gate electrodes of the pixel TFT of the pixel section, and of the p-channel TFT and the n-channel TFT disposed in the periphery of the pixel section, from a heat resistant conductive material; and

forming a gate wiring that is extended from the driver circuit and is connected to the gate electrodes from a low resistive conductive material.

40. A method for manufacturing a semiconductor device according to claim 32 further comprising the steps of:

forming gate electrodes of the pixel TFT of the pixel section, and of the p-channel TFT and the n-channel TFT disposed in the periphery of the pixel section, from a heat resistant conductive material; and

forming a gate wiring that is extended from the driver circuit and is connected to the gate electrodes from a low resistive conductive material.

41. A method for manufacturing a semiconductor device according to claim 37 wherein the heat resistant conductive material is formed from an element selected from among a group consisting of tantalum (Ta), titanium (Ti), molybdenum (Mo) and tungsten (W), a compound comprising the element, a compound combining the elements, a nitride which comprising the element or a silicide comprising the element.

42. A method for manufacturing a semiconductor device according to claim 38 wherein the heat resistant conductive material is formed from an element selected from among a group consisting of tantalum (Ta), titanium (Ti), molybdenum (Mo) and tungsten (W), a compound comprising the element, a compound combining the elements, a nitride which comprising the element or a silicide comprising the element.

43. A method for manufacturing a semiconductor device according to claim 39 wherein the heat resistant conductive material is formed from an element selected from among a group consisting of tantalum (Ta), titanium (Ti), molybdenum (Mo) and tungsten (W), a compound comprising the element, a compound combining the

elements, a nitride which comprising the element or a silicide comprising the element.

44. A method for manufacturing a semiconductor device according to claim 40 wherein the heat resistant conductive material is formed from an element selected from among a group consisting of tantalum (Ta), titanium (Ti), molybdenum (Mo) and tungsten (W), a compound comprising the element, a compound combining the elements, a nitride which comprising the element or a silicide comprising the element.

45. A method for manufacturing a semiconductor device according to claim 31 wherein the columnar spacer is further formed over the p-channel TFT and the n-channel TFT of the driver circuit.

46. A method for manufacturing a semiconductor device according to claim 32 wherein the columnar spacer is further formed over the p-channel TFT and the n-channel TFT of the driver circuit.

47. A method for manufacturing a semiconductor device according to claim 31 wherein the columnar spacer is formed so as to cover at least a source wiring or a drain wiring of the p-channel TFT and the n-channel TFT of the driver circuit.

48. A method for manufacturing a semiconductor device according to claim 32 wherein the columnar spacer is formed so as to cover at least a source wiring or a drain wiring of the p-channel TFT and the n-channel TFT of the driver circuit.

49. A method for manufacturing a semiconductor device according to claim 29 wherein the semiconductor device is one selected from a group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic game machine and a projector.

50. A method for manufacturing a semiconductor device according to claim 30 wherein the semiconductor device is one selected from a group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital

video disc player, an electronic game machine and a projector.

51. A method for manufacturing a semiconductor device according to claim 31 wherein the semiconductor device is one selected from a group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic game machine and a projector.

52. A method for manufacturing a semiconductor device according to claim 32 wherein the semiconductor device is one selected from a group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic game machine and a projector.

ABSTRACT OF THE DISCLOSURE

A p channel TFT of a driving circuit has a single drain structure and its n channel TFT, a GOLD structure or an LDD structure. A pixel TFT has the LDD structure. A pixel electrode disposed in a pixel portion is connected to the pixel TFT through a hole bored in at least a protective insulation film formed of an inorganic insulating material and formed above a gate electrode of the pixel TFT, and in an interlayer insulating film disposed on the insulation film in close contact therewith. These process steps use 6 to 8 photo-masks.

FIG. 1A

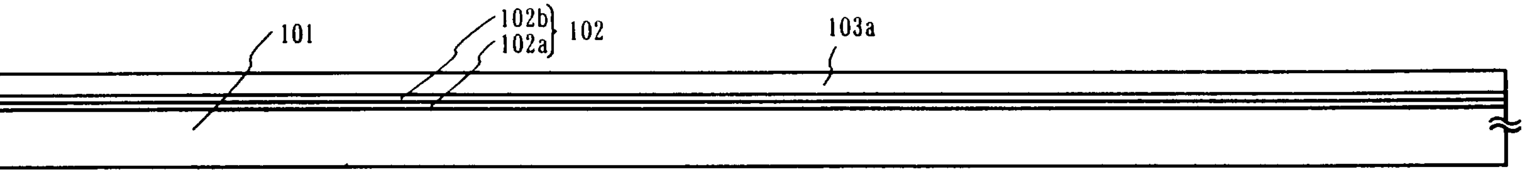


FIG. 1B

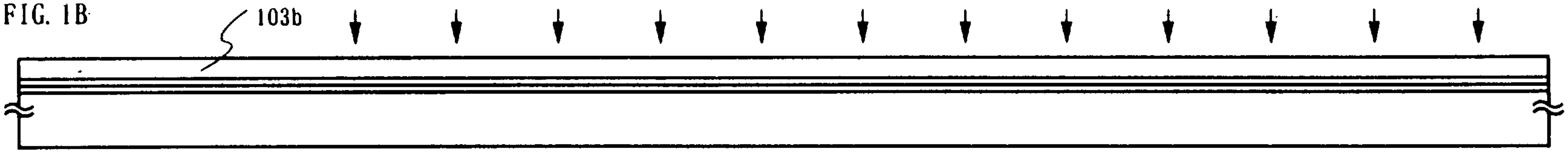


FIG. 1C

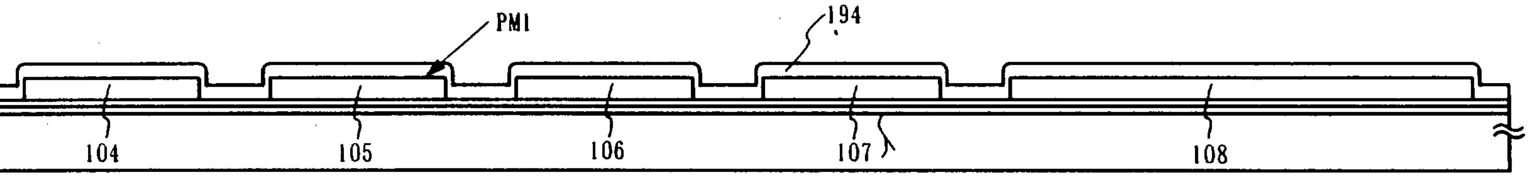


FIG. 1D

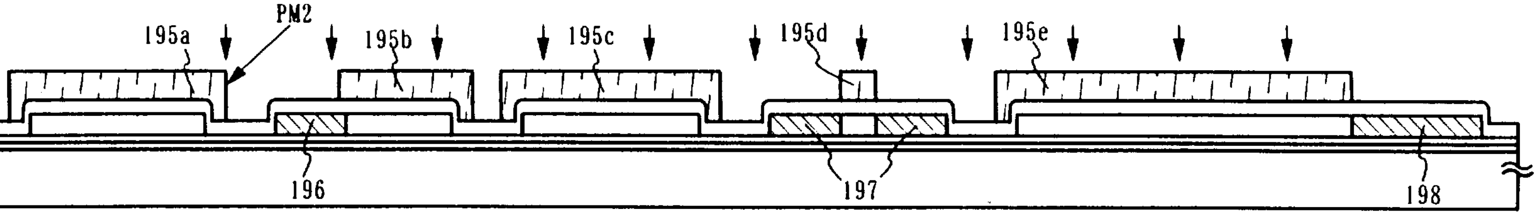


FIG. 1E

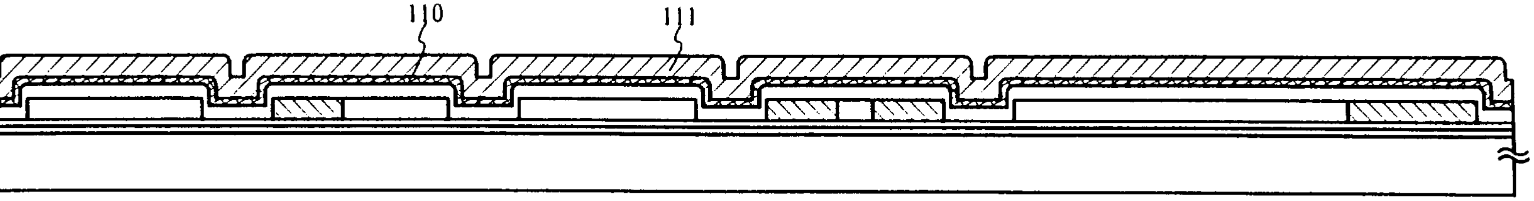


FIG. 2A

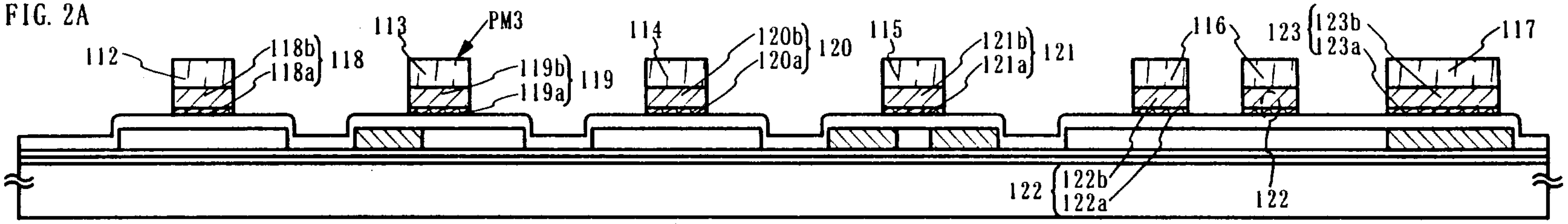


FIG. 2B

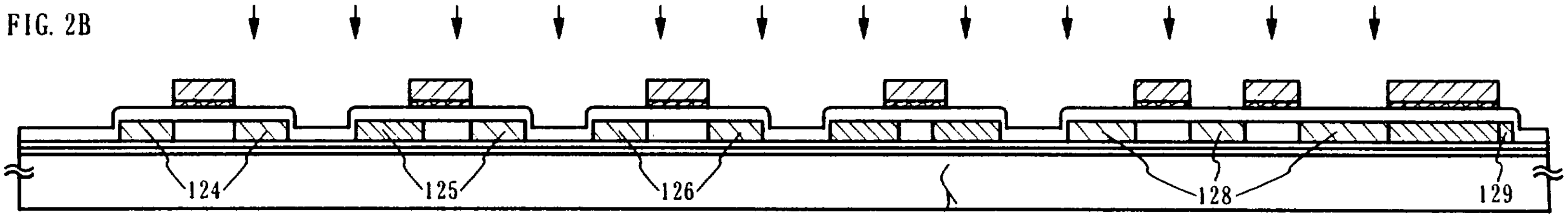


FIG. 2C

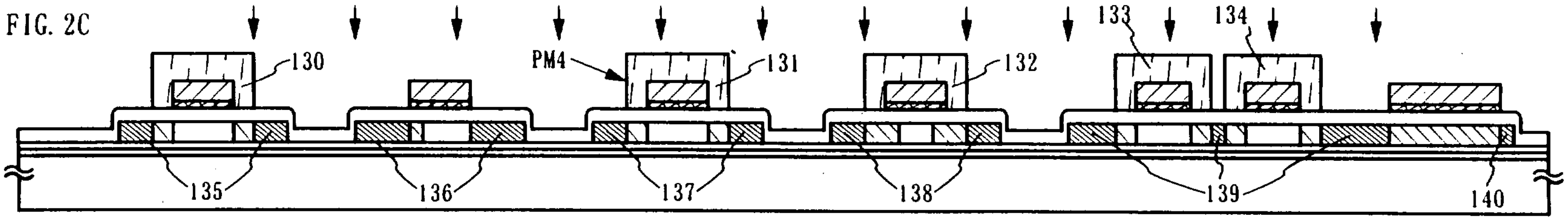


FIG. 2D

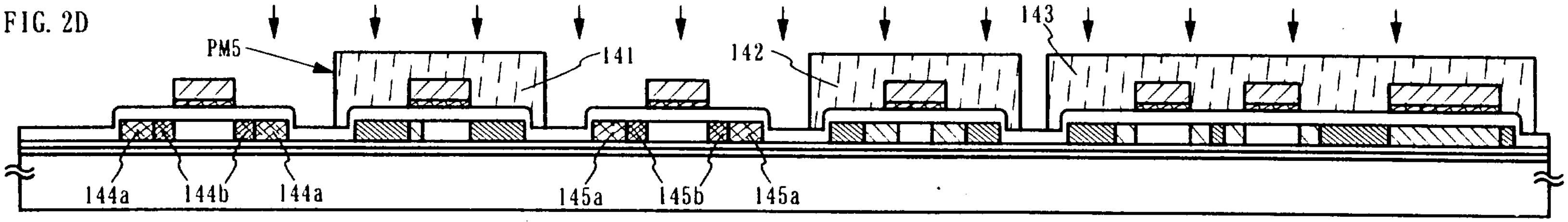


FIG. 3A

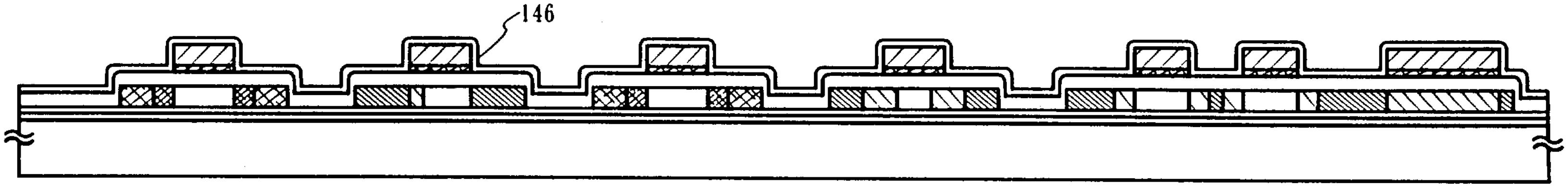


FIG. 3B

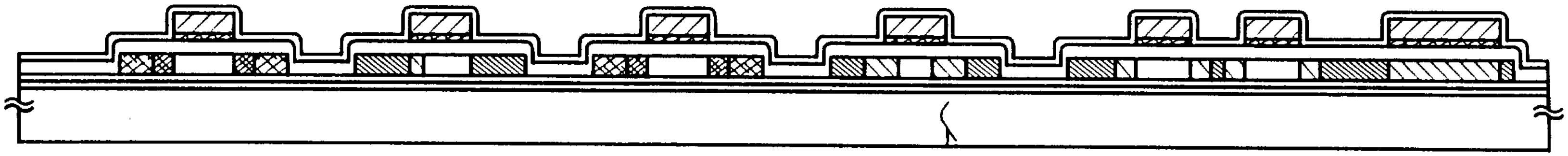


FIG. 3C

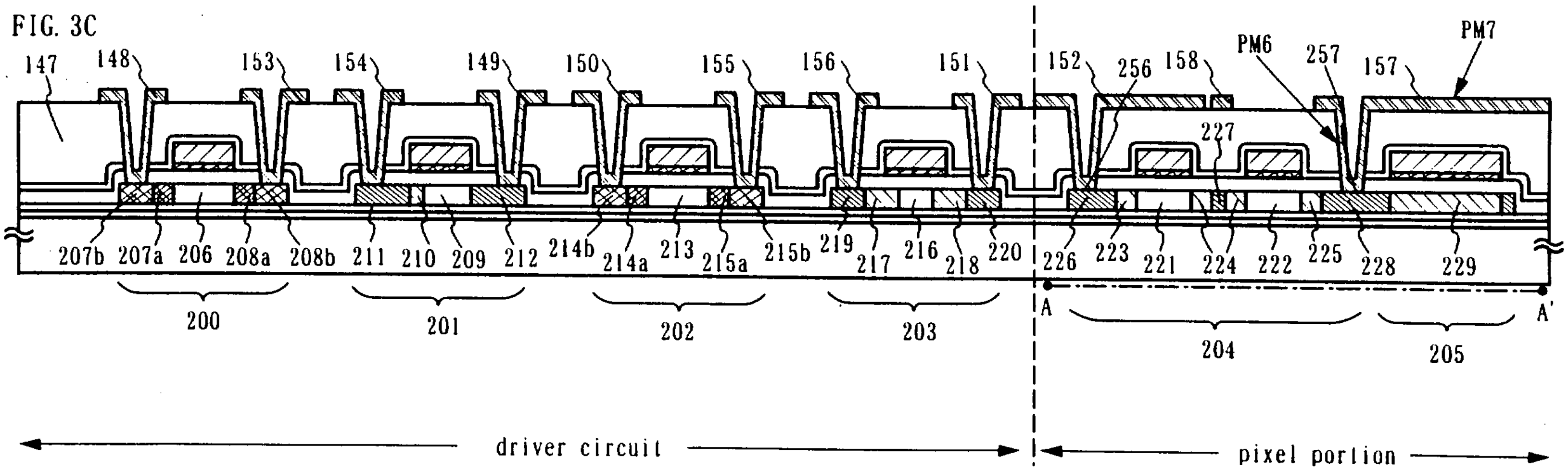


FIG. 4A

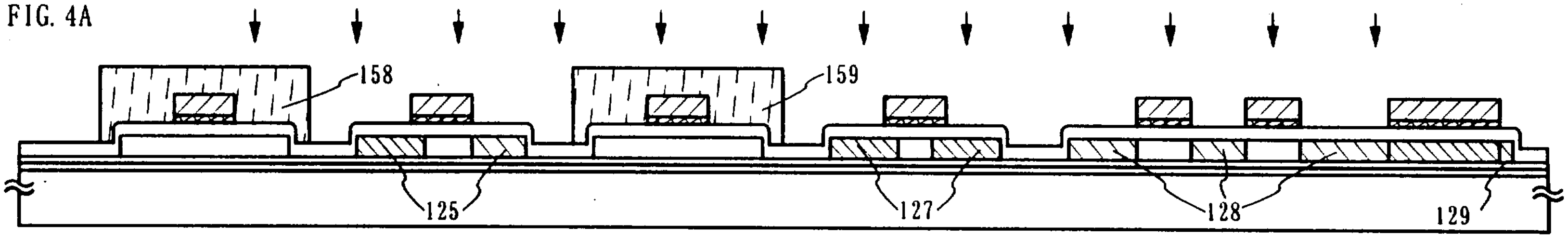


FIG. 4B

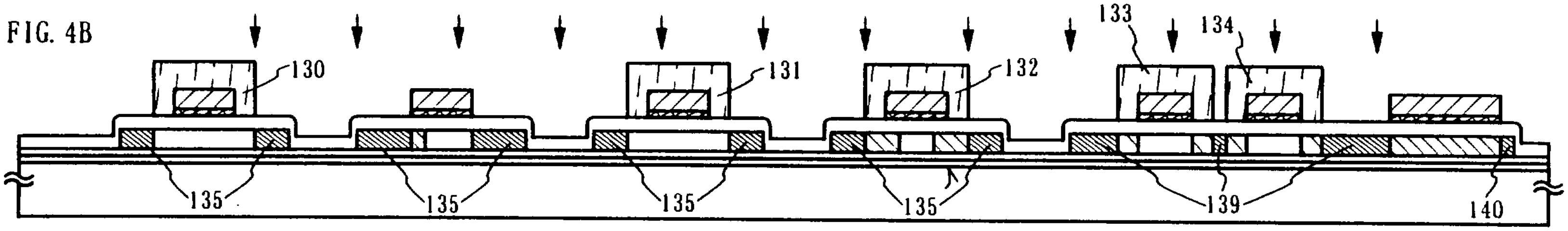


FIG. 4C

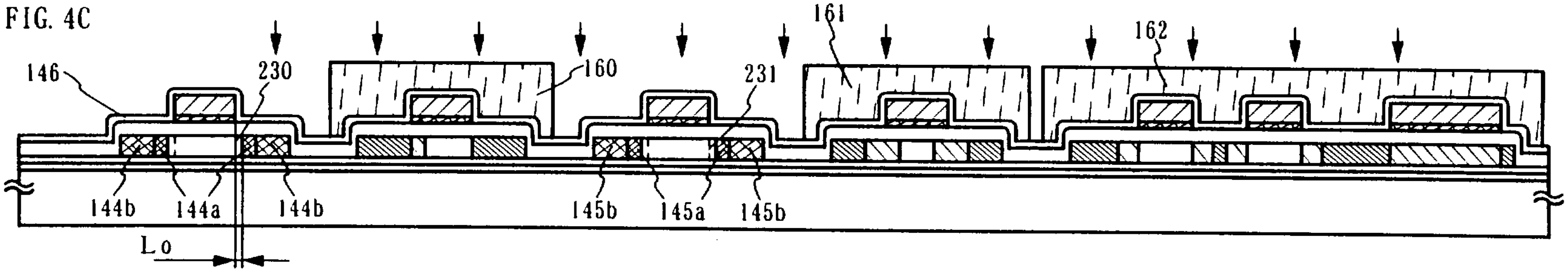


FIG. 5A

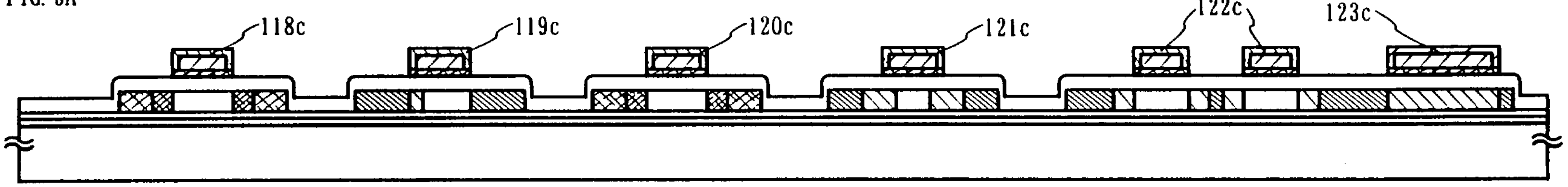


FIG. 5B

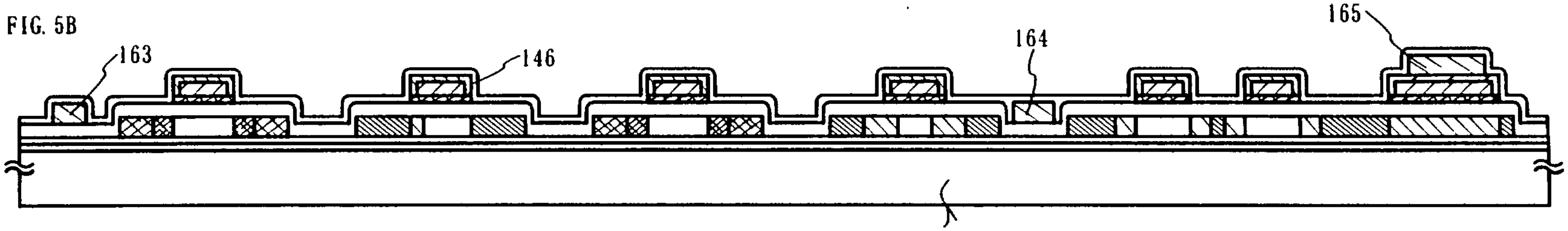
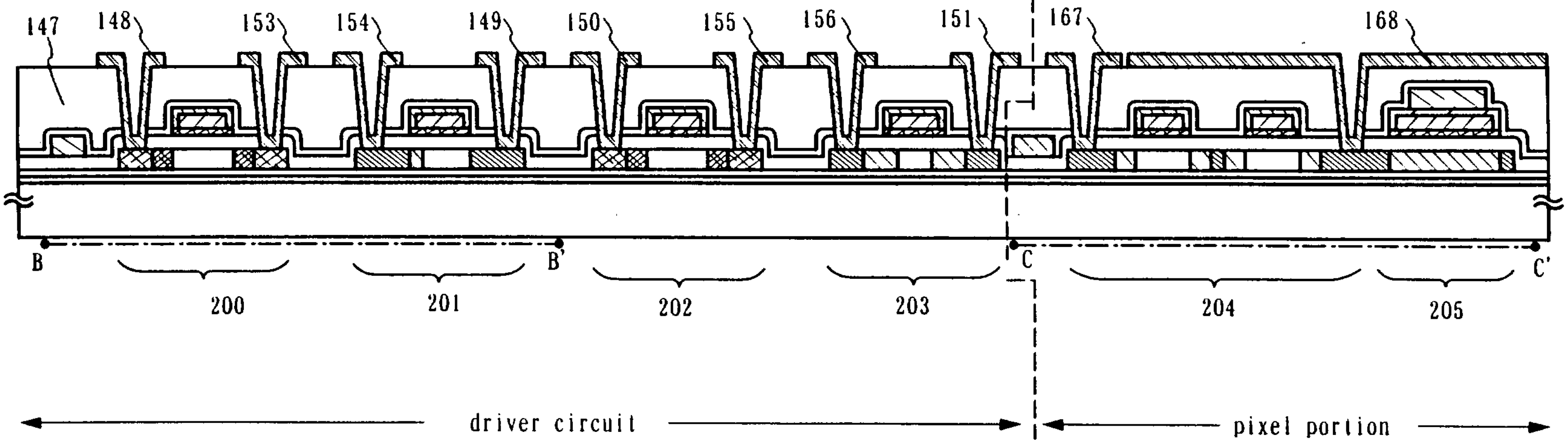


FIG. 5C



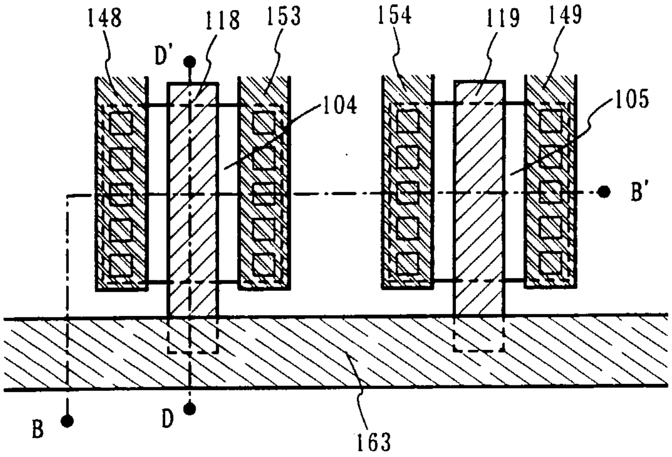

148
118
153
154
119
149
D'
104
105
B'
B
D
163

FIG. 6A

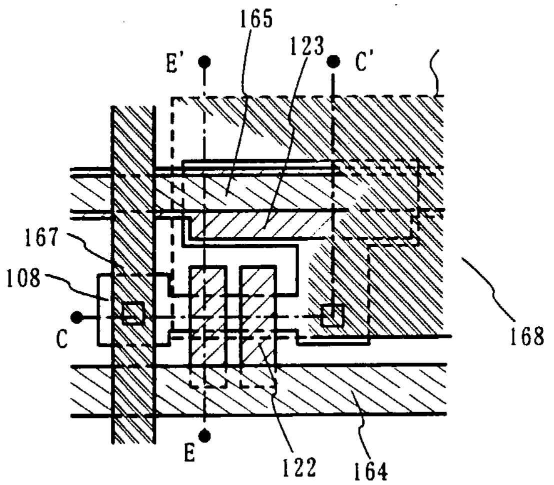

165
123
E'
C'
167
108
C
168
E
122
164

FIG. 6B

FIG. 7A

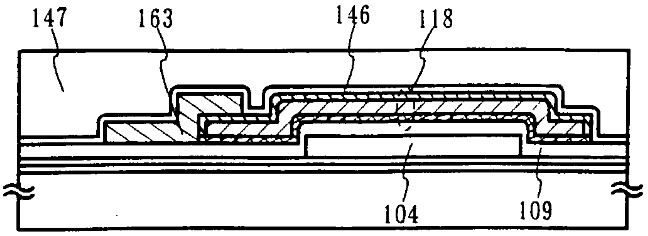


FIG. 7B

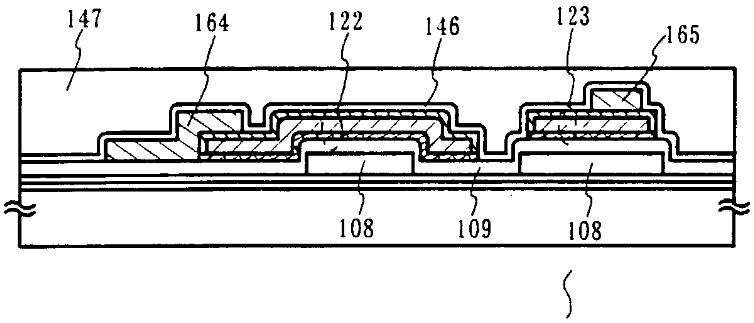


FIG. 8A

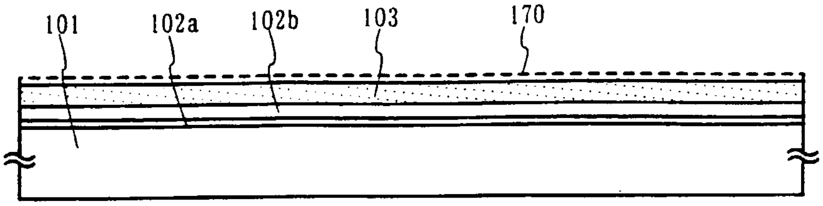


FIG. 8B

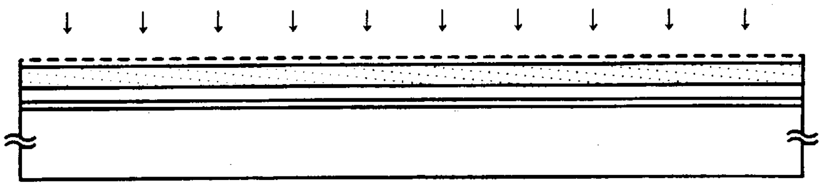


FIG. 8C

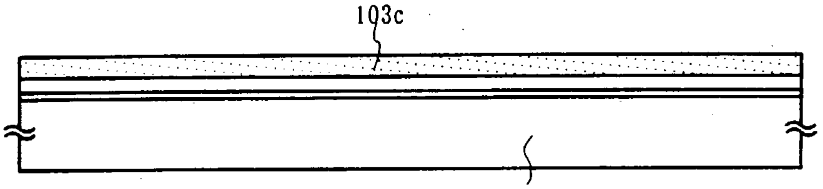


FIG. 9

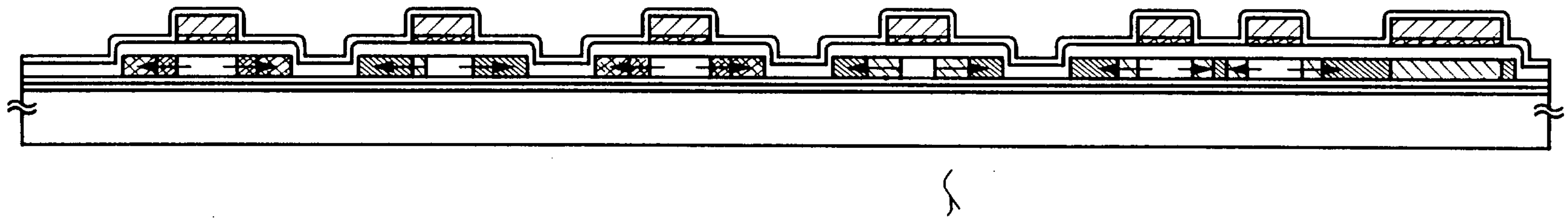


FIG. 10A

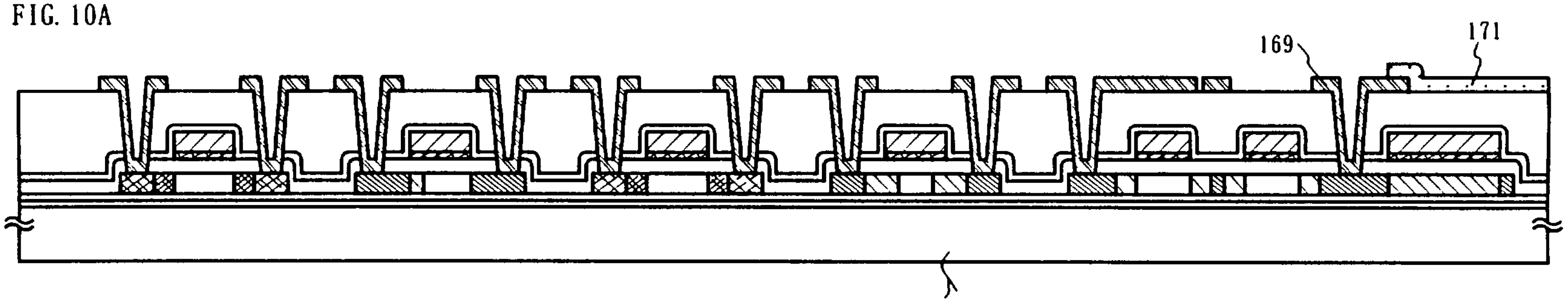


FIG. 10B

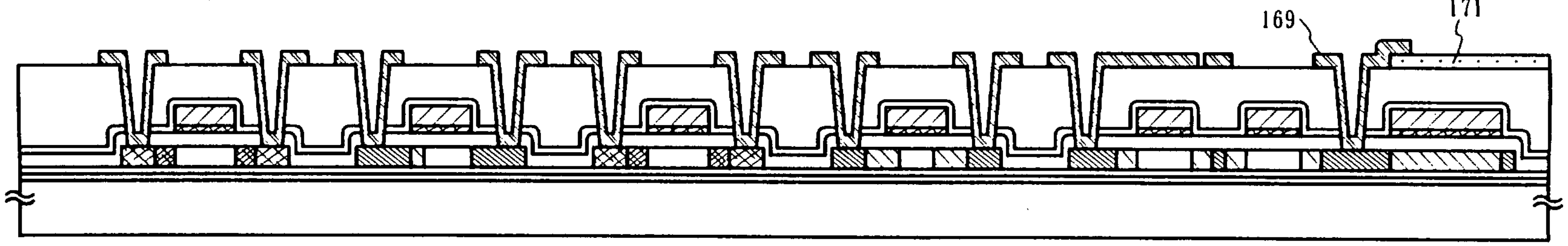


FIG. 11A

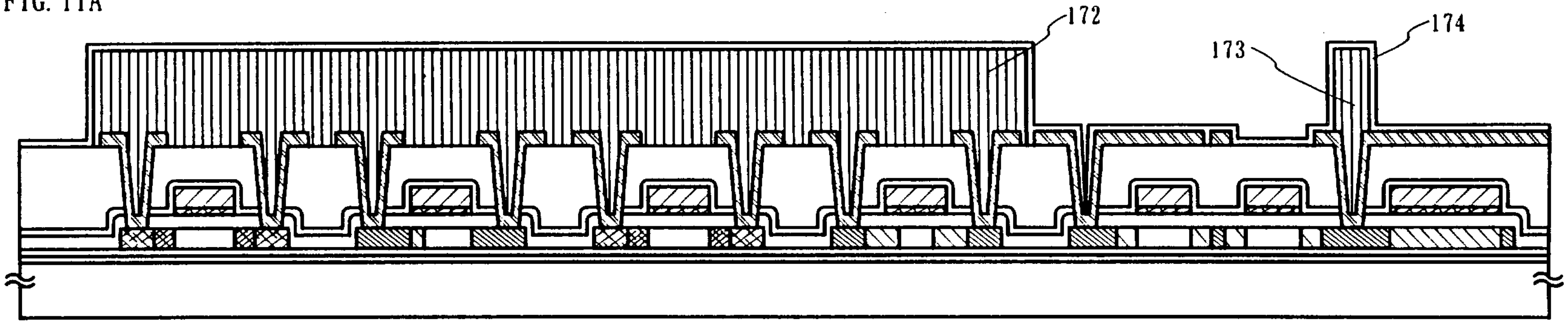


FIG. 11B

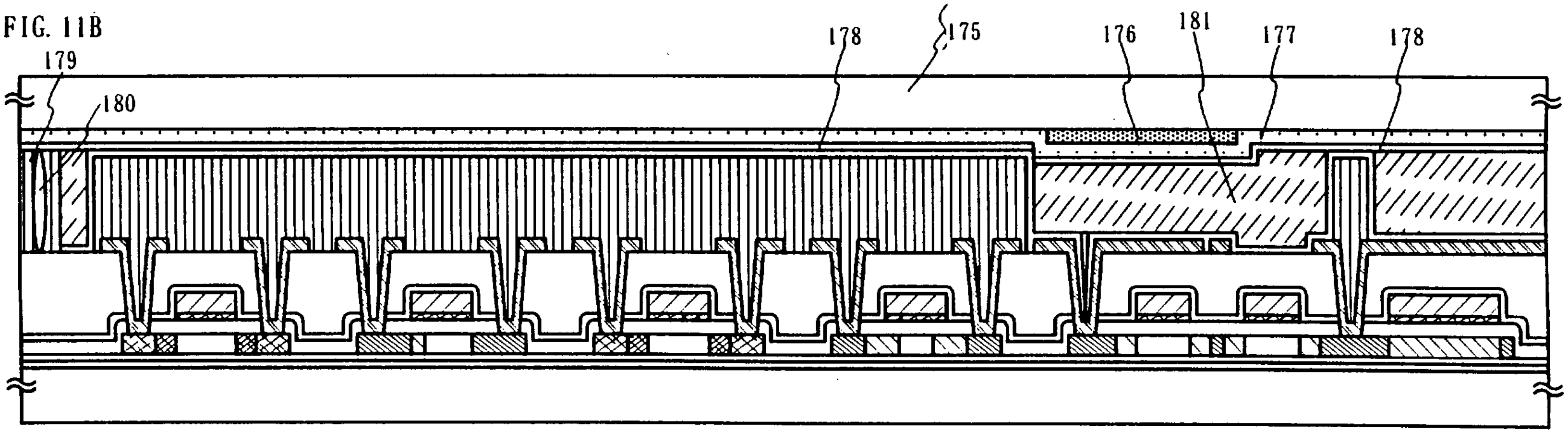
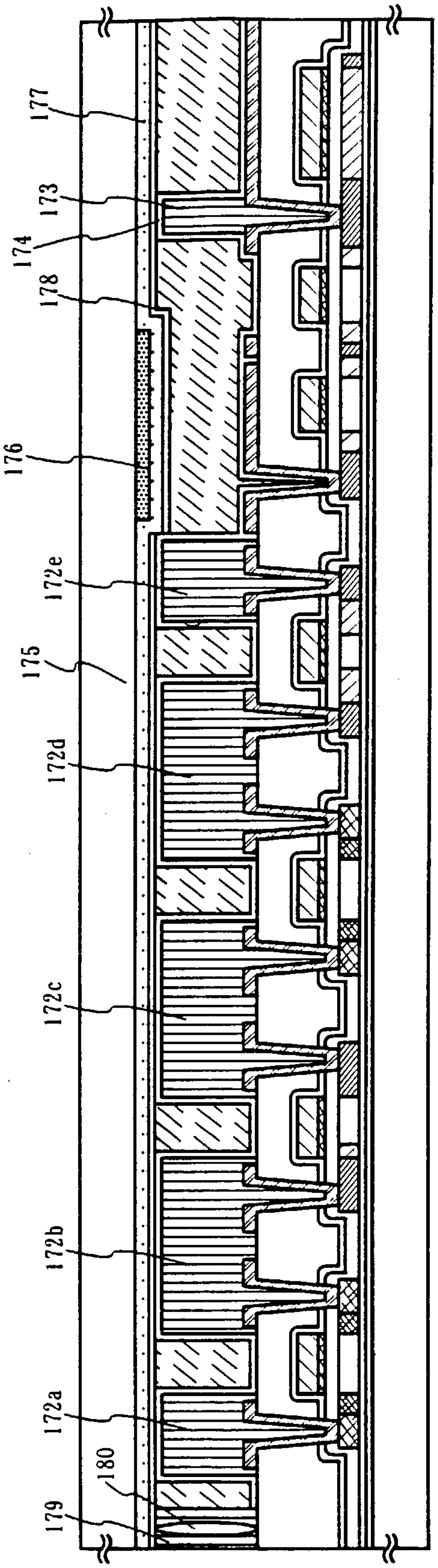


FIG. 12



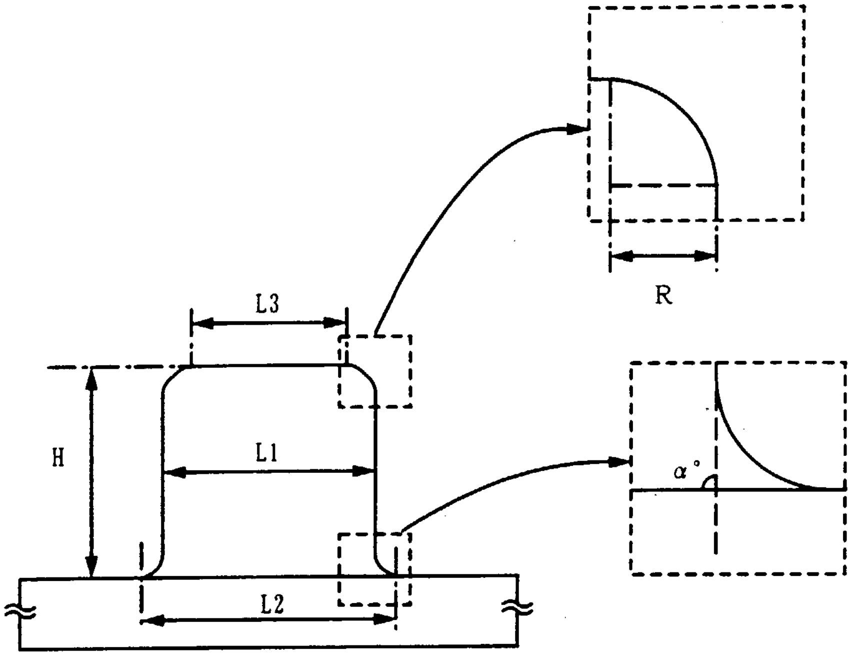


FIG. 13

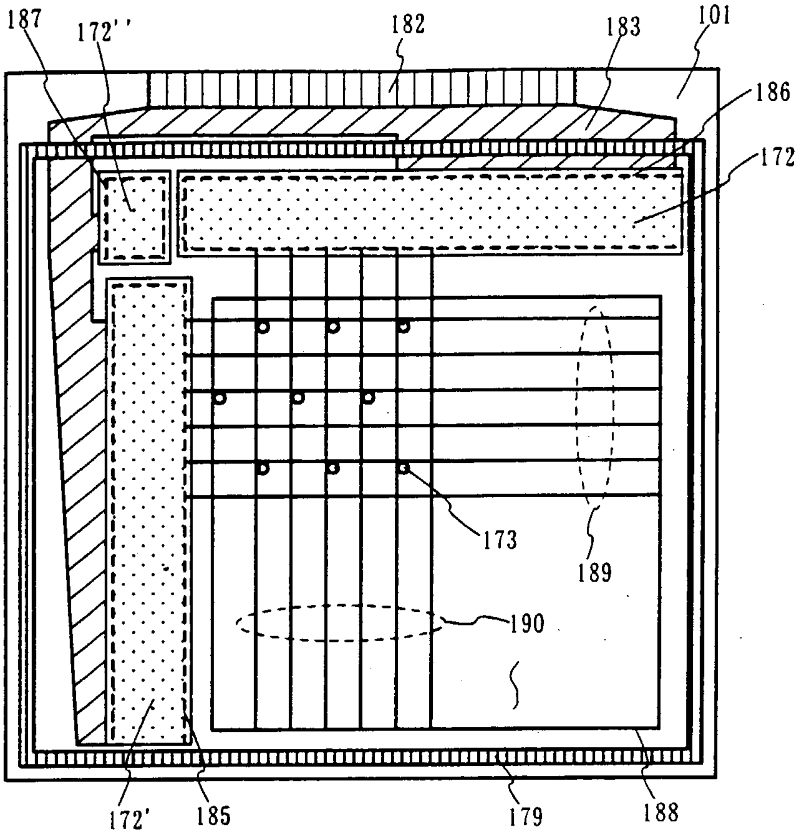


FIG. 14

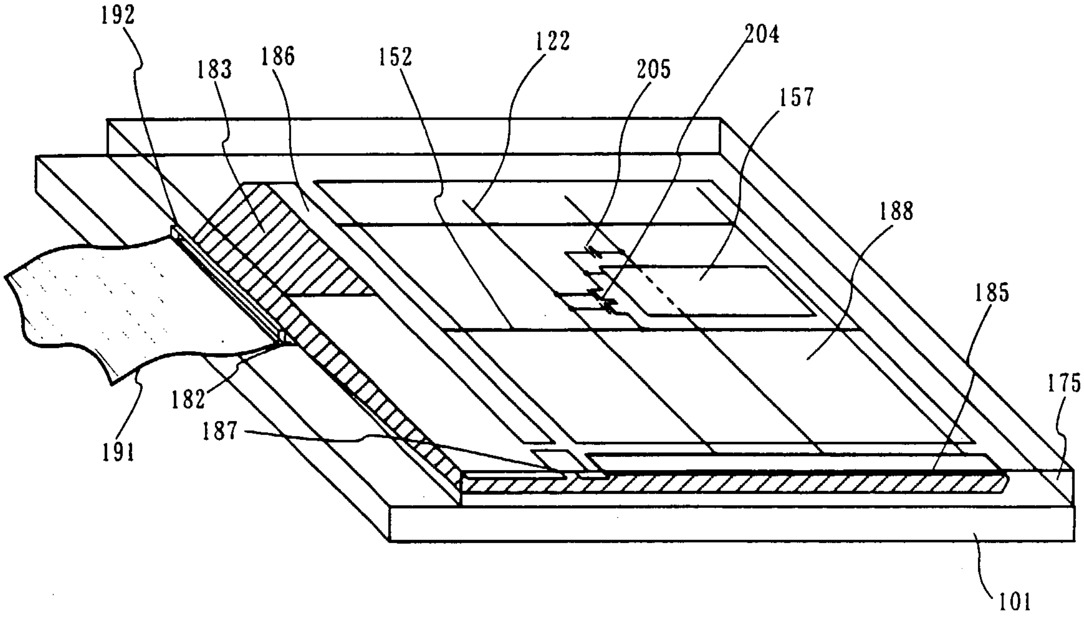


FIG. 15

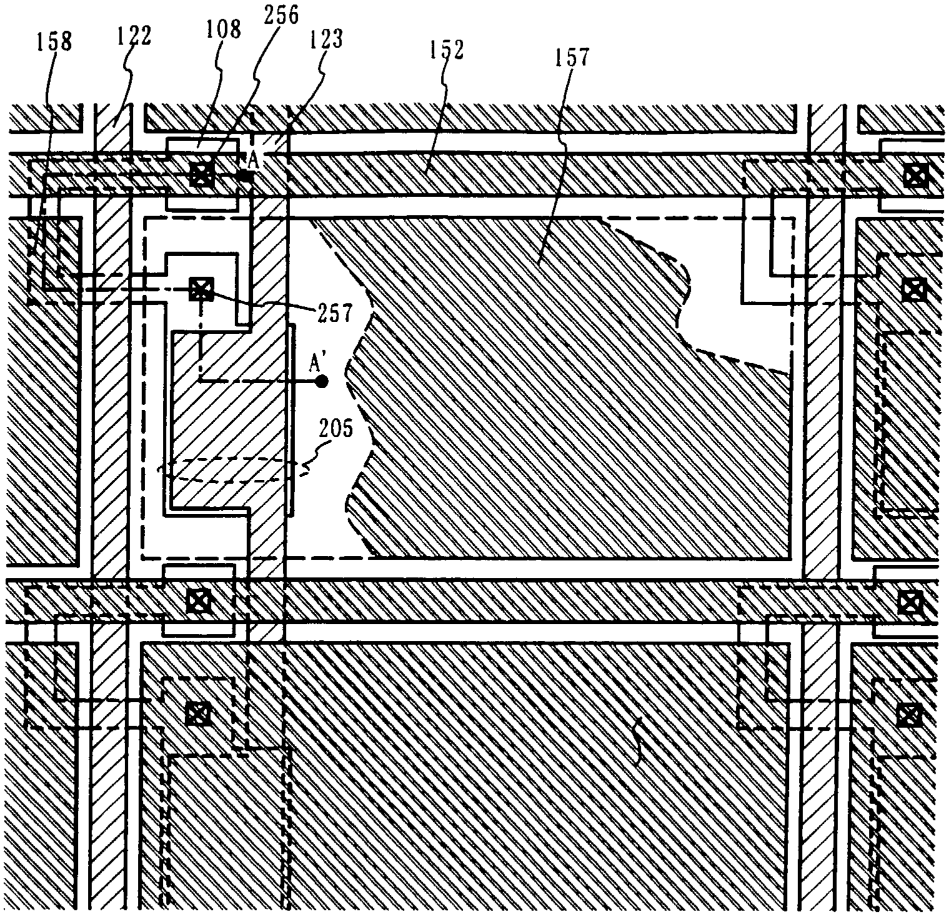


FIG. 16

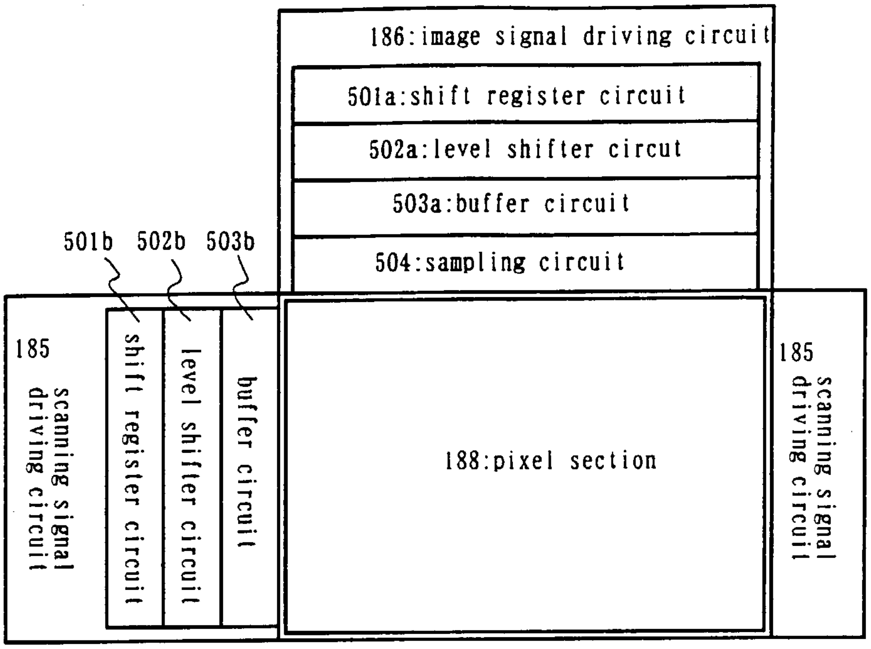

186:image signal driving circuit
501a:shift register circuit
502a:level shifter circut
503a:buffer circuit
504:sampling circuit
501b
502b
503b
185
scanning signal driving circuit
shift register circuit
level shifter circuit
buffer circuit
188:pixel section
185
scanning signal driving circuit

FIG. 17

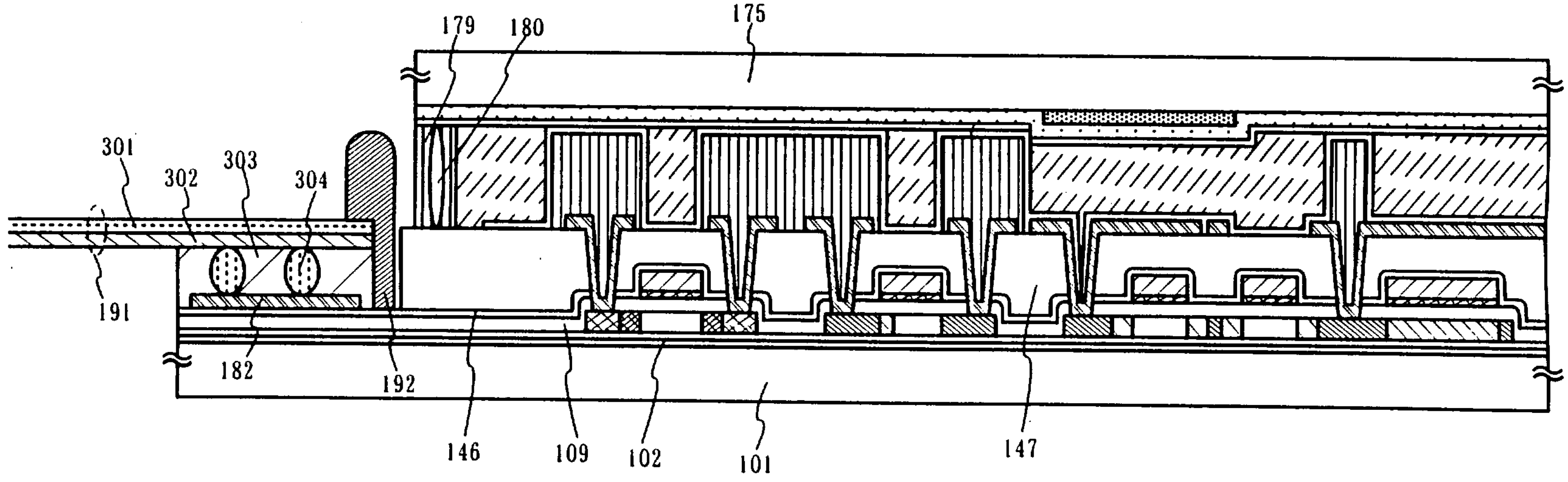


FIG. 18

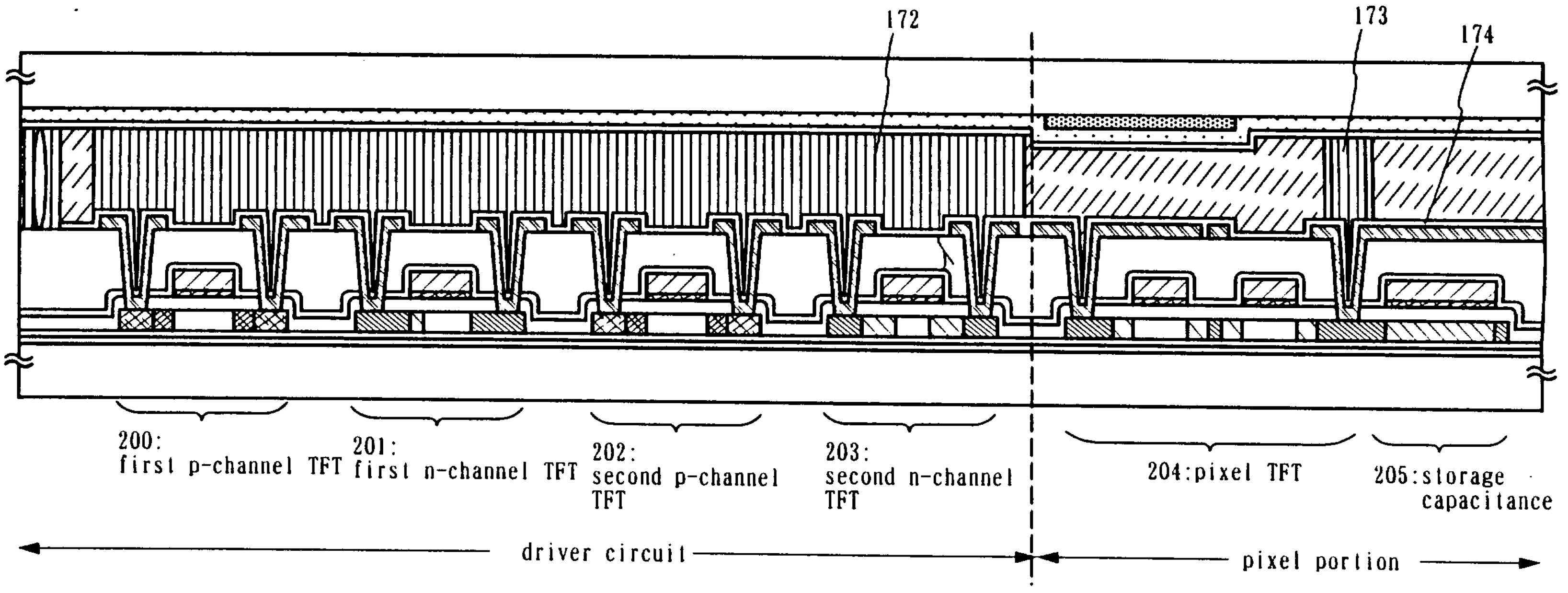

172
173
174
200:
first p-channel TFT
201:
first n-channel TFT
202:
second p-channel TFT
203:
second n-channel TFT
204:pixel TFT
205:storage capacitance
driver circuit
pixel portion

FIG. 19

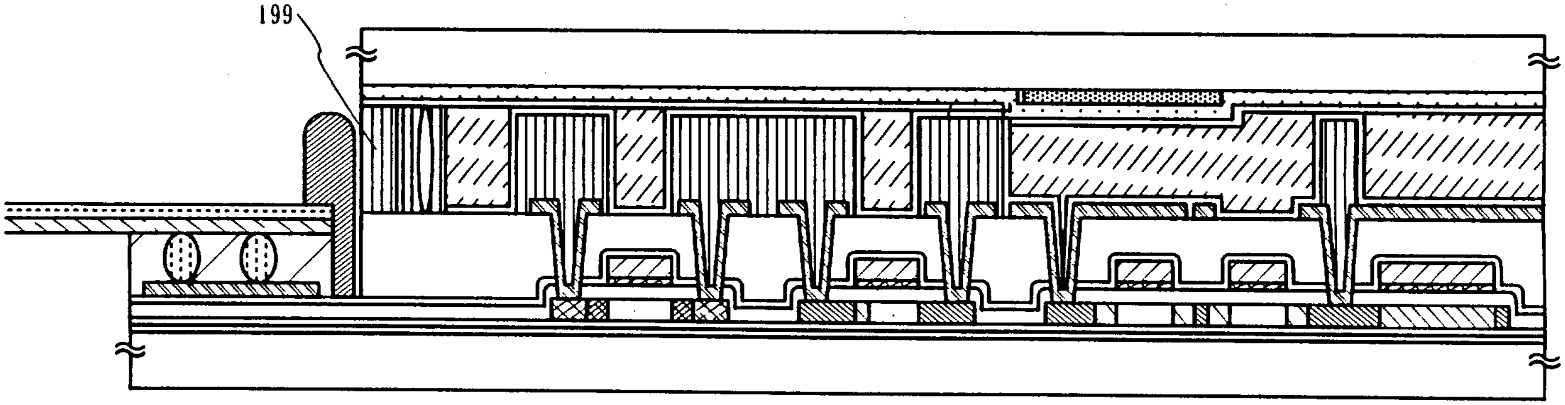


FIG. 20

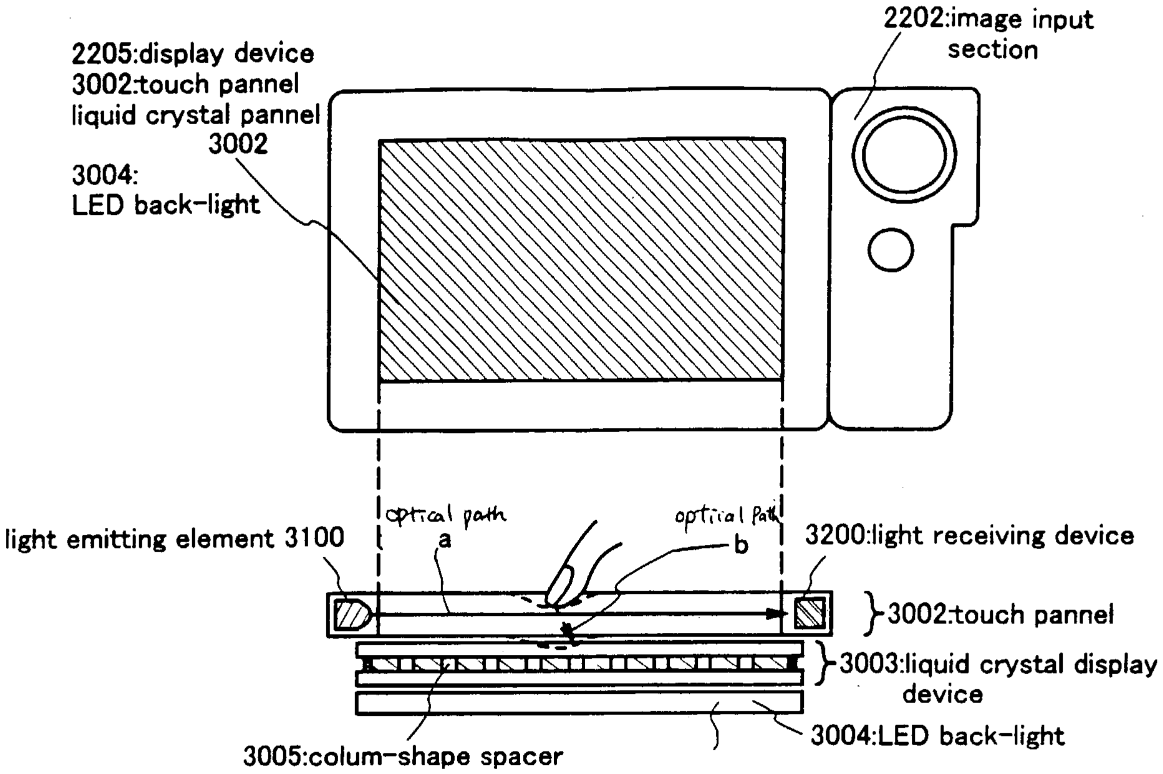


FIG.21A

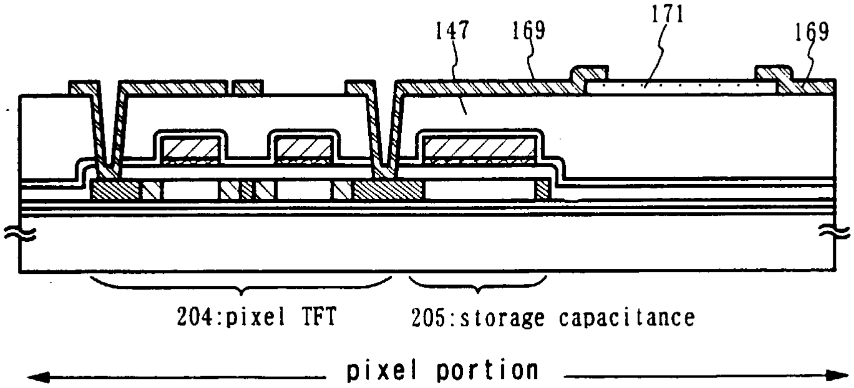


FIG. 21B

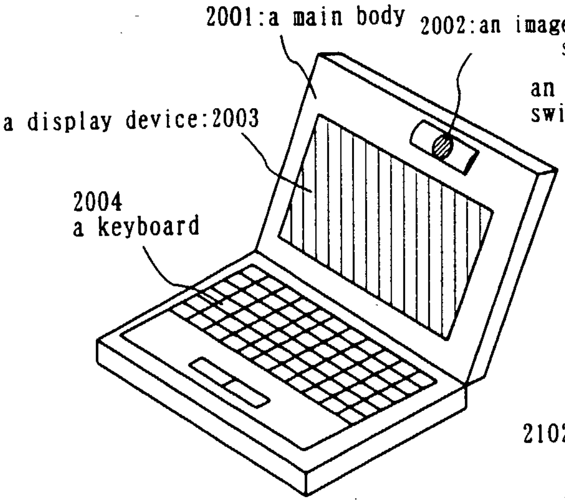


FIG. 22A

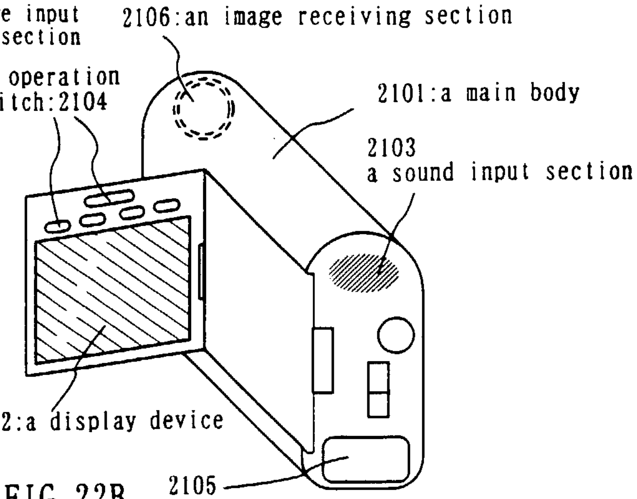


FIG. 22B

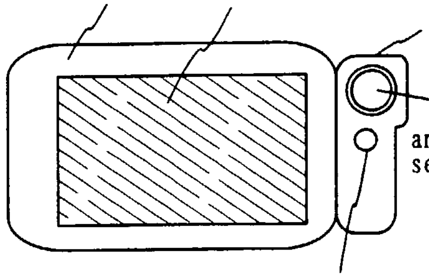


FIG. 22C

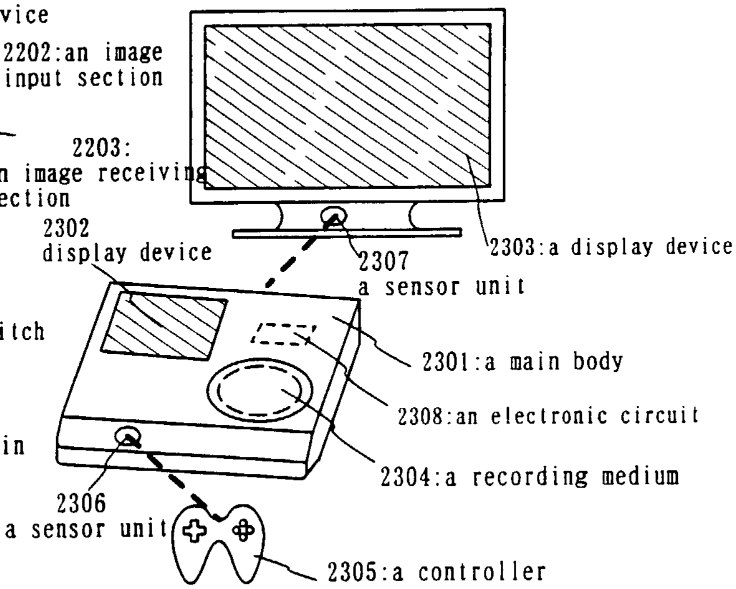


FIG. 22D

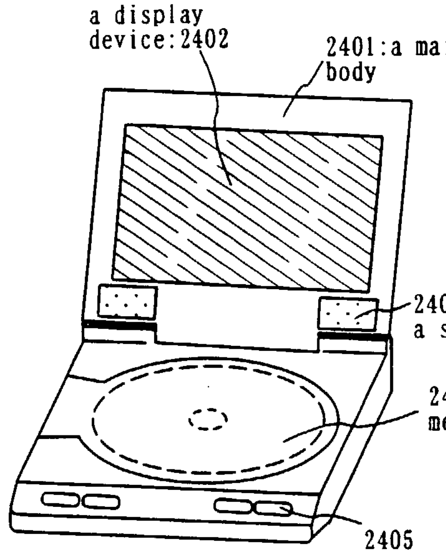


FIG. 22E

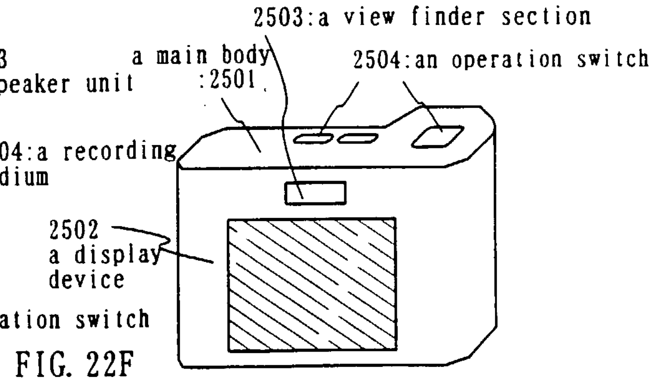


FIG. 22F

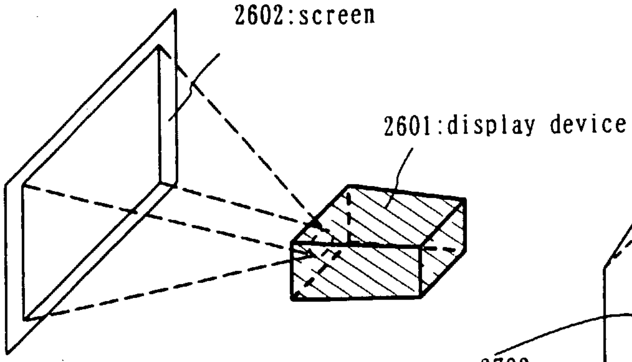


FIG. 23A

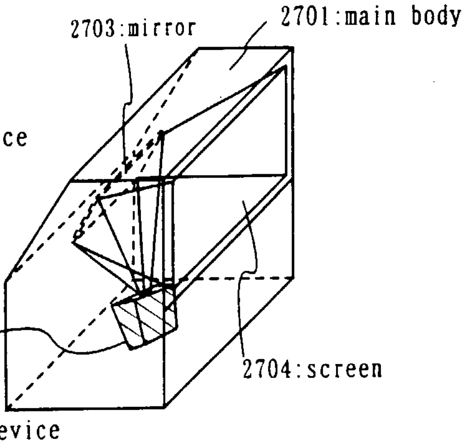


FIG. 23B

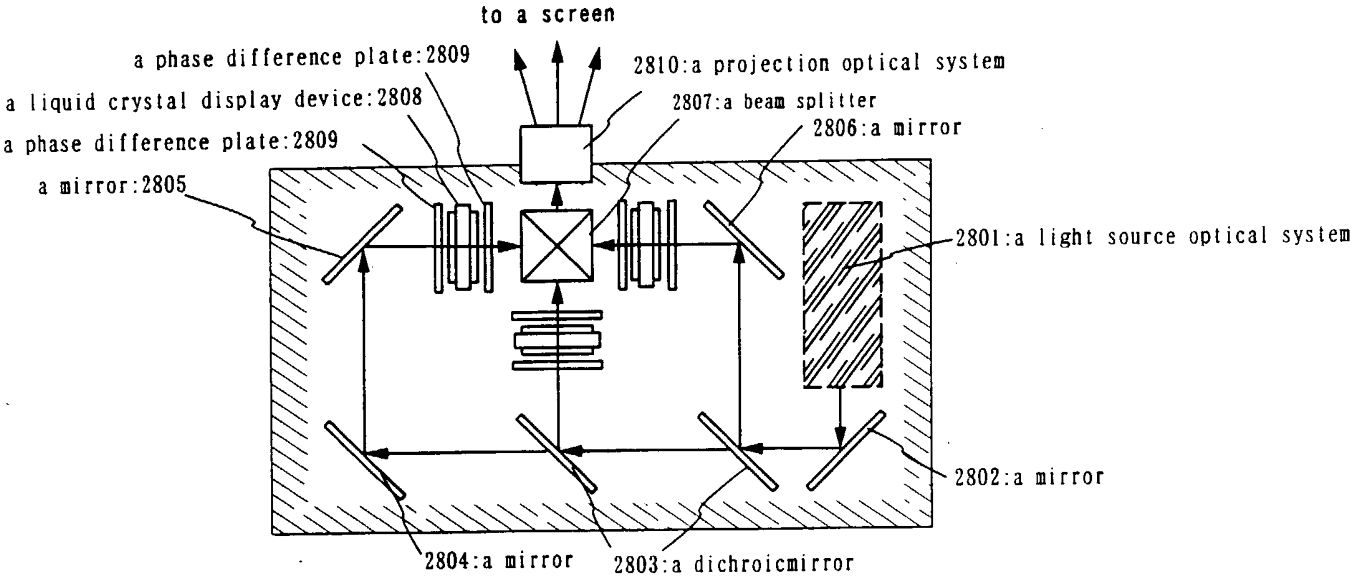

to a screen
a phase difference plate:2809
2810:a projection optical system
a liquid crystal display device:2808
2807:a beam splitter
a phase difference plate:2809
2806:a mirror
a mirror:2805
2801:a light source optical system
2802:a mirror
2804:a mirror
2803:a dichroicmirror

FIG. 23C

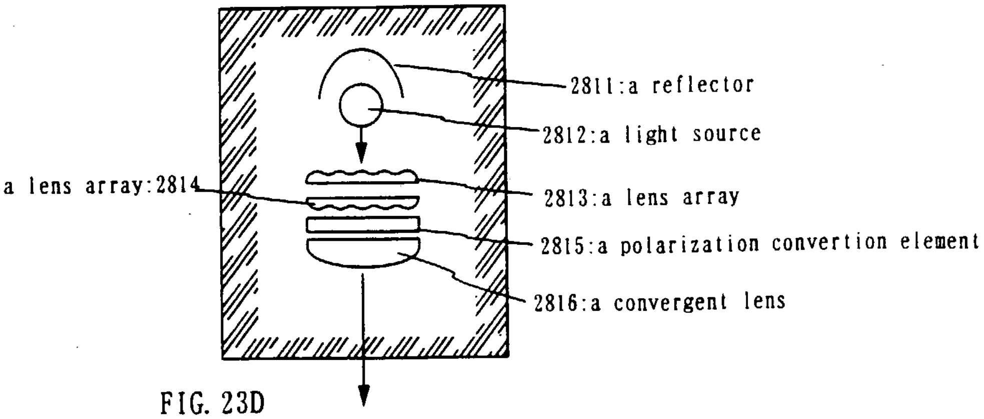


FIG. 23D